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LUIZ ANTÔNIO DA SILVA JÚNIOR

INTEGRATED DC-DC CONVERTER FOR PHOTOVOLTAIC ENERGY HARVESTING TARGETED TO INDOOR APPLICATIONS

Alegrete
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Master's Thesis submitted to the Graduate Program in Electrical Engineering of Federal University of Pampa in partial fulfillment of the requirements for the degree of Master in Electrical Engineering.

Supervisor: Alessandro Gonçalves Girardi
Co-supervisor: Lucas Compassi Severo

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Luiz Antônio da Silva Junior

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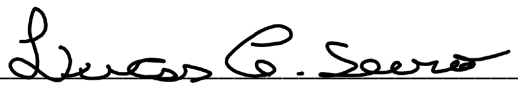

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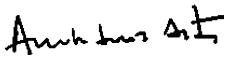

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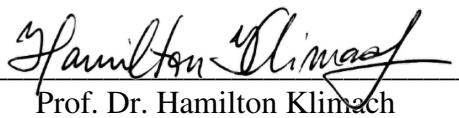

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For the affection, dedication, and care that my parents gave me throughout my existence, I dedicate this work to them. With much gratitude.

"Nothing splendid has ever been achieved
except by those who dared believe that
something inside of them was
superior to circumstance."
(Bruce Barton)

ABSTRACT

Internet of Things (IoT) is a current great trend in which the number of connected devices to the Internet increases over years, thus facilitating the monitoring and control of outdoor and indoor environments. In addition, the majority of electronic devices, mainly peripherals, are used most of the time indoors like office rooms, for example. These devices are usually power supplied by wiring or batteries. The use of wires can sometimes compromise the practicality of some electronic devices, and batteries must be frequently replaced or recharged. Energy harvesting is a great solution to overcome this problem, since the energy provided by the environment, such as lighting, can be harvested by a photovoltaic (PV) cell in order to power supply electronic devices and IoT sensor nodes. The power harvested by PV cells indoors is still quite limited, therefore energy harvesting systems in this type of environment are not widely exploited and target only low power applications. A PV cell may suffer shading caused by walls, furniture, and human movements. This requires an efficient conversion system that can adapt to the PV cell output voltage variations. In this context, the present work aims to propose an integrated conversion system for indoor light energy harvesting to partially replace battery usage in electronic devices and ultra-low-power (ULP) circuits. For the system block responsible for voltage conversion, we propose a reconfigurable DC-DC converter topology based on Switched Capacitor (SC) capable to providing a range of voltage conversion ratios (VCRs). A systematic simulation-based method is also proposed in order to design the conversion system, including switches and capacitors sizes and switching frequency. Results show that the proposed DC-DC converter can adjust itself to achieve 19 different VCRs including fractional, integers, step-down, follower, and step-up with an estimated peak charging efficiency around 90%. In addition, the conversion system can be employed in a vast range of duty-cycled ULP IoT applications. This is an important step towards a practical self-powered indoor system for IoT applications.

Keywords: Switched Capacitor. DC-DC converter. Indoor Energy Harvesting. Photovoltaic Cells. Electronic Devices. Internet of Things. Ultra-Low Power Circuits. Ultra-Low Voltage Circuits.

Conversor CC-CC Integrado para Colheita de Energia Fotovoltaica Voltada para Aplicações em Ambientes Fechados

RESUMO

Internet das Coisas é uma grande tendência atual na qual o número de dispositivos conectados à Internet aumenta ao longo dos anos, facilitando assim o monitoramento e controle de ambientes abertos e fechados. Além disso, a maioria dos dispositivos eletrônicos, principalmente os periféricos, são usados na sua maior parte do tempo dentro de ambientes fechados como salas de escritórios, por exemplo. Esses dispositivos geralmente são alimentados utilizando fios ou baterias. A utilização de fios pode, às vezes, comprometer a praticidade de alguns dispositivos eletrônicos, e baterias devem ser frequentemente trocadas ou recarregadas. A colheita de energia é uma ótima solução para resolver este problema, uma vez que a energia fornecida pelo ambiente, como, por exemplo, a iluminação, pode ser captada por uma célula fotovoltaica para alimentar dispositivos eletrônicos e sensores para Internet das Coisas. A potência captada por células solares em ambientes fechados ainda é bastante limitada, desse modo sistemas para colheita de energia neste tipo de ambiente são pouco explorados e visam somente aplicações de ultra-baixa potência. Uma célula fotovoltaica ainda pode sofrer sombreamentos causados por paredes, móveis e movimentos humanos. Isso exige um sistema de conversão eficiente e que possa se adaptar às variações de tensão de saída de uma célula fotovoltaica. Nesse contexto, o presente trabalho visa propor um sistema integrado de conversão para colheita da energia da iluminação em ambientes fechados para parcialmente substituir o uso da bateria em dispositivos eletrônicos e circuitos de ultrabaixa potência. Para o bloco do sistema responsável pela conversão de tensão, foi proposta uma topologia reconfigurável de conversor CC-CC à capacitores chaveados capaz de fornecer uma faixa de relações de conversão de tensão. Uma metodologia sistemática baseada em simulação elétrica também foi proposta com o intuito de projetar o sistema de conversão, incluindo os tamanhos das chaves, capacitores e a frequência de chaveamento. Resultados mostram que o conversor CC-CC proposto pode se ajustar para fornecer 19 diferentes razões de conversão de tensão incluindo razões de conversão fracionárias, inteiras, rebaixadoras, seguidora e elevadoras com um pico de eficiência de conversão estimado em torno de 90 %. Além do mais, o sistema de conversão pode ser empregado e vários circuitos de ultrabaixa potência que funcionam em ciclos alternados de operação, aplicados em dispositivos de Internet das Coisas. Esse é um passo importante em direção a um sistema prático e autoalimentado empregado em ambientes fechados para aplicações de Internet das Coisas.

Palavras-chave: Capacitor Chaveado. Conversor CC-CC. Colheita de Energia em Ambiente Fechado. Células Fotovoltaicas. Dispositivos Eletrônicos. Internet das Coisas. Circuitos de Ultrabaixa Potência. Circuitos de Ultrabaixa Tensão.

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1 INTRODUCTION

Internet of Things (IoT) is a relatively new term and one of the most trend topics of the present time. The Internet of Things is changing much about the world, from the way we drive to how we make purchases and even for how we get supply energy for our homes. It refers to the interconnection of physical devices from micro-scale electronic circuits to large servers through the Internet. According to the latest research from Strategy Analytics (MERCER, 2019), the number of devices connected to the internet reached 22.0 billion worldwide at the end of 2018. The report also predicts that 38.6 billion devices will be connected by 2025, and 50 billion by 2030.

Wireless Sensor Network (WSN) play a great role in the IoT concept because WSNs are responsible for monitoring and recording the physical conditions of the environment where they are allocated, and organizing the collected data at a central location. They are widely used in many fields including agriculture, transportation, manufacturing, and healthcare (DEMIR; AL-TURJMAN; MUHTAROĞLU, 2018).

There are two widespread ways of power supplying these sensors, by wiring or using batteries. Both of these options may require the same costs as the installation of the sensors, once wiring demands some wires that need to be allocated from the energy supplier to the sensors, and batteries need frequent maintenance to be replaced. Also, the energy capacity of the batteries is very limited in this scope (JUNG et al., 2014).

Apart from WSN, the predominant energy source of the most of electronic devices are batteries. Even with the increase in the energy density of batteries by a factor of 3 over the last 15 years, in several cases, their presence has a large impact, or even dominate, the size and operational cost (VULLERS et al., 2010).

The constant replacement of batteries can harm the environment due to toxic metals such as cadmium, mercury, lead and lithium which some batteries contain and it can pose threats to health and environment if improperly disposed of. Even though batteries represent less than one percent of total solid waste generated, they account for nearly two-thirds of the lead, ninety percent of the mercury, and over half of the cadmium found in the waste (PETERS et al., 2017).

There is a trend in which the number of electronic devices per person has been continuously increasing for decades. In addition, there is another and older trend that is the human tendency of spending a larger amount of time in indoor environments, especially buildings (RANDALL, 2006).

The collection and use of ambient energy in the environment, called energy harvesting or scavenging, is a good alternative in order to avoid the need for user intervention and extra wiring, and it assures that the product is available whenever required. In some applications, this approach can even replace the battery usage (YU et al., 2018).

Energy can be harvested from different ambient sources, and the most commonly used to generate electrical energy are solar, thermal, mechanical movement or vibration,

and ambient radio-frequency (RF) (HARB, 2011). In short, solar energy can be harvested through photovoltaic (PV) panels being exposed to light. Thermoelectric generators (TEGs) are used to extract energy from temperature differences. The vibration or movement-based energy scavenging refers to electrostatic, electromagnetic, and piezoelectric sources. In electrostatic transducers, one electrode moves in relation to another electrode of a polarized capacitor, and the distance or overlap between these two electrodes causes a voltage change across the capacitor and results in a current flow in an external circuit. In piezoelectric transducers, a voltage is generated in a piezoelectric capacitor by the deformations caused by vibrations or movement. In electromagnetic transducers, the relative motion of a magnetic mass with respect to a coil causes a change in the magnetic flux. This generates an AC voltage across the coil. The RF energy available through public telecommunication services, such as GSM and WLAN frequencies, can also be harvested by an appropriate antenna. Alternatively, energy can be harvested using a dedicated RF source positioned close to the sensor node, like RFID sensor networks. Table 1 presents the most usual energy harvesting sources as well as some scenarios with the power which can be harvested from each energy source (VULLERS et al., 2010).

Table 1 – Characteristics of the most common energy harvesting sources.

Source	Source Power	Harvested Power
Ambient Light		
Indoor	0.1 mW/cm^2	10 μW/cm^2
Outdoor	100 mW/cm^2	10 mW/cm^2
Thermal Energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1–10 mW/cm^2
Vibration/Motion		
Human	0.5 m at 1 Hz 1 m/s^2 at 50 Hz	4 μW/cm^2
Industrial	1 m at 5 Hz 10 m/s^2 at 1 kHz	100 μW/cm^2
RF		
GSM Base Station	0.3 μW/cm^2	0.1 μW/cm^2

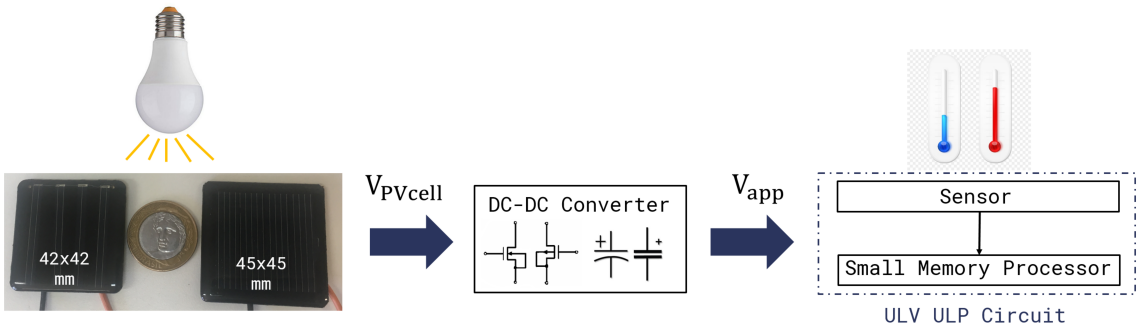
Source: From (VULLERS et al., 2010)

Observing the data presented in Table 1 it can be concluded that harvesting from ambient light is the best option for outdoor applications in terms of practicality and harvesting power since it is possible to harvest with a density up to 10 mW/cm^2 with a density power source of 100 mW/cm^2. Thermal energy performs in a similar way, but industrial-scale temperature differences are not as available as sunlight. Even though indoor ambient light source does not present a higher power density than other indoor sources, there are some advantages in performing indoor solar energy harvesting. In addition to the artificial lighting provided by the lamps, some extra energy may be harvested, at daylight,

from the natural solar radiance through the windows. Even a mixture of these two artificial and natural sources can be used to harvest energy. PV cells are cheap and easy to obtain. They can be built in many different sizes and shapes, and they also allow easy integration with electronic devices and peripherals. In addition, PV cells allow easily association in series and parallel to provide more voltage or current to the load (MENG et al., 2016).

Even with lower energy harvesting capability in indoor environments, small PV cells can be also an alternative for ultra-low-power (ULP) IoT devices, which can be duty-cycled to reduce energy consumption. Figure 1 depicts a battery-less photovoltaic energy harvesting system diagram. In this example, small PV cells are being used to harvest energy from artificial light and feed an ultra-low-power and ultra-low voltage (ULV) circuit application composed of a sensor - e.g. a temperature sensor - and a small memory processor. This application operates as follows: the system wakes for a short period of time sufficient for the memory processor to read and save the sensor value, then sleeps again for a greater period of time. This circuit can be used to monitor the temperature over time.

Figure 1 – Diagram of a battery-less photovoltaic energy harvesting system.



Source: Author

Additionally, some ULP circuits, such as low energy RF transceivers, can operate with ultra-low voltage (ULV) levels, around 0.4 V, close to the voltage range obtained by indoor small PV cells (Yu et al., 2017; Compassi-Severo; Van Noije, 2019). It is sufficient to supply, for example, a ULV circuit targeted to a Bluetooth Low Energy (BLE) application (Compassi-Severo; Van Noije, 2019). These characteristics require the use of high-efficiency DC-DC converters to perform the interface between the PV cell and the circuit. A small PV cell with 16 cm^2 can generate a few μW under artificial light, which is enough to power a small low-power transceiver during a period of time enough to generate a coded tone. Low-voltage circuits are particularly interesting applications of micro photovoltaic generation since the supply voltage is compatible with the voltage generated by small PV cells.

On the presented scope, this work focus on the use of solar energy harvesting as the main energy source to partially or completely replace the extensive battery usage in

electronic devices and IoT sensors.

In addition to the power source (ambient lighting) and transducers (PV cell), another important component on the energy harvesting system of Fig. 1 is the DC-DC converter. This circuit is responsible for adjusting the PV cell output to a voltage level which is compatible with the application circuit. In a different approach, using a battery to supply the application, the converter can also convert the PV cell voltage to a proper level for charging the device battery.

According to (WENS; STEYAERT, 2011), there are three fundamental DC-DC conversion methods. The first and simplest of all is the conversion through linear voltage converters using resistive dividers. In this case, only step-down conversions can be performed and the system efficiency is impaired because unused power is simply dissipated. The other two mentioned methods are approaches that can improve the converter efficiency through the use of inductors or capacitors in the circuit. Inductive types of converters utilize an LC tank to transfer energy from the input to the output. Capacitive types of converters use only capacitors to perform the same task (STEYAERT et al., 2011). The latter presents a great advantage for chip integration since capacitors are easier to integrate in conventional IC fabrication technologies than inductors (SANDERS et al., 2013). A very common capacitive type converter is the switched-capacitor (SC) - or charge pump (CP) - DC-DC converter, which uses only capacitors and switches to perform the voltage conversion.

Whereas a topology of an inductive type of converter can easily provide an adjustable voltage conversion ratio (VCR), a capacitive converter topology presents the disadvantage of providing a fixed VCR. A multiple-VCR DC-DC converter is necessary to dynamically adjust the conversion ratio for maintaining a constant output voltage even for variable generated input voltage, which is the case of light energy harvesting based on PV cells. Recalling the photovoltaic energy harvesting system from Fig. 1, the voltage generated by the PV cell may vary according to some factors such as illuminance level, the distance between the lamp and the PV cell, and shadings caused by human movements or furniture. To overcome this problem the DC-DC converter system must be able to reconfigure on-the-fly for adjusting the VCR to a required ratio, thus keeping the output voltage at a constant value (STEYAERT et al., 2011).

The main idea of this work is to propose a system able to provide a range of voltage conversion ratios through the combination of basic switched-capacitor converter topologies, such as the voltage doubler and the voltage divider. The greatest advantage of this approach is the design simplicity of the converter blocks, in which the same topology can be replicated several times to provide many voltage conversion ratios different from each other. In this work, a novel fully integrated multiple-VCR ULV SC DC-DC converter is proposed to be used with ULP devices powered by PV cells in indoor artificial light environments. It is composed of reconfigurable modules for dealing with multiple VCRs

while maintaining a fixed output voltage of 0.4 V. This voltage is compatible with either the operating voltage level of many ULV circuits used in IoT applications and the voltage provided by small PV cells at indoor.

A systematic simulation-based design method is presented for the converter, based on fast and slow operation mode analysis to find ideal switching frequency and capacitor values to improve conversion efficiency. Both switching frequency and capacitor values are considered to allow circuit operation at the ULV range. The circuit can be fully integrated using submicron low-cost CMOS fabrication processes.

1.1 OBJECTIVES

The present work has the main goal to propose and validate through electrical simulations a switched-capacitor DC-DC converter for indoor energy harvesting system supplied by photovoltaic cells using ambient lighting as an alternative power source in order to partially or completely replace battery usage of ULV and ULP applications. This energy harvesting system will be suitable for low power applications present in conventional rooms with lighting levels within the range required by the standard ISO 8995-1. Following this standard the illuminance in offices must range from 200 to 750 lux, depending on the task (CIE, 2002).

Within the main goal of this work, there are also specific goals: the proposal of a method for electric characterization of solar cells operating indoor; PV cells characterization to provide an insight about the electrical quantities and limitations of the panels operating only under artificial lighting; proposal of a switched capacitor converter topology able to offer a range of different voltage conversion ratios; electrical behavior simulation of the proposed topology to validate circuit operation; proposal of a systematic method to design the conversion system; circuit design and optimization aiming maximum efficiency; and post-layout simulation and validation of the conversion system.

1.2 ORGANIZATION OF THE WORK

The present work is organized as follows: Chapter 2 presents an overview of the DC-DC converters related works, showing different topologies, design approaches, and applications involving these converters. Chapter 3 deals with the basics about DC-DC converters focusing more on their modeling and behavior, in this chapter it is also discussed the strategy to obtain a converter with a range of VCRs using only basic switched-capacitor converter topologies, some electrical simulations are presented. In chapter 4 it is presented the proposed systematic simulation-based design method used to size flying capacitors, switches, and switching frequency of the proposed conversion system. Chapter 5 shows the main schematic simulation results of the proposed conversion system for two different designs and a comparison with other state-of-the-art related works. In

Chapter 6 it is presented some conclusions about the work done so far, and the tasks to be performed for future work. Finally, a method for PV cell characterization and some electrical characteristics curves of two small PV panels operating indoor are in Appendix A.

2 RELATED WORKS

This chapter presents a literature review about the works related to various applications of DC-DC converters, including employed topologies. First, an overview will be given on the main applications of DC-DC converters present in the literature. A greater focus will be given to applications involving energy harvesting, since they relate directly with the scope of this work. In addition, it will be discussed some state-of-the-art works related to topologies and approaches used to obtain many voltage conversion ratios using switched capacitor DC-DC converters.

2.1 INTEGRATED DC-DC CONVERTERS

DC-DC converters are widely used in different kinds of applications ranging from generating variable voltage supply for System-on-a-chip (SoC) to energy harvesting systems.

In this context, there are some different DC-DC converter topologies applied in a power management unit (PMU) that converts a voltage supplied by a battery into a desired fixed and smooth output voltage. It can also be used to provide multiple voltage domains for microprocessor and SoC designs and help to reduce power dissipation of the system. For these applications, Naidu and Kittur (2016) and Ghiasi et al. (2015) present different switched capacitor topologies but only to perform step-down conversions. Following the same step-down approach, the work of Manohar and Balsara (2015) presents a partially integrated buck DC-DC converter. Another approach is presented by Souvignet, Allard and Trochut (2016) in which a more versatile and fully integrated switched capacitor converter is used to provide step-down and step-up conversions.

Fully integrated switched capacitor DC-DC converters are well suited for supplying energy-constrained processors since they can achieve high efficiency within digital CMOS processes. In a near threshold application scope, fully integrated step-down switched capacitor DC-DC converters that deliver near-threshold output voltages are presented in the works of Turnquist et al. (2015) and Abdelfattah et al. (2015).

To extend the run time of a battery and micro-power medical applications, like medical implantable devices, there are two important scopes in which DC-DC converters can be employed. Therefore, Kim et al. (2016) presents a peak-current control noninverting buck–boost converter to extend the run time of a Ni–MH battery, and Miguez et al. (2016) introduces a micro-power inductive DC-DC step-down converter aimed to reduce the supply voltage in a medical implantable device.

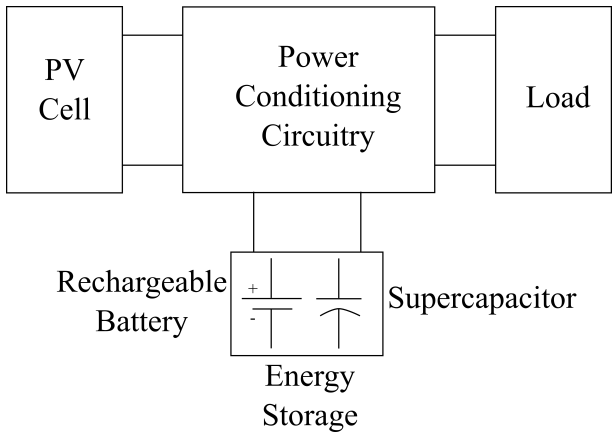
An energy harvester system is another way to include DC-DC converters, the main idea is to use a DC-DC converter to amplify or reduce the voltage harvested from ambient sources and apply it in other circuits or store it in a energy storage element. In the presented scope, Goeppert and Manoli (2016) designed an inductive DC-DC boost converter for energy harvesting using temperature gradients exploitable by thermoelectric

generators. The work of Chowdary, Singh and Chatterjee (2016) presents the application of a DC-DC buck-boost inductor type converter in a modular power management system that can harvest energy from three sources simultaneously, such as solar, vibration and RF. The work of Mondal and Paily (2016) introduces an efficient on-chip inductor-less switching power converter for solar energy harvesting. It proposes a tree-topology charge pump circuit in order to amplify the voltage obtained through the PV cell and transfer its energy to an energy buffer comprised of a supercapacitor or a rechargeable battery. Dini et al. (2015) uses a DC-DC buck-boost converter with an off-chip inductor as a fully autonomous power converter integrated circuit (IC) for energy harvesting of multiple and multi-type sources, such as piezoelectric, photovoltaic, thermoelectric, and RF transducers. A step-up switched capacitor has been included in an ultra-compact single-chip solar energy harvesting IC using parallel-connected photodiodes as on-chip solar cell for biomedical implant applications Chen et al. (2017). A batteryless solution is presented by Chen et al. (2018) using a DC-DC boost converter stepping-up architecture with a single off-chip inductor designed for thermoelectric energy harvesting application.

Considering an energy harvesting more specific scope, such as the scavenging of the energy provided mainly by artificial lighting through small photovoltaic panels, the paper of Nasiri, Zabalawi and Mandic (2009) shows different power conversion circuit topologies, such as topologies composed of supercapacitors, rechargeable and nonrechargeable batteries. These circuits have the configuration presented in Fig. 2, and are designed for indoor energy harvesting using PV cells for low-power indoor devices like remote sensors, supervisory and alarm systems, distributed controls, and data transfer system. A Single Inductor Dual-Input Dual-Output (SI-DIDO) topology is proposed by Meng et al. (2016) which presents a battery in its structure in order to supply the load together with a PV cell when the indoor environment is under-illuminated. A low-power-consumption boost converter with maximum power point tracking algorithm for indoor photovoltaic energy harvesting is proposed and by Tsai, Wu and Wei (2017), this system is designed to transfer energy from a PV cell to a supercapacitor used as energy storage element. Finally, the work of Mondal and Paily (2017) presents a complete on-chip single stage tree-topology switched capacitor based power converter with a fixed voltage conversion ratio around 2.5 for an indoor PV harvester.

Regarding the methods for obtaining a converter system capable of providing a range of many different voltage conversion ratios, a fine-grained conversion ratio resolution of $V_{in}/2^N$, where V_{in} is the input voltage and N is the number of stages, is obtained by Bang, Blaauw and Sylvester (2016) through a successive-approximation SC (SAR SC) DC–DC converter in which multiple stages of 2:1 SC converters are cascaded. A different approach is used in Wu et al. (2017) in which a moving-sum charge pump structure is presented. This structure consists of a reduced Dickson charge pump to produce two to nine times V_{in}, a voltage mux to select four voltages from two to nine times according to

Figure 2 – Configuration of the indoor energy harvesting system using PV cell.



Source: Adapted from (NASIRI; ZABALAWI; MANDIC, 2009)

the conversion ratio, and a summing series parallel stage where the selected voltages on the flying capacitors are placed in series and summed to charge the output node capacitor. Liu et al. (2016) presents an adjustable SC converter built by cascading three doublers switched-capacitor converters and properly selecting their input connections through a two-way demultiplexer and four-way demultiplexer, integral CRs as 1, 2, up to 8 can be obtained. There are also fractional conversion ratios (CRs) which are realized by a reconfigurable step-down charge pump with CRs as $\frac{1}{3}$ and $\frac{2}{3}$. Its output is included in the four-way demultiplexer and results in mixed CRs as $1\frac{1}{3}$, $1\frac{2}{3}$, up to 8. This SC converter is applied in a hybrid system that can harvest energy from photovoltaic and thermoelectric generator transducers. The work of Jung et al. (2014) proposes a fully integrated energy harvester that maintains at least 35% end-to-end efficiency when harvesting from a 0.84 mm^2 solar cell in low light condition of 260 lux. The voltage conversion in this harvesting system is performed by a self-oscillating switched-capacitor in which DC-DC voltage doublers are cascaded to form a complete harvester, with configurable overall conversion ratio from 9 to 23. A more sophisticated and complex technique is used by Jiang et al. (2018) where an algorithmic voltage-feed-in (AVFI) topology is introduced in order to systematically generate any arbitrary buck–boost rational ratio with optimal conduction loss while achieving reduced topology-level parasitic loss. The presented fully integrated switched-capacitor power converter executes a total of 24 VCRs (11 buck and 13 boost) with wide-range efficient buck–boost operations.

Table 2 contains the main DC-DC converters mentioned above separated in terms of application at indoor solar harvesters or VCR adjustable converters. The converters presented by Bang, Blaauw and Sylvester (2016) and Wu et al. (2017) have the largest number of available VCRs, 117 and 126, respectively. Even with a large number of available VCRs, both converters focus on just one type of conversion step-down or step-up. This

Table 2 – State-of-the-art adjustable or indoor light SC based converters.

	(JUNG et al., 2014)	(BANG et al., 2016)	(LIU et al., 2016)	(MONDAL et al., 2017)	(WU et al., 2017)	(JIANG et al., 2018)
Converter Topology:	Cascaded 1:2 SC	Cascaded 2:1 SC	Combination of SC	Capacitive boost	Dickson SC	Algorithmic voltage-feed-in SC
Converter Type:	Step-up	Step-down	Step-up	Step-up	Step-up	Step-down and step-up
Implementation Complexity:	Low	Low	Medium	Low	Medium	High
Number of VCRs:	15	117	14	1	126	24
Input Voltage:	0.14 - 0.5 V	3.4 - 4.3 V	0.45 - 3 V	0.39 - 0.43 V	0.25 - 0.65 V	0.22 - 2.4 V
Output Voltage:	2.2 - 5.2 V	>0.45 V	3.3 V	1 V	3.8 - 4 V	0.85 - 1.2 V
Energy Harvesting Source:	Indoor light	N/A	Indoor light and thermoelectric	Indoor light	Indoor light	N/A

Source: Author

is also the case of the works from Jung et al. (2014), Liu et al. (2016) and Mondal and Paily (2017). The converter presented by Jiang et al. (2018) is more versatile, being able to perform both step-down and step-up conversions with a wide range of VCRs. On the other hand, the implementation complexity of this converter is quite high. The majority of the works which present converters with a goof number of available VCRs implement the conversion system by cascading or combining one or more SC converter topologies. This technique is versatile and the implementation complexity is low or medium depending on the overall conversion system structure.

2.2 CONCLUSION

In this chapter, it is presented a literature review about the works related to the main applications of DC-DC converters and the different topologies presented. A major focus is given for DC-DC converters applied on the energy harvesting scope. There are several alternative energy sources used in the harvesting system, as well as many circuit approaches to perform voltage conversions. The majority of the discussed papers presented a rechargeable battery or other energy storage element in order to store the energy provided by the alternative source and to assist in the energy supply for the load. This chapter also presents the main techniques and topologies for providing a converter system with many different voltage conversion ratios.

3 PROPOSED SWITCHED CAPACITOR CONVERTER TOPOLOGY

This chapter presents a simplified model to understand the operation of different switched-capacitor converter topologies. A detailed explanation of the approach used to obtain an SC based topology capable of providing a range of different voltage conversion ratios is given. In addition, this chapter shows electrical simulations of the proposed SC topology in order to validate its operation. Finally, the construction details of the proposed digital control system is presented.

3.1 CHARGE FLOW ANALYSIS WITH SSL IMPEDANCE

All DC-DC converter topologies have their own ideal voltage conversion ratio (iVCR), and it represents the maximum ratio between the output voltage and the input voltage of the power converter. This iVCR is the upper bound for the actual voltage conversion ratio (VCR) and the topology only operates at a theoretical 100% efficiency when the iVCR is reached. For a converter with an input voltage V_{in}, an output voltage V_{out} and a common ground connection, the VCR is defined by (BREUSSEGEM; STEYAERT, 2012):

$$VCR = \frac{V_{out}}{V_{in}} \tag{3.1}$$

A useful tool for identifying the role of the different components in the conversion block is the charge flow analysis. This analysis can be combined with the slow-switching limit (SSL) impedance, which neglects the finite resistances of the switches, capacitors, and interconnects, in order to extract the charge flow vectors a_c^j. These vectors play an important role in the conversion block modeling and can be derived for any standard non-degenerate two-phase SC converter (BREUSSEGEM; STEYAERT, 2012).

Charge flow vectors represent the charge flows that occur immediately after the closing of the switches in each respective phase of the SC circuit. A charge flow vector is composed of elements that represent a specific capacitor or independent voltage source in the circuit, and they show the charge flow into that component, normalized with respect to the output charge flow.

The charge flow vector is described generically by:

$$\vec{v_c}^{(j)} = [q_{out}^{(j)}\ q_i^{(j)}\ ...\ q_n^{(j)}\ q_{in}^{(j)}]^T / q_{out} \tag{3.2}$$

where n is the number of flying capacitors, $q_i^{(j)}$ represents the amount of charge transferred during state or phase j by capacitor i, q_{in} refers to the input charge transferred to the system, and q_{out} is the total amount of charge transferred to the load during a switching period T.

The elements of the charge flow vector can be derived by inspection for every state of the conversion period following the principles described below: Kirchhoff's current

law in each node, which means the sum of charge flow elements must be equal to zero in each circuit node. For every flying capacitor, the sum of both state's charge flow elements is equal to zero. The output capacitor C_{out} behaves as a voltage source with respect to the remainder of the circuit. Also, the charge vector elements of both states of the flying capacitors have opposite signs, and the charge vector elements of the output sum to 1. Furthermore, the total output charge is the sum of the output charges in each phase, $q_{out}^{(1)} + q_{out}^{(2)} = q_{out}$ and the total input charge is the sum of the input charges in each phase, $q_{in}^{(1)} + q_{in}^{(2)} = q_{in}$.

The output power is equal to the input power ($P_{out} = P_{in}$) in steady-state for an ideal converter. Also, if we integrate over a switching cycle, the output energy is equal to the input energy ($E_{out} = E_{in}$). Considering the capacitor potential energy $E = qV$, the input and output energy can be described as:

$$q_{out}V_{out} = q_{in}V_{in} \tag{3.3}$$

Rearranging Eq. 3.3, the ratio of the total input and output charge flow vector elements represents the iVCR (N) of the topology:

$$N = \frac{q_{in}}{q_{out}} \tag{3.4}$$

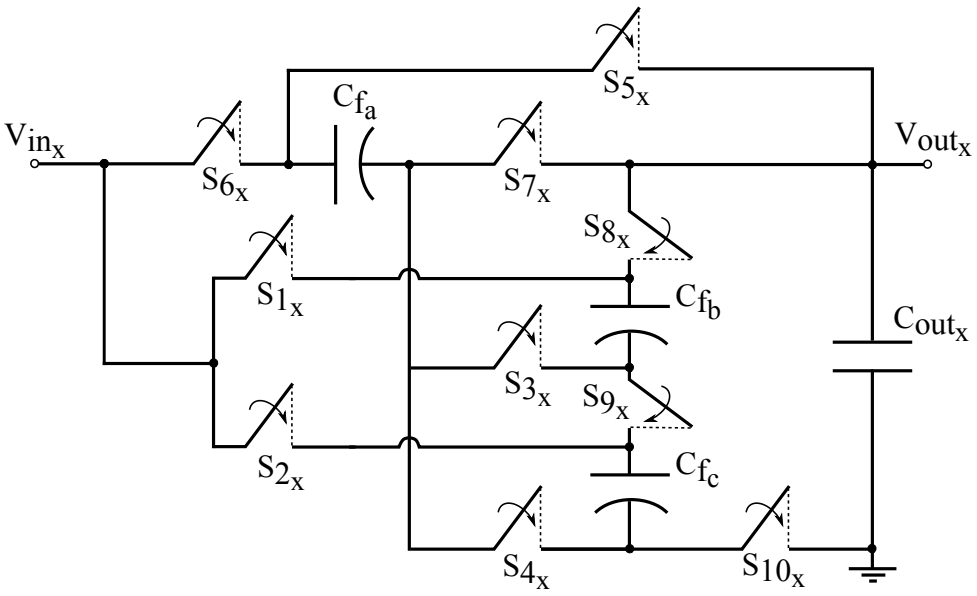
Converters with fractional VCRs are required in certain applications to keep up a fixed or constant output voltage at a given value even if the solar cell suffers variations like load variation, variation in its polarization, illuminance levels, etc.

A straightforward way to implement a switched-capacitor DC-DC converter with fractional VCR is the fractional converter (MAKOWSKI; MAKSIMOVIC, 1995). An example of a fractional 4/5 switched-capacitor DC-DC converter is shown in Fig. 3. This topology has ten switches S_{1_x}, S_{2_x}, S_{3_x}, S_{4_x}, S_{5_x}, S_{6_x}, S_{7_x}, S_{8_x}, S_{9_x}, S_{10_x}, three flying capacitors C_{f_a}, C_{f_b} and C_{f_c}, and an output buffer capacitor C_{out_x}. All capacitors have the same value.

This fractional converter has two phases of operation. In the first operation phase S_{1_x}, S_{2_x}, S_{3_x}, S_{4_x} and S_{5_x} switches are on and the other ones off. The opposite occurs in the second operation phase. Fig. 4 shows the electrical diagrams for the fractional converter operation phases.

In addition, the charge flow vectors can be derived for each operation phase. Recalling the step of the charge flow analysis which the sum of both state's charge flow elements is equal to zero for every flying capacitor. Based on this, the vector signal and the direction of the charge flow can be arbitrarily defined. In this work, we choose to represent the vector element with a minus signal when the charge is flowing into the capacitor, and the arrow representation in the diagram is going from the positive to the negative terminal of the capacitor. In the other case when the charge is coming out of the capacitor, the

Figure 3 – Fractional converter electrical circuit.



Source: Author

vector element is positive and the arrow representation in the diagram is going from the negative to the positive terminal of the capacitor.

For the first operation phase:

$$\vec{v_{frac}}^{(1)} = [q_{out_x}^{(1)} \quad q_{C_{f_a}}^{(1)} \quad q_{C_{f_b}}^{(1)} \quad q_{C_{f_c}}^{(1)} \quad q_{in_x}^{(1)}] = [\frac{1}{5} \quad \frac{1}{5} \quad \frac{1}{5} \quad \frac{-2}{5} \quad \frac{2}{5}] \tag{3.5}$$

For the second operation phase:

$$\vec{v_{frac}}^{(2)} = [q_{out_x}^{(2)} \quad q_{C_{f_a}}^{(2)} \quad q_{C_{f_b}}^{(2)} \quad q_{C_{f_c}}^{(2)} \quad q_{in_x}^{(2)}] = [\frac{4}{5} \quad \frac{-1}{5} \quad \frac{-1}{5} \quad \frac{2}{5} \quad \frac{2}{5}] \tag{3.6}$$

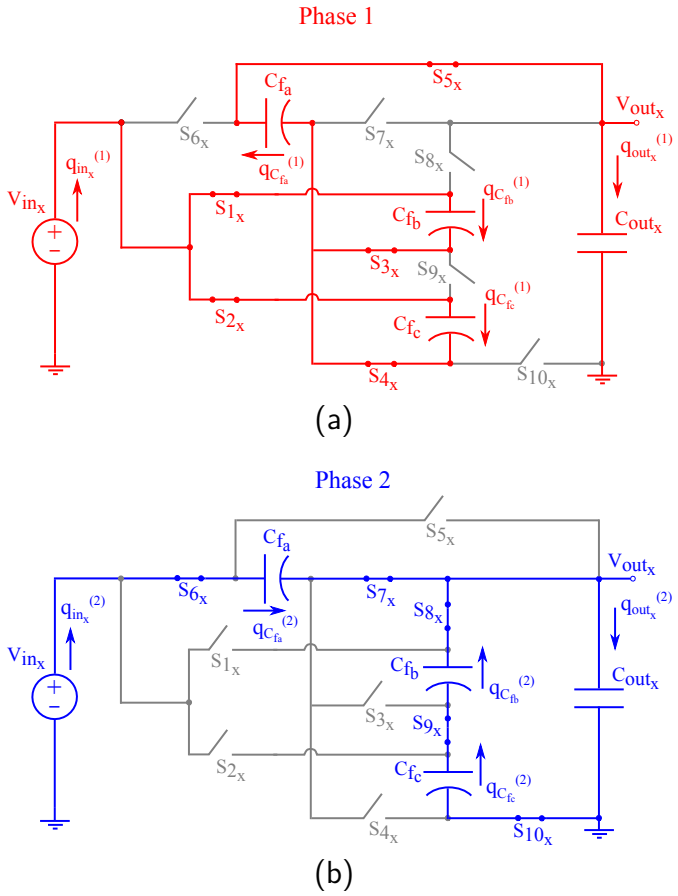
The VCR can be obtained for this fractional DC-DC converter:

$$VCR = \frac{q_{in}}{q_{out}} = \frac{\frac{2}{5} + \frac{2}{5}}{\frac{1}{5} + \frac{4}{5}} = \frac{4}{5} \tag{3.7}$$

According to the Topology Occurrence Theorem (MAKOWSKI; MAKSIMOVIC, 1995), which predicts the achievable iVCR given a certain number of flying capacitors, if the number of flying capacitors in the converter topology is limited to three, there are many conversion ratios that can be achieved as shown in Table 3.

There are some drawbacks in implementing a fractional SC DC-DC converter. The iVCR of a fractional converter is hard to be determined by visual inspection and its synthesis is non-methodological, that is, there is no sequence of steps to analyze and find the iVCR topology (BREUSSEGEM; STEYAERT, 2012). Also, the increase in the number of flying capacitors in the converter circuit results in an increase in its output impedance. If the application requires more than one fractional VCR, it will also be necessary to

Figure 4 – Fractional 4/5 switched capacitor DC-DC converter operation: phase 1 (a) and phase 2 (b).



Source: Author

Table 3 – Options of iVCR related to the number of flying capacitors.

n flying capacitors	iVCR
1	1/2, 1, 2
2	1/3, 1/2, 2/3, 3/2, 1, 2, 3
3	1/5, 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 1, 5/4, 4/3, 3/2, 5/3, 2, 5/2, 3, 4, 5

Source: From (BREUSSEGEM; STEYAERT, 2012)

implement another fractional converter topology to be cascaded. The implementation of several cascaded topologies of fractional converters is impracticable to the project due to its high complexity.

3.2 MULTI-TOPOLOGY CONVERTERS

Sometimes more than one VCR, fractional or integer, is required and a single topology is not suitable in this case. According to Breussegem and Steyaert (2012) topology

and iVCR are directly dependent, and this put constraints on the input-output voltage range of the converter and the associated converter's performance within this range. Multi-topology capacitive converters are a good alternative to increase the converter efficiency over a broad range of conversion scenarios.

Multi-topology converters have a capacitor-switch array that is capable of switching between both states or phases of the base topology and switching between different topologies. Each one of these topologies is adequate for a given conversion scenario and input-output range.

As mentioned at the beginning of this chapter, a specific converter topology has an upper bound for which conversion can be performed, the iVCR. Also, the efficiency has an upper bound that corresponds to the ratio of the actual VCR and the iVCR:

$$\begin{aligned} VCR &\leq iVCR \\ \eta &= \frac{VCR}{iVCR} \end{aligned} \tag{3.8}$$

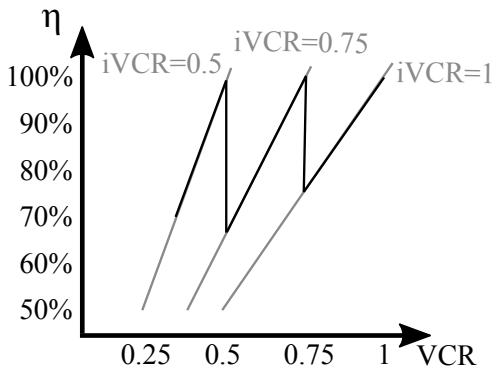
A single converter topology designed to operate at a certain conversion rate must have its efficiency worsened if the circuit input or output voltage values change causing it to work with a conversion ratio different from its iVCR. In that case, the efficiency of a capacitive converter can be improved with the use of a multi-topology converter. As an example, Fig. 5 illustrates an efficiency graph in which a hypothetical converter is implemented with three multiple topologies. In this graph, the gray line represents the ideal efficiency ratings of three topologies (iVCR= 1, 3/4, and 1/2). In a separate configuration, each topology is designed to have a maximum VCR corresponding to the iVCR. In this case, each topology demonstrates a low efficiency η if the VCR deviates significantly from iVCR. On the other hand, combining multiple topologies in a single structure can boost efficiency as depicted in a thick dark line of the graph. In this situation, the converter has three ideal VCRs and can maintain its maximum efficiency when the required VCR changes for a value equal to one of the converter iVCRs.

3.3 DOUBLER/DIVIDER MODULE

A basic multi-topology converter is presented in this work. It comprises a voltage doubler and a voltage divider integrated in a single topology. So, with this basic multi-topology converter is possible to double the input voltage or divide it by two and present it at the converter output. The electrical diagram of the proposed multi-topology converter is presented in Fig. 6, it comprises of a single flying capacitor C_{fly_1}, a single output buffer capacitor C_{out_1} and six switches S_1, S_2, S_3, S_4, S_5 and S_6. The output capacitor C_{out_1} has the same value of C_{fly_1}.

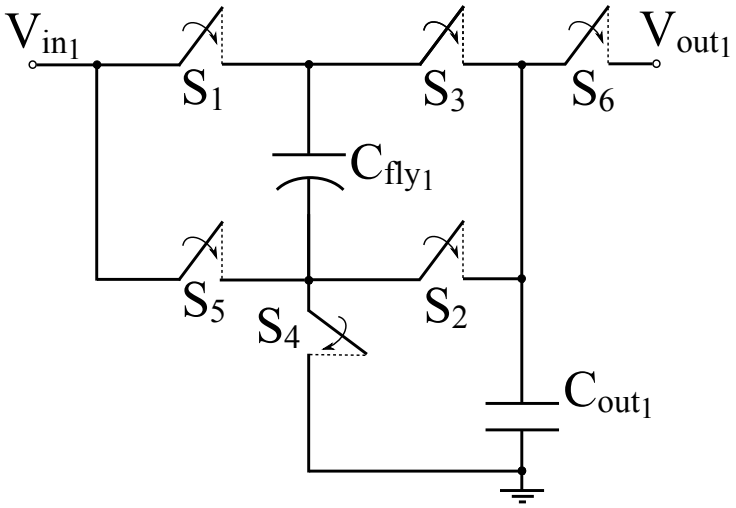
The multi-topology converter can change between two topologies with different iVCRs. Each topology has a combination of switches that must be turned on and off in

Figure 5 – Graphical representation of the potential efficiency improvement by using the multi-topology approach.



Source: Adapted from (BREUSSEGEM; STEYAERT, 2012)

Figure 6 – Proposed basic multi-topology converter electrical circuit.



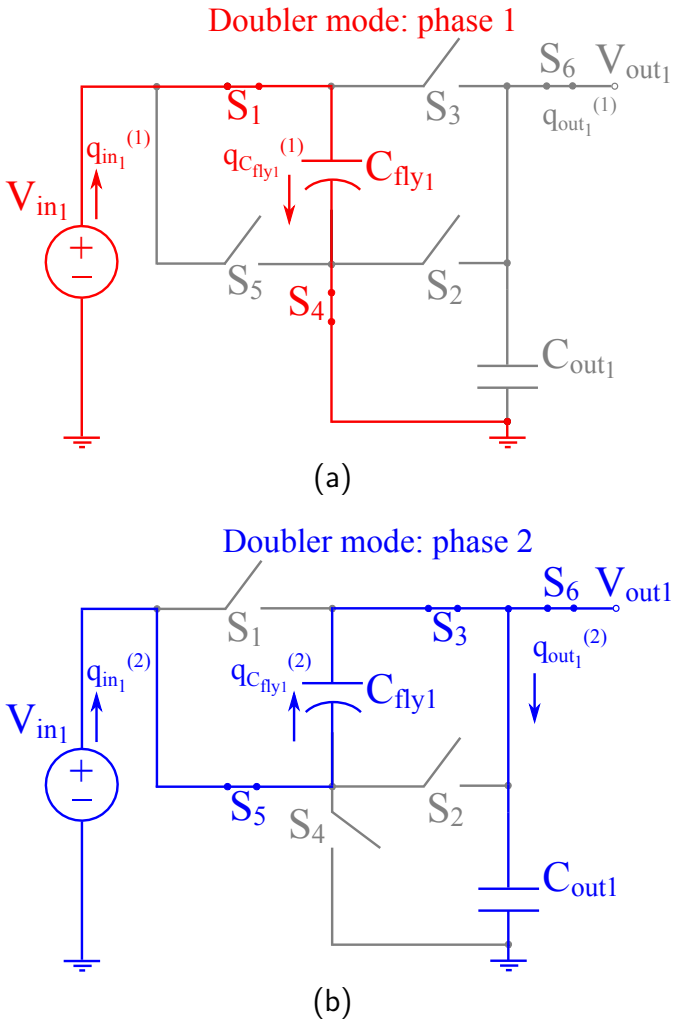
Source: Author

order to get a certain iVCR.

For the multi-topology converter to work like a Voltage Doubler, switch S_2 is always off and switch S_6 is always on. So, this resulting topology has two working phases as illustrated in Fig. 7. In phase 1, switches S_1 and S_4 are on and switches S_3 and S_5 are off. In this phase, C_{fly_1} capacitor is charging with input voltage provided by V_{in_1}. During phase 2, the switches are configured in an opposite way of phase 1. In phase 2, C_{fly_1} is already charged with V_{in_1} and this input voltage is connected in a way that the output node is twice V_{in_1} when C_{out_1} is fully charged.

The following charge flow vectors are derived for a single-stage voltage doubler

Figure 7 – Phase 1 (a) and phase 2 (b) of the multi-topology converter operating as a voltage doubler.



Source: Author

for first and second operation phases, respectively:

$$\vec{v_{dou}}^{(1)} = [q_{out1}^{(1)} \quad q_{C_{fly1}}^{(1)} \quad q_{in1}^{(1)}] = [0 \quad -1 \quad 1] \tag{3.9}$$

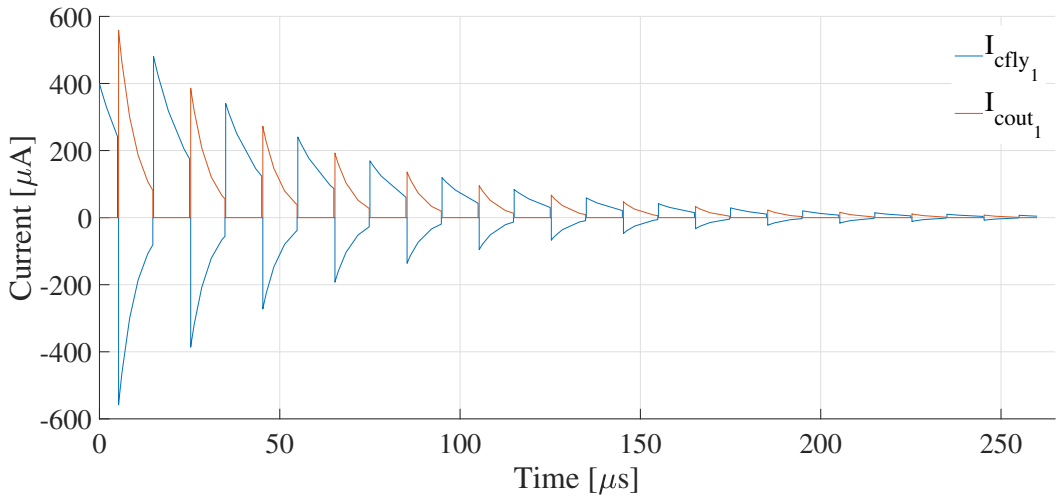
$$\vec{v_{dou}}^{(2)} = [q_{out1}^{(2)} \quad q_{C_{fly1}}^{(2)} \quad q_{in1}^{(2)}] = [1 \quad 1 \quad 1] \tag{3.10}$$

The VCR can be obtained for this voltage doubler DC-DC converter as:

$$VCR = \frac{q_{in1}}{q_{out1}} = \frac{1+1}{0+1} = 2 \tag{3.11}$$

The electrical simulation of this configuration was performed to better explain the topology behavior. All electrical simulations that will be presented from now on in this chapter were executed using ideal switches to validate the topologies operation and all topologies capacitors were set with 10 nF.

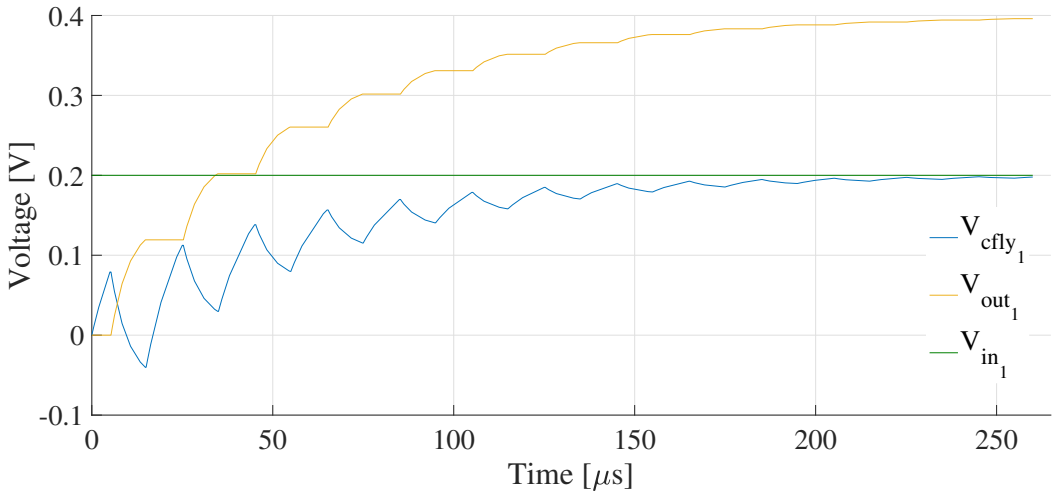
Figure 8 – Doubler converter currents.



Source: Author

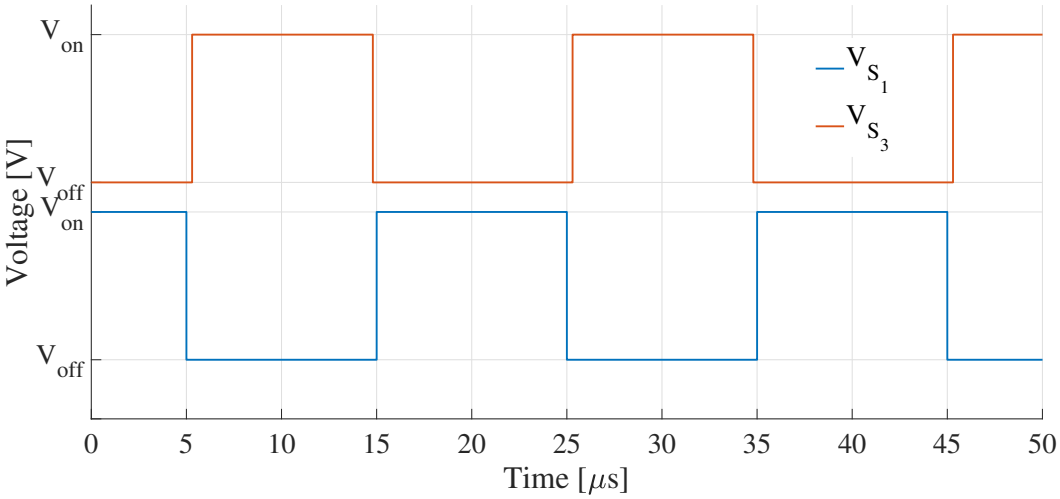
A voltage of 0.2 V with a small series resistance of 100 Ω was used as input. Fig. 8 shows C_{out_1} and C_{fly_1} currents over the simulation period. It can be observed that the currents have high peaks in the first transient cycles and they tend to zero in steady-state when the capacitors are fully charged. Fig. 9 shows the capacitors voltages as well as the input and output voltages. The output and C_{out_1} voltages are equal and their curves are overlapped. In this figure, it can be observed that C_{fly_1} capacitor charges over the cycles, and when its voltage reaches 0.2 V the converter output presents twice the input voltage. Fig. 10 shows switches operating cycles. When S_1 is on S_3 if off, and vice versa. There is a small delay in the moment that a switch turns off and the other turns on. This prevents the signals overlapping which may cause undesired operation in the circuit.

Figure 9 – Doubler converter voltages.



Source: Author

Figure 10 – Doubler converter switches signals.



Source: Author

For the multi-topology converter to work like a Voltage Divider, switch S_5 is always off during both operation phases. Then, the resulting topology also has two working phases illustrated in Fig. 11. Phase 1 is set when switches S_1 and S_2 are on and S_3 and S_4 are off. In this scenario, C_{fly_1} and C_{out_1} are in series being charged with $V_{in_1}/2$ each. In phase 2, the switches are also configured in the opposite way of phase 1. Here, both capacitors are already charged and connected in parallel, resulting in a V_{out_1} with half of the input voltage.

The charge flow vectors which represent the voltage divider in operation phases 1 and 2 are presented below:

$$\vec{v_{div}}^{(1)} = [q_{out_1}^{(1)} \quad q_{C_{fly_1}}^{(1)} \quad q_{in_1}^{(1)}] = [\frac{1}{2} \quad \frac{-1}{2} \quad \frac{1}{2}] \tag{3.12}$$

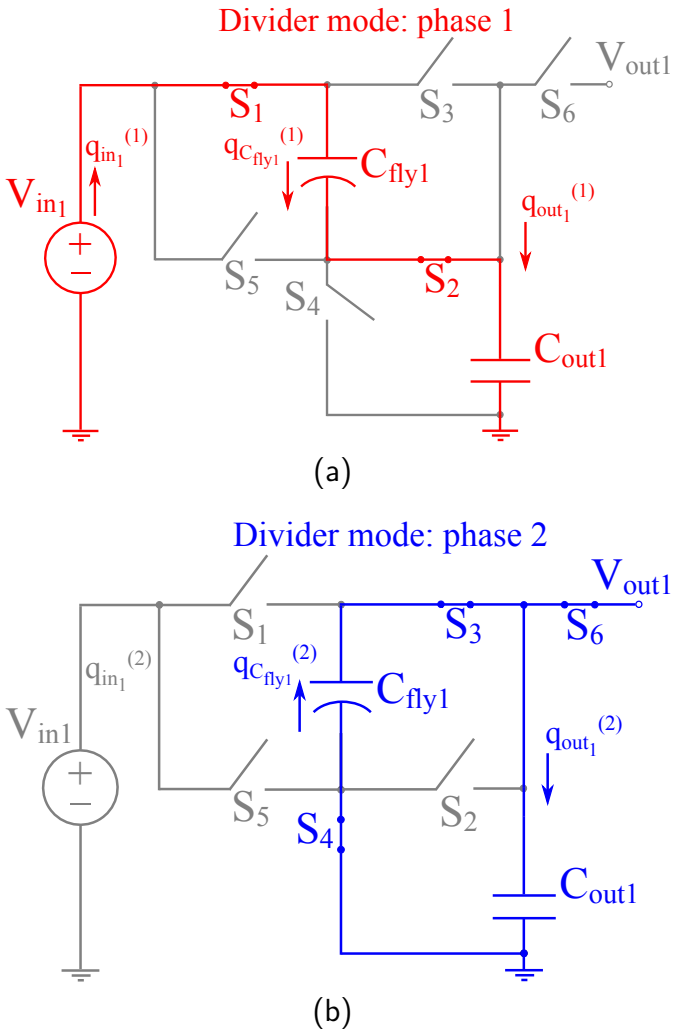
$$\vec{v_{div}}^{(2)} = [q_{out_1}^{(2)} \quad q_{C_{fly_1}}^{(2)} \quad q_{in_1}^{(2)}] = [\frac{1}{2} \quad \frac{1}{2} \quad 0] \tag{3.13}$$

The conversion ratio is then obtained as:

$$VCR = \frac{q_{in1}}{q_{out1}} = \frac{\frac{1}{2} + 0}{\frac{1}{2} + \frac{1}{2}} = \frac{1}{2} \tag{3.14}$$

The electrical simulation of this configuration was performed in order to evaluate the topology behavior. For the voltage divider simulation, an input voltage of 0.8 V was applied for a 100 Ω series resistance. The capacitors currents are equal in this topology, so just C_{fly_1} is represented in Fig. 12. Once again, it can be noted that there is a high peak current on the transient period denoting capacitors charging, and the currents tend to zero when the capacitors are already charged. Fig. 13 shows the topology voltages. As the currents, capacitor voltages are also equal with output voltage equal to them. The output

Figure 11 – Phase 1 (a) and phase 2 (b) of the multi-topology converter operating as a voltage divider.



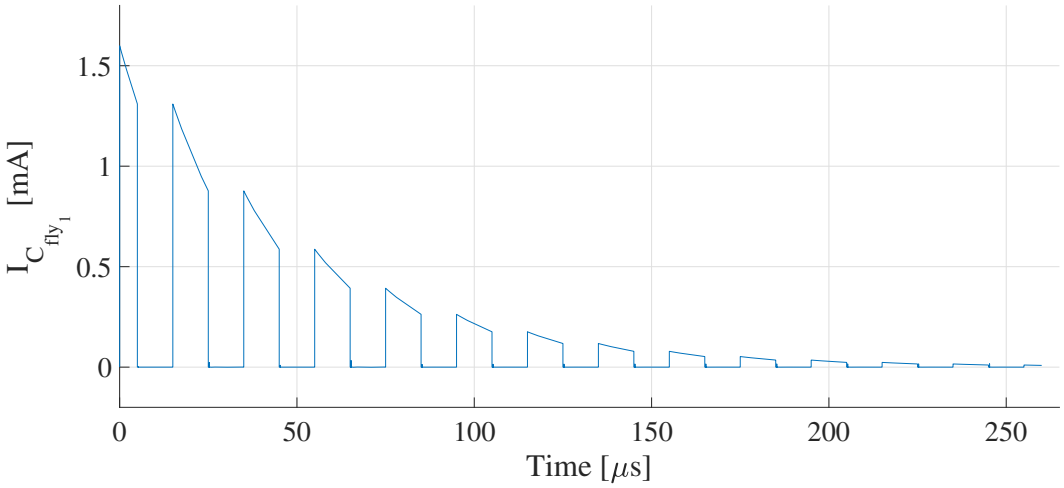
Source: Author

node increases over time and only reaches half of V_{in_1} when there is no high current peak on the capacitors. The switches signals are the same as the ones presented in Fig. 10.

3.4 ADDER/SUBTRACTOR MODULE

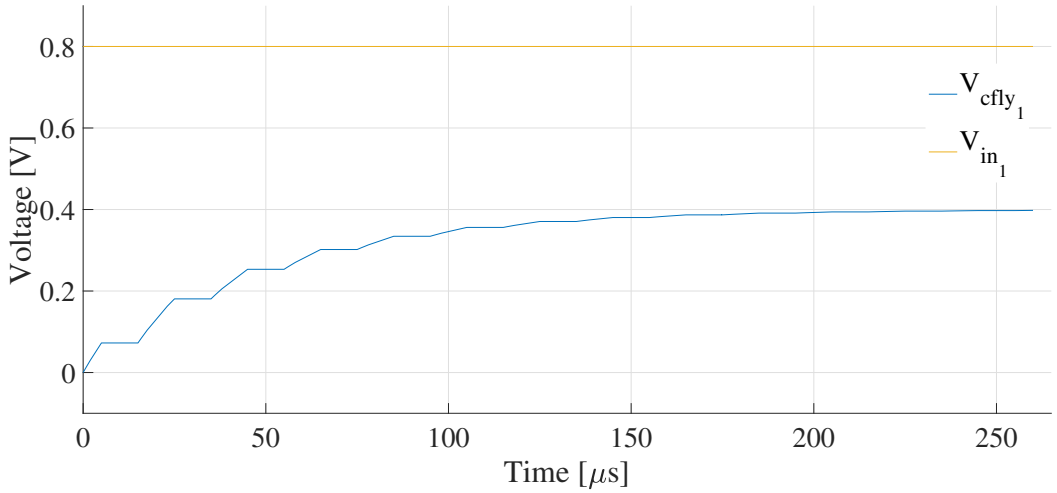
The idea is to create a system using the previously presented basic multi-topology converter as the main conversion block which is possible to get a range of fractional and integer VCRs. The Doubler/Divider multi-topology converter output voltage can be modeled as a power of two 2^n, wherein a single module n can assume -1 or 1. When $n = -1$ the topology behaves as a Voltage Divider and $n = 1$ configures the module as a Voltage Doubler. The power of two conversion characteristic can be expanded by cascading the multi-topology converter. This is done by connecting the output of the first converter to the input of the second converter. For example, two single doubler modules in

Figure 12 – Voltage divider currents.



Source: Author

Figure 13 – Voltage divider voltages.



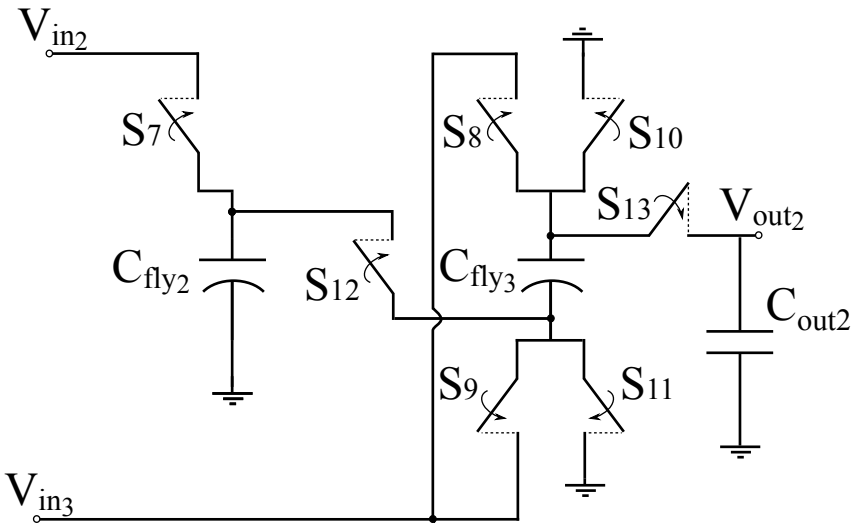
Source: Author

sequence (forming a block), with $n = 1$ represents a 2^2 conversion, and the output voltage will be four times the input voltage. This kind of approach only provides VCRs related to a power of two characteristic, so, in order to obtain intermediate VCRs, a two-input Adder/Subtractor was also proposed. Thereby two, equal or different, input voltages can be added or subtracted and with that, it is possible to combine two VCRs obtained from the multi-topology converter resulting in an intermediate voltage conversion ratio.

The electrical diagram of the proposed Adder/Subtractor converter is depicted in Fig. 14. It has seven switches S_7, S_8, S_9, S_{10}, S_{11}, S_{12}, S_{13}, two flying capacitors C_{fly_2}, C_{fly_3}, and C_{out_2} represents the output load capacitor. Depending on the switches arrangement,

this module can work as a two input adder or subtractor circuit. So the output voltage is equal to the addition or subtraction of both independent input voltages V_{in_2} and V_{in_3}.

Figure 14 – Adder-subtractor converter electrical circuit



Source: Author

Similarly to the Divider/Doubler module, the Adder/Subtractor also operates in two phases. For the topology to work as a two-input adder, the first phase positively charges the flying capacitors with the voltages presented in its inputs, then switches S_7, S_8, and S_{11} are turned on and the other ones are turned off. In the second phase, both charged capacitors are connected in series and the energy is released to the output node. In this case, S_{12} and S_{13} are on and the remaining are off. Fig. 15 shows the electrical diagrams of the two described working phases.

The charge flow analysis can also be used to derive the voltage conversion ratio of this conversion module. So, the following charge flow vectors are obtained for the voltage adder:

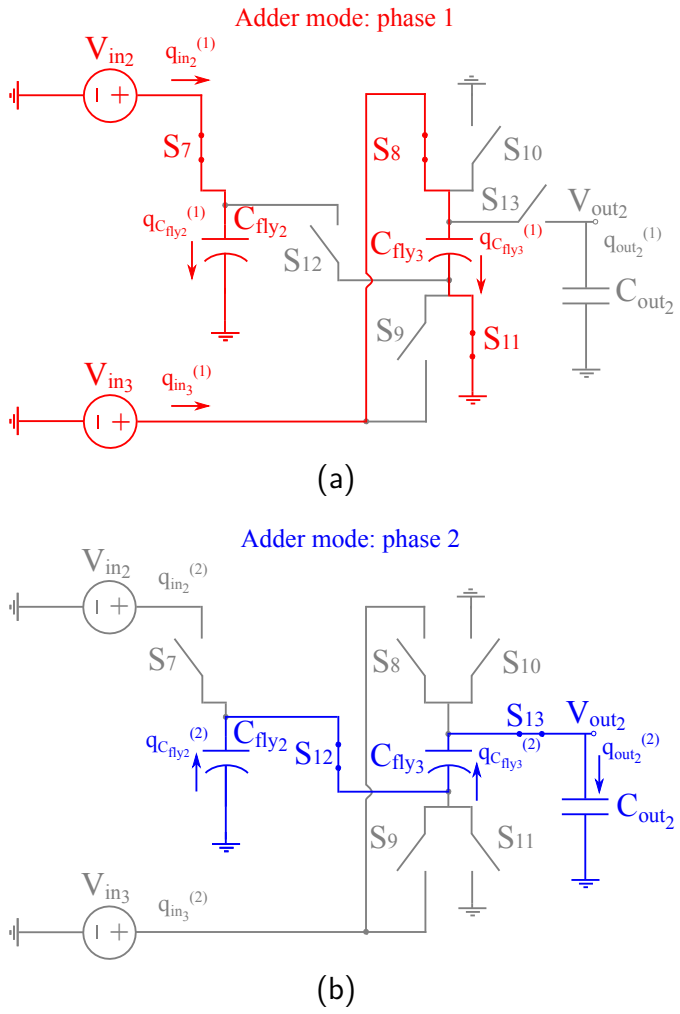
$$\begin{aligned} \vec{v_{add}}^{(1)} &= [q_{out_2}^{(1)} \quad q_{C_{fly_2}}^{(1)} \quad q_{C_{fly_3}}^{(1)} \quad q_{in_2}^{(1)} \quad q_{in_3}^{(1)}] \\ &= [0 \quad -1 \quad -1 \quad q_{in_2} \quad q_{in_3}] \end{aligned} \tag{3.15}$$

$$\begin{aligned} \vec{v_{add}}^{(2)} &= [q_{out_2}^{(2)} \quad q_{C_{fly_2}}^{(2)} \quad q_{C_{fly_3}}^{(2)} \quad q_{in_2}^{(2)} \quad q_{in_3}^{(2)}] \\ &= [1 \quad 1 \quad 1 \quad 0 \quad 0] \end{aligned} \tag{3.16}$$

The VCR can be obtained summing $\vec{v_{add}}^{(1)}$ and $\vec{v_{add}}^{(2)}$:

$$VCR = \frac{q_{in}}{q_{out_2}} = \frac{q_{in_2} + q_{in_3} + 0 + 0}{1 + 0} = q_{in_2} + q_{in_3} \tag{3.17}$$

Figure 15 – Operation phase 1 (a) and phase 2 (b) of the Adder/Subtractor converter working as voltage adder.

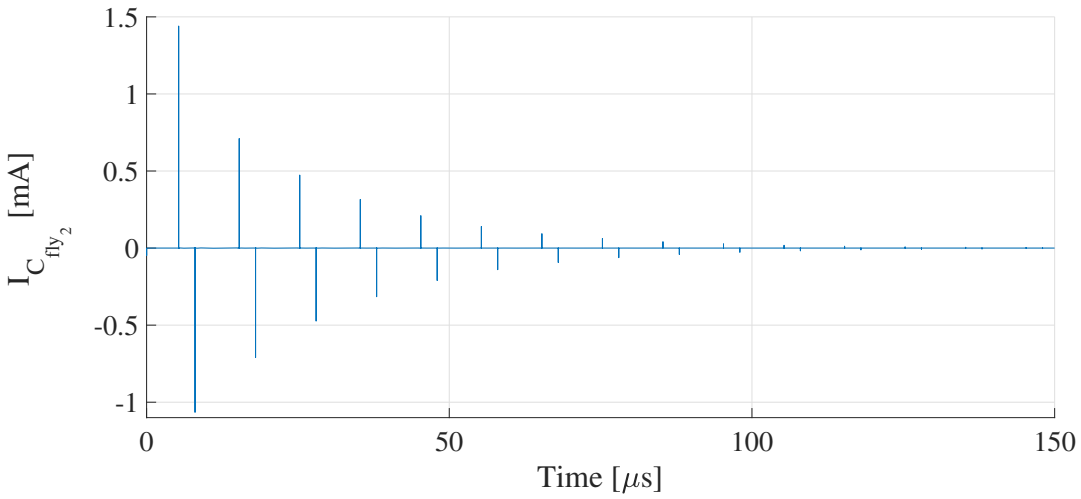


Source: Author

An electrical simulation was performed using 0.1 V and 0.3 V as voltages inputs with no series resistance because in practice this module will be connected to the output of the previous module. In this case, currents for the two flying capacitors, C_{fly_2} and C_{fly_3}, are the same and C_{fly_2} current is represented in the graph of Fig. 16. It can be noted that the current presents high peaks of very short duration when the capacitors are charging in the first cycles. This peak decreases over time and the current reaches zero when capacitors are charged. Fig. 17 presents the voltages of the two inputs, flying capacitors, and the circuit output. C_{fly_2} is charging with the 0.3 V voltage provided by V_{in_2} and C_{fly_3} is charging with the 0.1 V voltage provided by V_{in_3}. The output voltage is the sum of the charges in C_{fly_2} and C_{fly_3}, but this sum is only validated when the capacitors end the transitory phase and start the steady-state, which happens after some simulations cycles. Fig. 18 shows the clock signals of switches S_7 and S_{13}. S_7 is also representing S_8 and S_{11}, and S_{13} is also representing S_{12} . As shown in the multi-topology converter simulations,

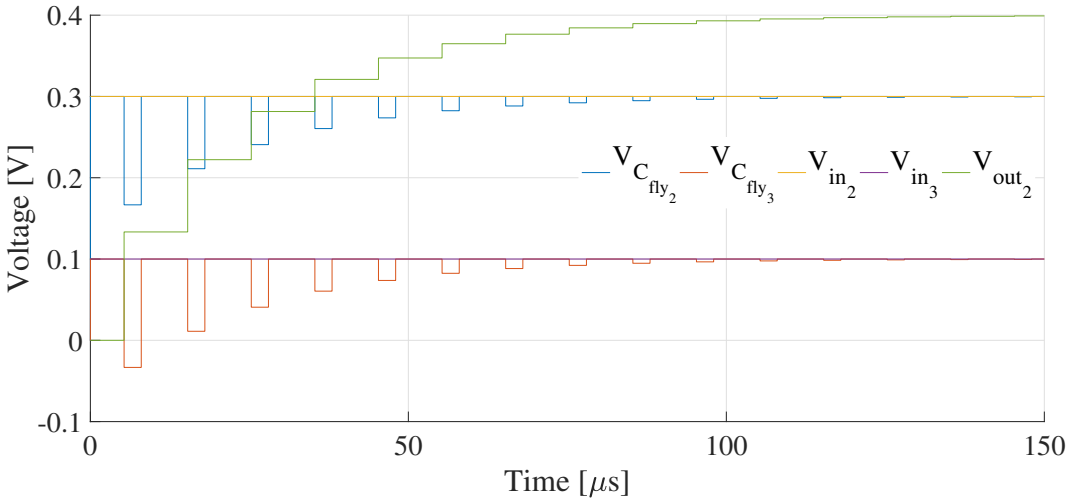
the switches have a small delay in the transition from on to off and vice-versa.

Figure 16 – Current of the converter adder mode.



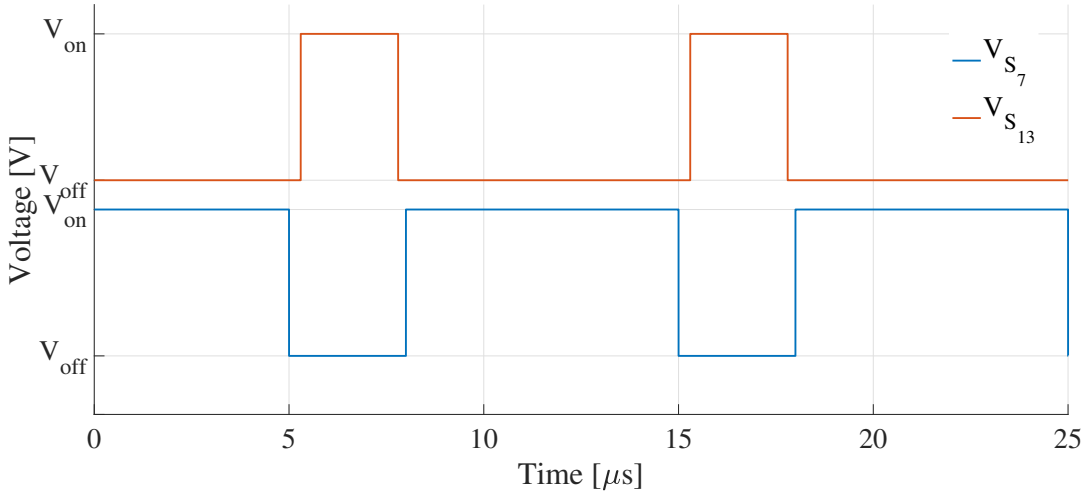
Source: Author

Figure 17 – Voltages of the converter adder mode.



Source: Author

Figure 18 – Switches signals of the converter adder mode.



Source: Author

The subtractor circuit mode is very similar to the adder mode and it also has two phases of operation. In the first phase, capacitor C_{fly_2} is positively charged, and C_{fly_3} is negatively charged. In this case, S_7, S_9, and S_{10} are on and the other switches are off. Regarding switches configuration, the second phase is the same one presented in the adder topology case. Fig. 19 shows the electrical diagrams of the subtractor topology operation phases.

The charge flow vectors are derived for a single stage voltage subtractor as following:

$$\begin{aligned} \vec{v_{sub}}^{(1)} &= [q_{out_2}^{(1)} \quad q_{C_{fly_2}}^{(1)} \quad q_{C_{fly_3}}^{(1)} \quad q_{in_2}^{(1)} \quad q_{in_3}^{(1)}] \\ &= [0 \quad -1 \quad 1 \quad q_{in_2} \quad -q_{in_3}] \end{aligned} \tag{3.18}$$

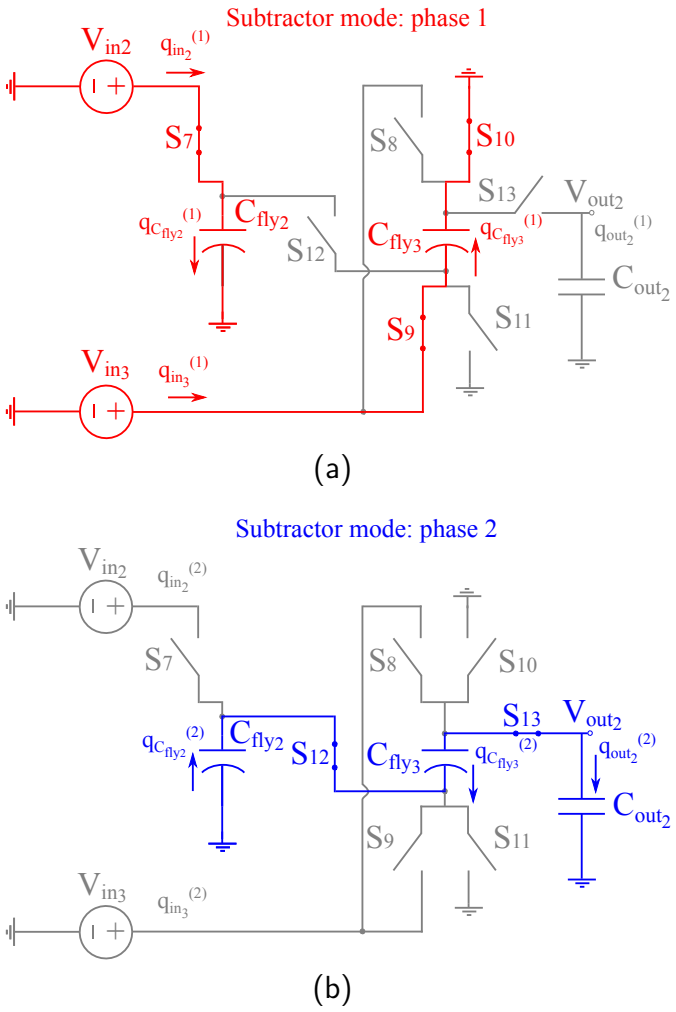
$$\begin{aligned} \vec{v_{sub}}^{(2)} &= [q_{out_2}^{(2)} \quad q_{C_{fly_2}}^{(2)} \quad q_{C_{fly_3}}^{(2)} \quad q_{in_2}^{(2)} \quad q_{in_3}^{(2)}] \\ &= [1 \quad 1 \quad -1 \quad 0 \quad 0] \end{aligned} \tag{3.19}$$

The voltage conversion ratio can than be obtained for this voltage subtractor DC-DC module:

$$VCR = \frac{q_{in}}{q_{out_2}} = \frac{q_{in_2} - q_{in_3} + 0 + 0}{1 + 0} = q_{in_2} - q_{in_3} \tag{3.20}$$

Electrical simulation was executed using 0.6 V and 0.1 V as voltages inputs with no series resistance. The flying capacitors currents have opposite signs and their behavior is the same as the current presented in the previous case, as can be seen in Fig. 20. Fig. 21

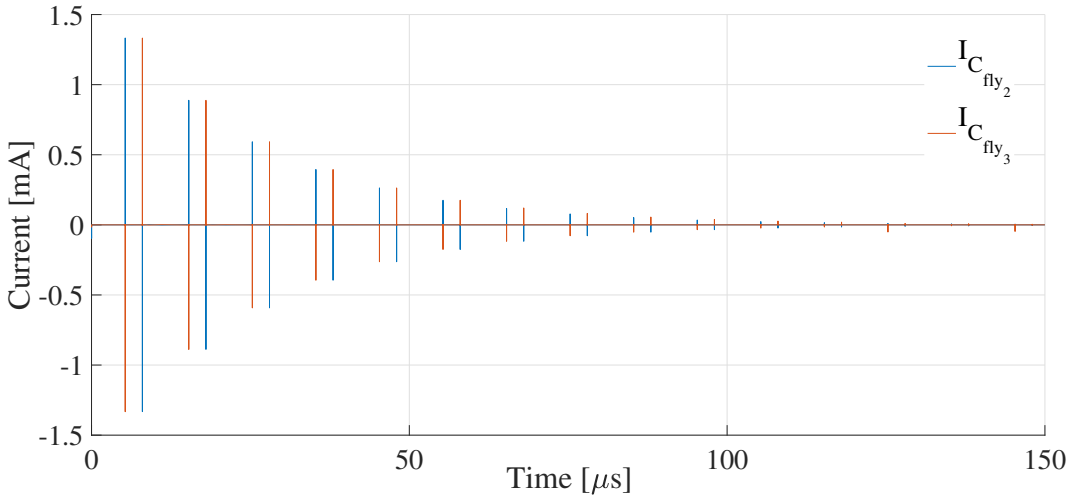
Figure 19 – Operation phase 1 (a) and phase 2 (b) of the Adder/Subtractor converter working as voltage subtractor.



Source: Author

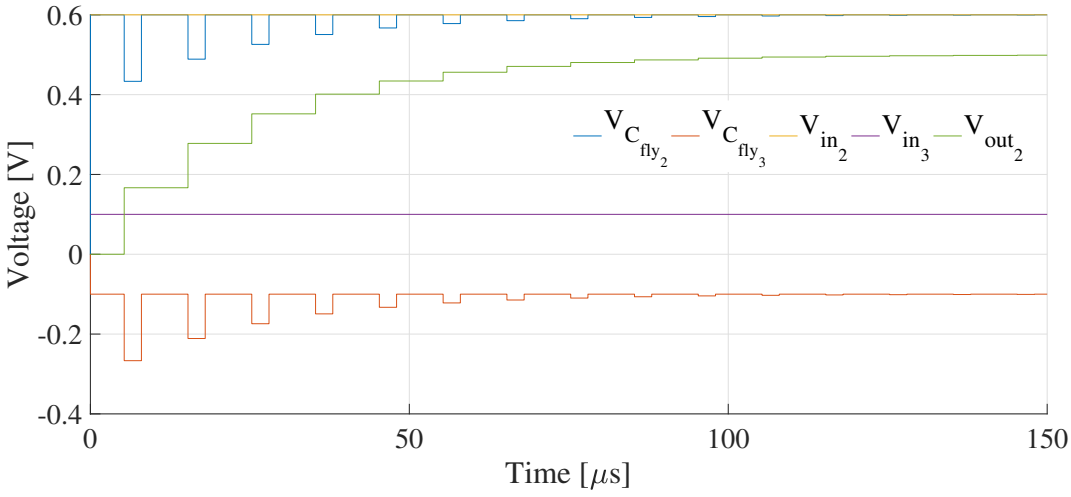
presents the voltages of the two inputs, flying capacitors, and the circuit output. C_{fly_2} is charging positively with the 0.6 V voltage provided by V_{in_2} and C_{fly_3} is charging negatively with the 0.1 V voltage provided by V_{in_3}. Thus the supposed subtraction of the voltages inputs occurs, but the validated value just appears in the output when the flying capacitors complete their charging. The switch signals are the same presented in Fig. 18, but in this case switch S_7 is also representing S_9 and S_{10}.

Figure 20 – Currents of the converter subtractor mode.



Source: Author

Figure 21 – Voltages of the converter subtractorr mode.



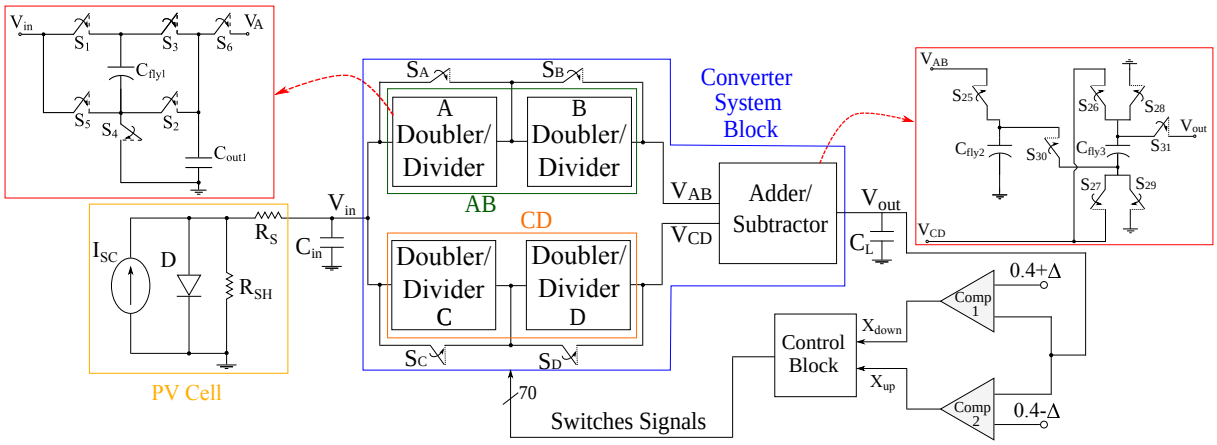
Source: Author

3.5 MULTIPLE-VCR SC DC-DC CONVERTER

Using four Doubler/Divider modules (A, B, C, and D) and the Adder/Subtractor module we created a conversion system to obtain several different VCRs. Modules A and B are in series, composing the AB block. The same occurs for modules C and D, which compose the block CD. AB and CD blocks are in parallel and share the same input voltage provided by the PV cell. The outputs of both blocks are the input voltages for the Adder/Subtractor module, which provides for the load the resulting fixed output voltage. Fig. 22 shows a diagram where the described system can be better understood. It is outlined by blue lines. The bypass switches represented by S_A, S_B, S_C, and S_D are activated when a VCR does not require voltage to pass through any internal module or block. For example, when switches S_A and S_B are on, the voltage provided by the PV cell bypasses AB block and goes directly to one input of the Adder/Subtractor module. Also, all switches of both A and B modules are off preventing a short circuit between the input and output of each module.

Including this bypass switches, the entire converter system block has 35 switches in total. Additionally, there are 10 integrated capacitors and one output load capacitor which is not integrated into the converter system block. Since this output load capacitor can be external to the chip and it is responsible for providing the energy to the load, the output capacitor size can be adjusted depending on the application circuit. Also, an external input capacitance can be used between the PV cell and the DC-DC converter to extract the maximum power of the PV cell and reduce voltage oscillations that may occur during PV cell operation.

Figure 22 – Diagram of the proposed multiple-VCR SC DC-DC converter system.



Source: Author

Combining all topologies configurations with the proposed system it is possible to generate 19 different VCRs: 0.25, 0.5, 0.75, 1, 1.25, 1.5, 1.75, 2, 2.25, 2.5, 3, 3.5, 3.75, 4,

4.25, 4.5, 5, 6 and 8.

The converter system block, outlined by blue lines in Fig. 22, can be easily expanded in order to provide a wider range of VCRs. To accomplish this system expansion, more multi-topology converters can be cascaded in the main block, resulting in more options of ratios with a power of two characteristics. In addition, more main blocks can be added in parallel, and consequently, an Adder/Subtractor converter with more inputs will be able to combine more ratios. Finally, blocks with other single or multi-topology converters can be used in the system in order to offer more options of ratios for the combinations. It is important to note that if the converter system is expanded its output resistance and charge efficiency can be worsened.

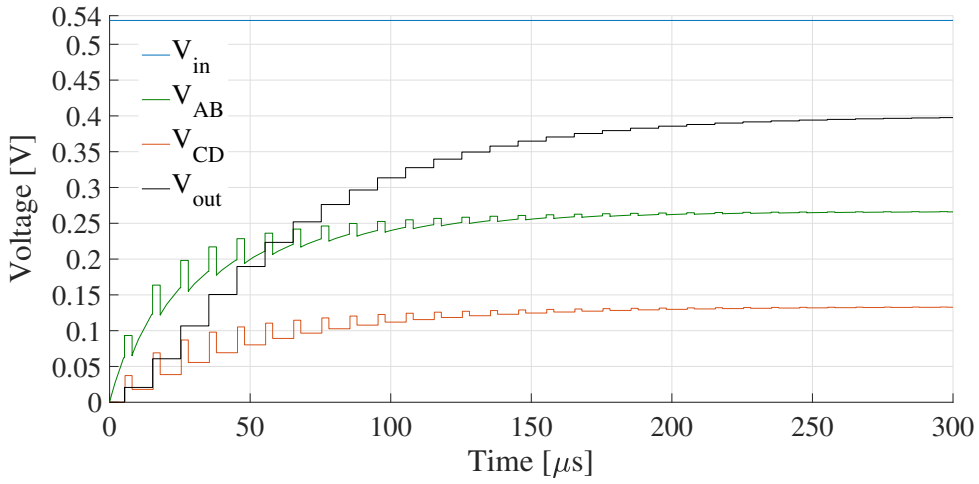
As an example of the system operation, electrical simulations will be presented for two cases with different VCRs: 0.75 and 1.5.

One way to achieve a 0.75 VCR is setting the output of one cascaded Doubler/Divider block with a 0.5 ratio and the other cascaded block with a 0.25 ratio. For AB block, considering the two cascaded multi-topology converters, just one Doubler/Divider module is configured as a voltage divider. The other module is off, and switch S_B is on. The divider output presents a voltage equal to $V_{in}/2$ and the bypass switch replicates this voltage on the AB block output. The two Doubler/Divider modules in the CD block are both configured as voltage dividers, thus this block output is $V_{in}\frac{1}{4}$. The 0.5 ratio in AB block output and 0.25 ratio in CD block output are connected to the Adder/Subtractor converter. The latter is configured as a two-input adder and adds the output ratios of AB and CD blocks. So, the output voltage on the load node is equal to $0.75V_{in}$ V.

A simulation example was executed using 0.533 V as input with a 100 Ω series resistance. Fig. 23 contains the system main voltages. V_{AB} represents the AB block output and V_{CD} represents the CD block output. As previously mentioned, the AB block is configured as a voltage divider, thus its output is around 0.266 V after steady state. CD block has two voltages dividers in sequence and its output is around 0.133 V. Finally, the Adder/Subtractor converter is adding these two output blocks voltages and the load node has a voltage of approximately 0.399 V which corresponds to the $0.75V_{in}$ ratio. Switches signals are presented in Fig. 24. It can be observed that the switches for both the first converters blocks (S_{1A},S_{3A},S_{1C} and S_{3C}) are operating simultaneously, while switches for the CD block second converter (S_{1D} and S_{3D}) only start operation when the second phase of the previous block begins.

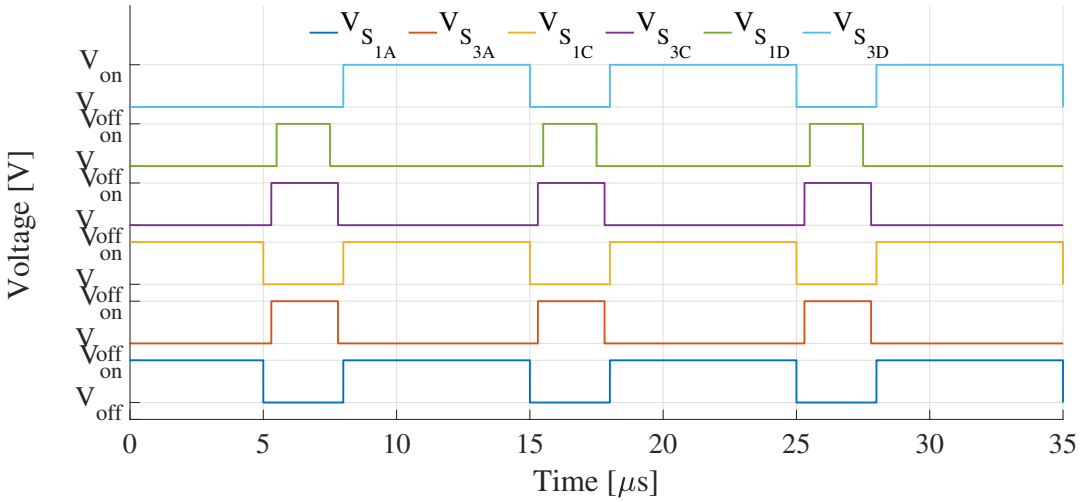
One of the approaches to get a 1.5 VCR is setting one of the blocks as a voltage doubler and the other block as a voltage divider, and then subtracting their ratios. In this example, regarding the two cascaded Doubler/Divider modules on the AB block, module A is configured as voltage doubler topology and the other module is off with switch S_B on. The input voltage is doubled by the first converter and the bypass switch replicates the $2V_{in}$ voltage on AB block output. CD block has similar behavior, but the difference

Figure 23 – Main voltages of the proposed converter system with VCR=0.75.



Source: Author

Figure 24 – Switches signals of the proposed converter system with VCR=0.75.



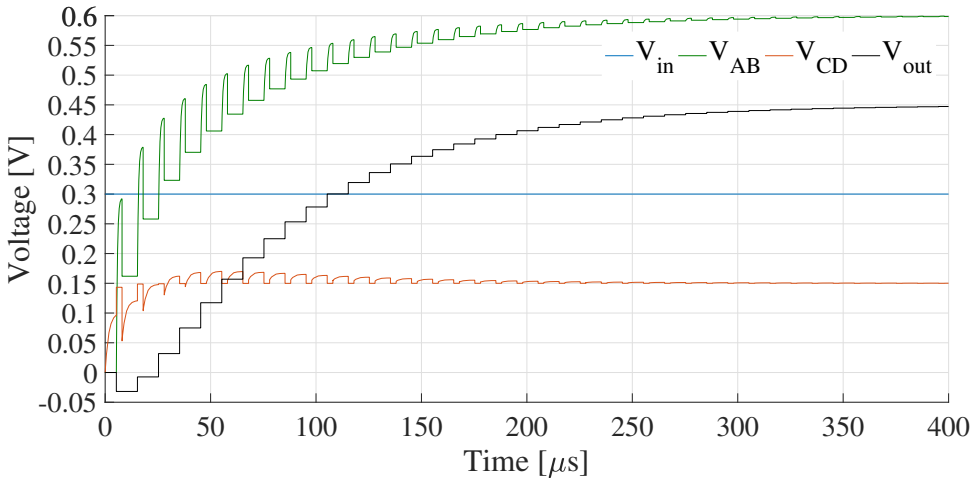
Source: Author

is that its first Doubler/Divider module is configured as a voltage divider. So, CD block output presents a voltage of $V_{in}/2$. These two voltages are subtracted by the subtractor configuration of the Adder/Subtractor converter, and the output voltage on the load node is equal to $1.5V_{in}$ V.

Another simulation example was performed with a voltage input equal to 0.3 V with a 100 Ω series resistance. Fig. 25 presents the system's main voltages and the node names are the same as the previous simulations. As explained before, the AB block is configured as a voltage doubler, thus its output is around 0.6 V after steady state. CD block operates in a similar way, but instead of a voltage doubler, the first module is

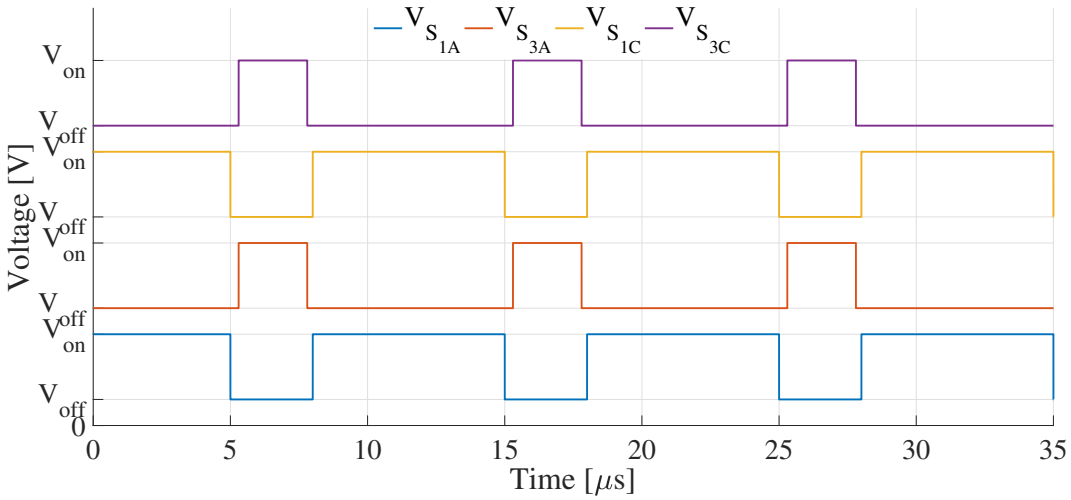
configured as a voltage divider. So, after steady-state, the voltage output on the CD block is around 0.15 V. The Adder/Subtractor converter is subtracting these two output blocks voltages and the load node has a voltage about 0.45 V which corresponds to the $1.5V_{in}$ ratio. Fig. 26 shows the switches signals and can be noted that the switches for both first blocks converters operate simultaneously since they are in parallel.

Figure 25 – Main voltages of the proposed converter system with VCR=1.5.



Source: Author

Figure 26 – Switches signals of the proposed converter system with VCR=1.5.



Source: Author

3.6 CONTROL BLOCK AND COMPARATORS

Figure 22 presents a control block that is used to configure the reconfigurable modules in order to implement the desired VCR. The system can be automatically adjusted by sensing the output voltage and selecting the proper VCR for maintaining the output fixed in 0.4 V. Two comparators (Comp1 and Comp2) sense if the output voltage level is above or below 0.4 V and a digital control selects the switches signals to reduce or increase the current VCR. A Δ parameter is added (subtracted) to the reference voltages at the input of comparators in order to implement hysteresis in the comparison function.

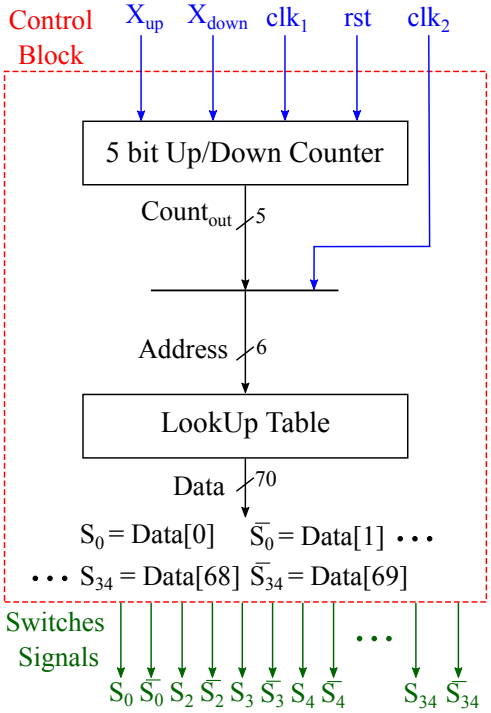
It is important to note that the design and physical implementation of the control block and comparators are outside the scope of this work, which is focused on developing the DC-DC converter. The control block and comparators are essential modules to later demonstrate the behavior of the proposed converter. Then, a suggestion for a simple digital control will be presented and ideal comparators can be used to interact together with the proposed DC-DC converter to validate its operation.

A possible control block implementation consists basically of a digital 5 bit up/down the counter and a lookup table. Fig. 27 presents more details about the control implementation. Signals X_{up}, X_{down}, clk_1, rst and clk_2 are the input of the digital control; X_{down} and X_{up} are the comparison bits provided by comparators Comp1 and Comp2, respectively; clk_1 is the clock signal responsible for controlling the speed increment and decrement of the counter; rst is the signal used to reset the counter to its predefined initial value; and clk_2 is the clock used to generate the conversion system switches signals. The digital control output provides switches signals that are connected to each switch of the conversion system. The control bus has 70 bits.

The counter is responsible for counting or selecting the voltage conversion ratio, and since there are 19 different values, 5 bits are necessary to count all VCRs. The count goes from the lowest to the highest VCR. In our implementation, binary value 00001 represents VCR=0.25 (minimum) and 10011 represents VCR=8 (maximum). Values between this range represent intermediate VCRs, and values outside this range turn all switches off so that no VCR is configured. Counter increases or decreases based on the comparison bits, X_{up} and X_{down}, provided by the comparators. For example, if the converter output voltage is greater than (0.4 + Δ) V, the counter will decrease by one its count to decrease VCR; if the converter output voltage is smaller than (0.4 - Δ) V, the counter will increase by one its count to increase VCR; finally, if the converter output voltage is in the range of (0.4 $\pm\Delta$) V, the counter keeps its value to maintain the current VCR. Figure 28 shows a flowchart that explains in more detail the logic operating of the 5 bit up/down counter.

At every transition of clk_1 from low to high, a step of the flowchart of Fig. 28 is executed. If the reset signal (rst) is high, then the counter ($Count_{out}$) is reset to the predefined initial value 00001 that represents the smaller available VCR (=0.25) for the

Figure 27 – Block diagram of the proposed digital control.

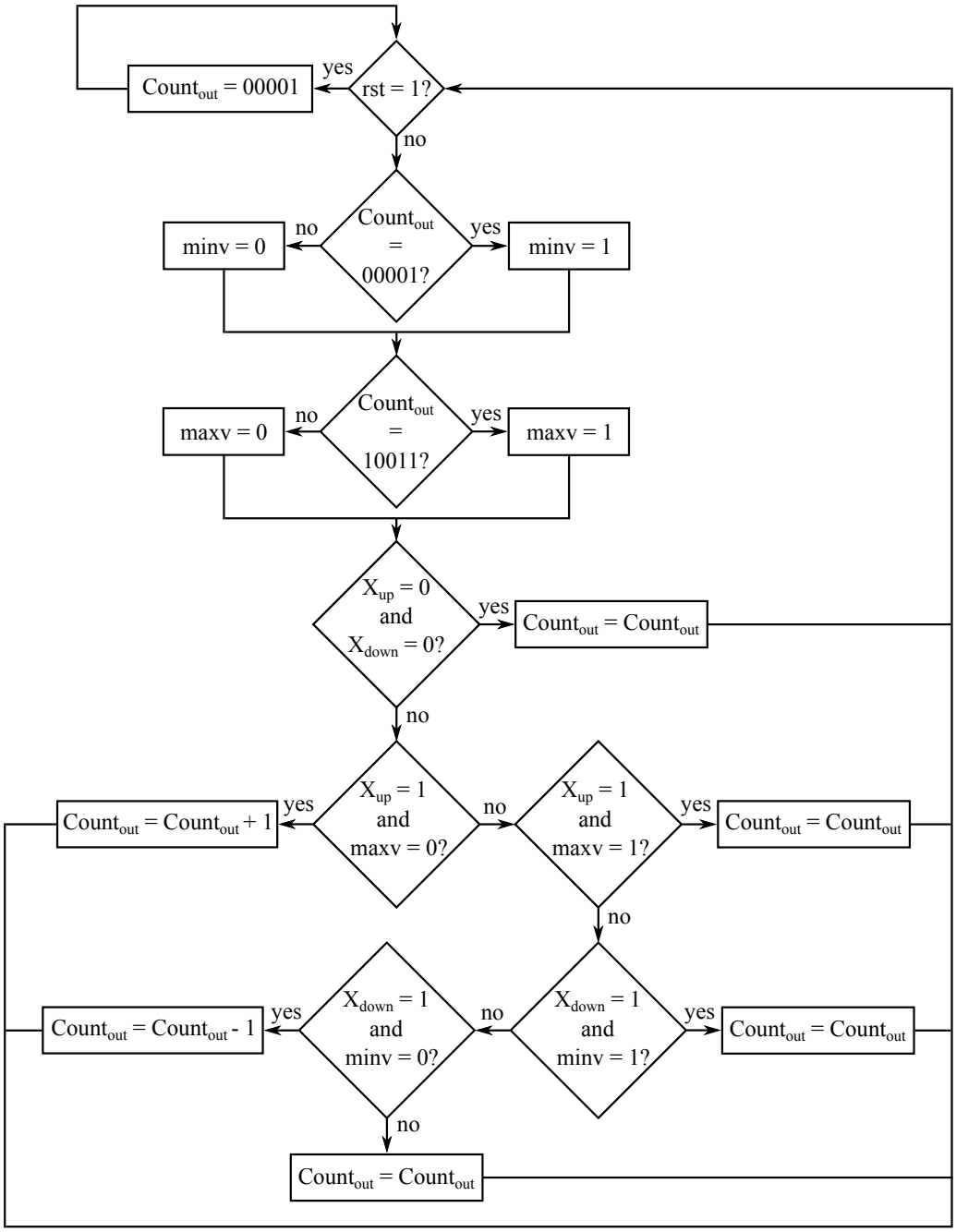


Source: Author

conversion system. When rst is low then $Count_{out}$ value is verified to check if the counter achieved the lowest or the highest VCR. This measure serves to prevent the counter from continuing to increase or decrease when a minimum or maximum value of VCR is reached since the counter can count more values than the number of available VCRs. So, when the counter is representing the minimum VCR, flag minv goes high; and flag maxv goes high when the counter is at the maximum VCR. The next steps consist of checking the states of the comparison bits (X_{up} and X_{down}) and the mentioned flags to decide the action for the counter. X_{up} and X_{down} in low state indicates that the converter output voltage is in the range of 0.4 $\pm\Delta$ V, so the counter does not change its value. When X_{up} is high, it means converter output voltage is smaller than 0.4 - Δ V and the counter increments (increase VCR) only if the flag maxv is low. Otherwise the counter keeps the current value. Similarly, when X_{down} is high the converter output voltage is greater than 0.4 + Δ V. Then, the counter decrements (decrease VCR) only if flag minv is low. Otherwise, the counter keeps its current value.

It is known that for each VCR there are different switches configuration that must turn on and off in operating phases 1 and 2. In our implementation, each configuration is preallocated and saved in a lookup table. The access address of this lookup table has 6 bits. The 5 most significant bits represent the VCR informed by the counter ($Count_{out}$), and the least significant bit represents the operation phase, 1 and 2, which is informed by an alternating clock signal called clk_2. Phase 1 of operation is represented by $clk_2 = 0$

Figure 28 – Flowchart of the digital control counter.



Source: Author

and phase 2 is represented by $clk_2 = 1$. Table 4 shows the values contained in the lookup table. In order to simplify the switches signals representation in Table 4, only one signal was shown per switch, but in the implementation there are two signals where one is the complement of the other. The switches signals control bus is composed as follows: $S_0\bar{S}_0S_1\bar{S}_1S_2\bar{S}_2S_3\bar{S}_3...S_{34}\bar{S}_{34}$. This control bus represents the switches signals of Fig. 22. The equivalence is defined as: from S_0 to S_5 represent switches S_1 to S_6 of the Doubler/Divider A module; from S_6 to S_{11} represent switches S_1 to S_6 of the Doubler/Divider B module;

from S_{12} to S_{17} represent switches S_1 to S_6 of the Doubler/Divider C module; from S_{18} to S_{23} represent switches S_1 to S_6 of the Doubler/Divider D module; from S_{24} to S_{30} represent switches S_7 to S_{13} of the Adder/Subtractor module; finally, from S_{31} to S_{34} represent the bypass switches S_A to S_D.

Table 4 – Example of the implemented lookup table of the digital control block.

Address			Switches Signals
VCR	$Count_{out}$	clk_2	$S_0S_1S_2S_3S_4S_5S_6S_7S_8S_9S_{10}S_{11}S_{12}S_{13}...S_{34}$
0.25	00001	0	0000000011011100000011011011000100
		1	0000001100000011011100000000000111000
0.50	00010	0	1100000011011100000011011100100000
		1	0011011100000011011100000000000110000
0.75	00011	0	0000000000001100000011011011000110
		1	0000000000000011011100000000000111100
1.00	00100	0	0000001100000000001100000000000111010
		1	0000000011010000000011011100100101010
1.25	00101	0	0000000000001100000011011100100110
		1	0000000000000011011100000000000111100
1.50	00110	0	0000000000000000001100000000000111110
		1	0000000000000000000011011100100111010
1.75	00111	0	0000001001011100000011011011000100
		1	0000000010110011011100000000000111000
2.00	01000	0	0000000000000000000000000011001001111
		1	0000000000000000000000000000000111111
2.25	01001	0	0000001001011100000011011100100100
		1	0000000010110011011100000000000111000
2.50	01010	0	0000001001010000001100000000000111010
		1	0000000010110000000011011100100101010
3.00	01011	0	0000000000000000000100101110010011110
		1	0000000000000000000001011000000111110
3.50	01100	0	1001010010110000001100000000000110010
		1	0010111001010000000011011011000010
3.75	01101	0	1001010010111100000011011011000000
		1	0010111001010011011100000000000110000
4.00	01110	0	0000001001010000001001011100100101010
		1	0000000010110000000001011000000111010
4.25	01111	0	1001010010111100000011011100100000
		1	0010111001010011011100000000000110000
4.50	10000	0	1001010010110000001100000000000110010
		1	0010111001010000000011011100100010
5.00	10001	0	1001010010110000000000000011001000011
		1	0010111001010000000000000000000110011
6.00	10010	0	1001010010110000001001011100100010
		1	0010111001010000000001011000000110010
8.00	10011	0	1001010010111001010010111100100000
		1	0010111001010010111001010000000110000

Source: Author

3.7 CONCLUSION

This chapter presents a simplified model to understand the operation of the switched-capacitor converter topologies. Some proposed structures of SC converters, such as the voltage-doubler and the voltage-divider are introduced and their operation phases explained in terms of charge flow analysis. The chapter also presents the concept of multi-topology SC converters and their application to obtain more than one voltage conversion ratio with a single topology. This concept is used to explain the operation of the proposed SC based topology capable of providing a range of different VCRs. In addition, this chapter presents some electrical simulations validating the operation of the blocks which compose the converter system, as well as the operation of the complete converter system. Lastly, the operation and construction details of the suggested digital control system are addressed in the chapter.

4 DESIGN METHOD

This chapter details the choices made for the practical implementation of the proposed DC-DC conversion system. The systematic method based on electrical simulations is proposed. It is used to design switches, capacitors, and operating frequency that compose the VCR adjustable switched-capacitor DC-DC converter.

4.1 CONVERTER SYSTEM DESIGN METHOD

According to Breussegem and Steyaert (2012), the design of a capacitive DC-DC converter containing multiple topologies introduces some additional constraints compared to single topologies. The author describes that the multiple topologies converter design should include the influence of the additional idle switches (since multiple topologies converter requires more switches), meet the requirements for a set of operation points, and give an optimum solution given a set of user constraints.

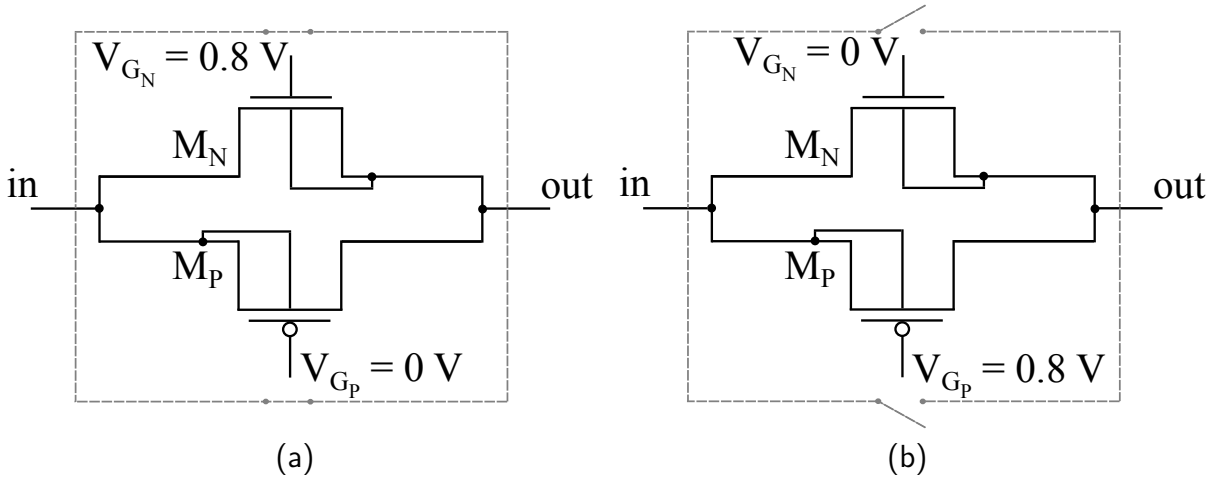
Following this idea, the single topology converter model is extended and a multi-objective algorithm is used for the purpose of optimizing the design. Beyond the multi-objective algorithm, it is necessary a complete mathematical modeling of the capacitive converter modules. Moreover, the modeling parameters presented by Breussegem and Steyaert (2012) can not be applied for the Adder/Subtractor converter module proposed in this work since its a two input converter topology.

On the other hand, we also propose a systematic design method based on electrical simulations in order to provide a practical way to size capacitors, switches, and operating frequency. This method does not require the complete modeling of the switched-capacitor converter modules.

The design of the proposed DC-DC converter includes the sizing of capacitors and switches and the definition of optimal or ideal switches operating frequency. CMOS transmission gates are used for all switches of the proposed conversion system, and the design was performed in a CMOS 180 nm process. The transmission gate is implemented with the bulk node of each transistor connected to the respective source node. This approach can be implemented using a deep n-well transistor and avoids the use of large transistors to compensate for the increase in the threshold voltage. Synopsys HSpice is used for all schematic electrical simulations.

The schematic of the transmission gate used as switches is denoted by the black lines of Fig. 29. To turn a switch on it is necessary to apply a voltage V_{G_N} of 0.8 V on the M_N transistor gate and $V_{G_P} = 0$ V on the M_P transistor gate as shown in Fig. 30a. On the other hand, to turn a switch off it is necessary to apply a voltage V_{G_N} of 0 V on the M_N transistor gate and $V_{G_P} = 0.8$ V on the M_P transistor gate as shown in Fig. 30b. Since the transmission gate is built with two transistors, n-type and p-type, there are two opposite signals (V_{G_N} and V_{G_P}) for each switch. The converter system block has 35 switches in total, so there are 70 bits in the control bus presented in Fig. 27.

Figure 29 – Electrical schematic of the transmission gate used as switch: switch turned on (a) and switch turned off (b).



Source: Author

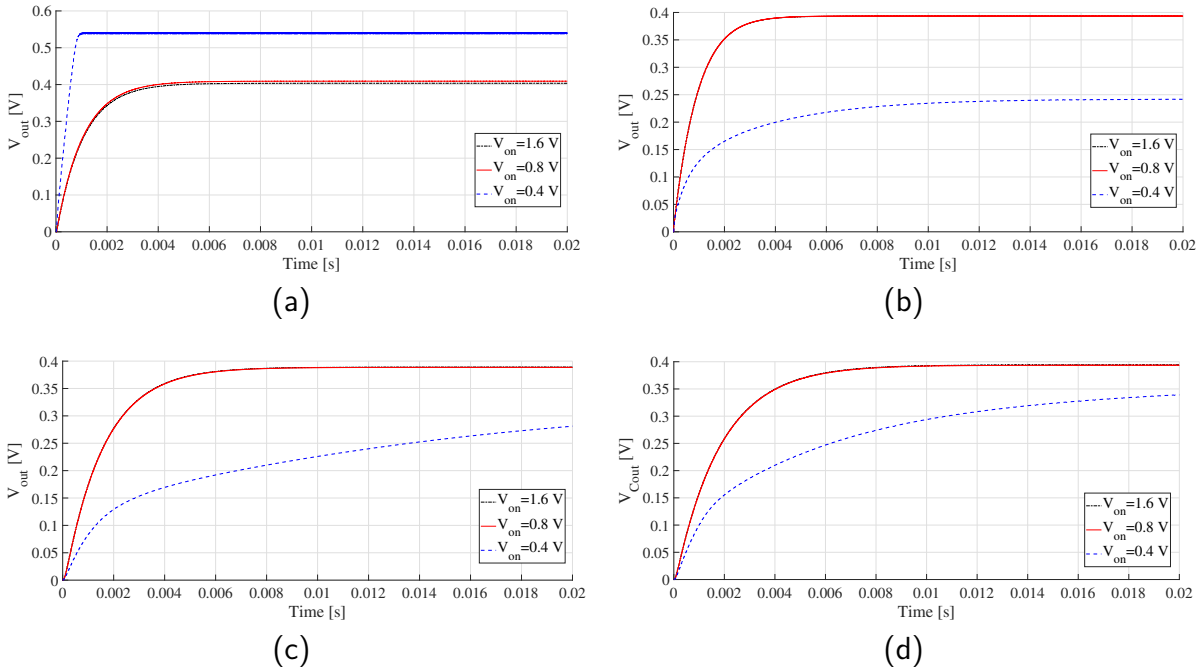
The transmission gates were chosen to implement the converter switches after comparing with n-type MOSFET switches with respect to the operation of the conversion system block charging the output load capacitor C_L. For this comparison, electrical simulations were executed using the converter system switches implemented only with transmission gates and only with n-type MOSFETs. Four VCRs were simulated: 0.5 and 0.75 to represent the situation when higher voltages are presented (V_{in} = 0.8 and 0.533 V) on the converter system input, and 4.5 and 8 when lower voltages are presented (V_{in} = 0.088 and 0.05 V). For a simpler representation, the voltage applied as V_{G_N} to turn on the switches is named here as V_{on}, and V_{G_P} is always the opposite voltage of V_{G_N} as represented in Fig. 29. Three different voltages were used as V_{on} for each VCR simulation: 0.4, 0.8, and 1.6 V. These voltages represent the converter V_{out}, twice the converter V_{out} and four times the converter V_{out}, respectively.

The simulated curves for the transmission gate switches implementation are presented in Fig. 30, and the simulated curves for n-type MOSFET switches implementation are presented in Fig. 31.

There is no relevant difference between the switches implementations when lower voltages are presented as V_{in} and the system behaves as a step-up converter (VCR = 4.5 and 8). In Figs. 31c, 31d, 32c, and 32d the curves for V_{on} equal to 1.6 V (black line) and 0.8 V (red line) are almost overlapped. In this case a minimum V_{on} voltage of 0.8 V charges the output load capacitor with the desired voltage of 0.4 V (or near to it) in both implementations.

A clearer difference between the two implementations appears, in the worst-case scenario, when higher voltages are presented as V_{in} and the system behaves as a step-down converter (VCR = 0.5 and 0.75). As observed in Figs. 32a and 32b, for the n-type

Figure 30 – Electrical simulations of the converter system block built with transmission gate switches varying V_{on} for: VCR=0.5 (a), VCR=0.75 (b), VCR=4.5 (c), and VCR=8 (d).



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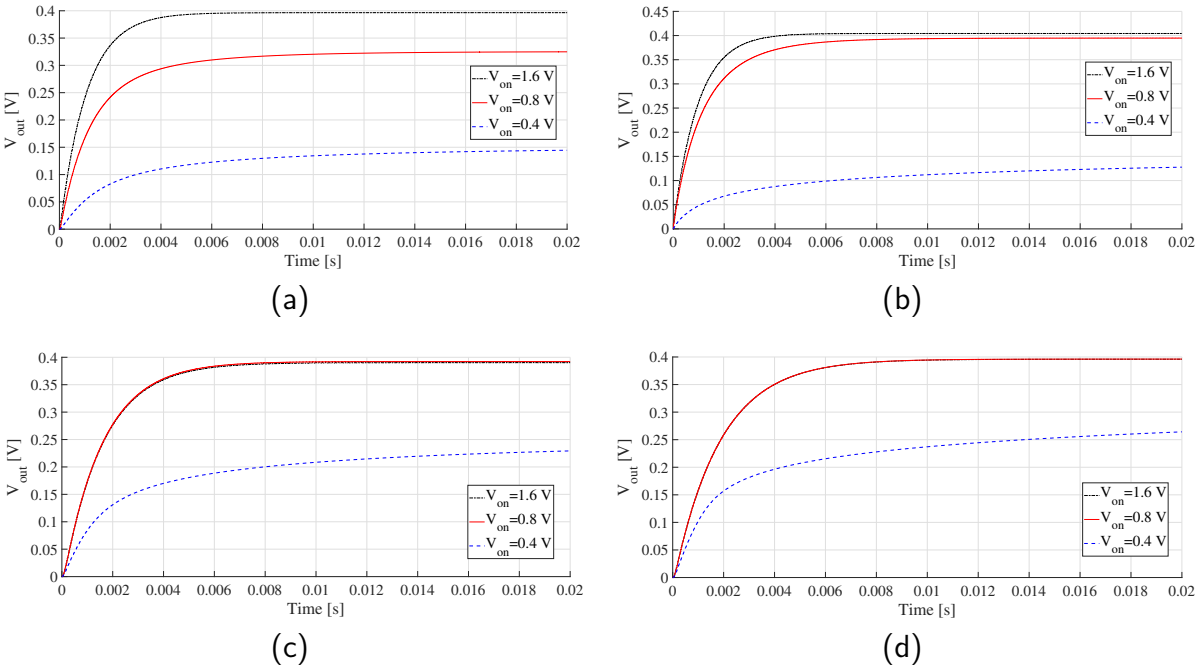
MOSFET switches implementation a V_{on} equal to 1.6 V is necessary to charge the output load capacitor with 0.4 V mainly when the input voltage is 0.8 V (VCR = 0.5). This can be confirmed by the fact that in this case, the V_{DS} of the transistor that composes the switch is large because V_{in} is higher, so V_{GS} needs to be increased so that the switch operates as expected. The transmission gate switches implementation maintains the same performance for the step-down VCRs, compared to step-up VCRs, to charge the output load capacitor with a minimum V_{on} voltage of 0.8 V as shown in Figs. 31a and 31b. In this worst-case scenario, transmission gates are better switch implementations as they do not need a higher V_{on} voltage for proper operation. For this reason, transmission gates were chosen to implement all converter system switches with V_{on} equal to 0.8 V.

The final version of the energy harvesting system, which includes the converter system proposed by this work, needs to be as simple as possible and completely integrated. Using the converter output voltage itself as a signal to turn on/off switches is an interesting idea which avoids the need of an extra and dedicated circuit for providing the desired voltage to drive the switches.

Considering that after start-up, when the output load capacitor is already charged with 0.4 V, this voltage is used to supply the load and, additionally, it can be used to the clock generator circuit to provide signals to drive the switches. However, a voltage of 0.4 V at the gate of the transistors is not sufficient for proper operation of the switches, especially

Figure 31 – Electrical simulations of the converter system block built with n-type MOSFET switches varying V_{on} for: VCR=0.5 (a), VCR=0.75 (b), VCR=4.5 (c), and VCR=8 (d).



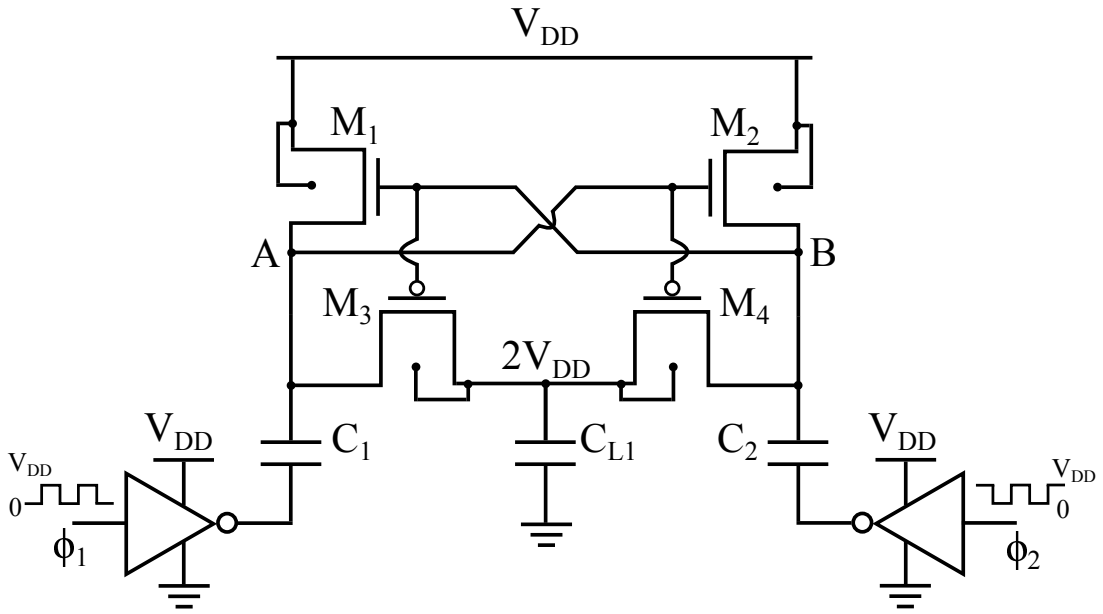
Source: Author

in step down VCRs. This is due to the fact that in these cases $V_{DS} > V_{GS}$, impacting the operation of the transistors as a switch. So, the output voltage of the converter must be doubled to offer a voltage near to 0.8 V (steady-state) to properly control the switches. This can be accomplished with the aid of a voltage doubler circuit like the cross-coupled doubler topology of Fig. 32, proposed by TianRui Ying, Wing-Hung Ki and Mansun Chan (2003). This circuit has a simple operation in which there are two pulsed input signals, ϕ_1 and ϕ_2, alternating between 0 and V_{DD} V. They are complementary signals, so when ϕ_1 is equal to V_{DD}, ϕ_2 is equal to 0 V and vice versa. This controls the circuit so that one side operates at a time and C_1 and C_2 capacitors are charged with V_{DD} V. The C_{L1} capacitor is charged up in both phases with $2V_{DD}$ because C_1 and C_2, charged with V_{DD}, are placed in series with the V_{DD} provided by the inverters. Also, in nodes A and B there are complementary signals alternating between $2V_{DD}$ and V_{DD}.

By setting the V_{DD} of this circuit as the output voltage of our proposed conversion system, it is possible to double the converter output voltage from 0.4 to 0.8 V in the steady-state.

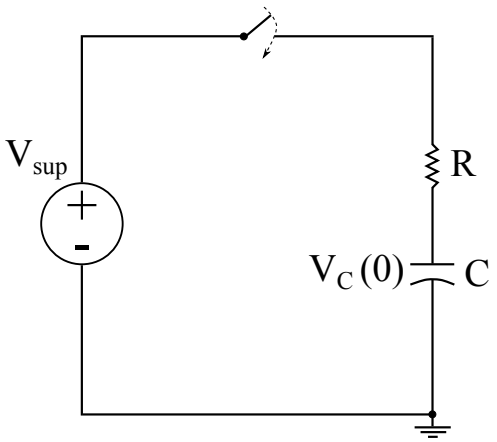
Considering a real capacitive DC-DC converter, the energy is transferred from the input supply to the load by means of capacitors. Figure 33 shows a circuit diagram used to model the charging process of capacitor C after switching (at t=0). This circuit can be used to model the energy transfer from a supply to a single capacitor. In order to simplify,

Figure 32 – Cross-coupled doubler circuit.



Source: Author

Figure 33 – Circuit diagram used to model the charging process of capacitor C after switching (at t=0).



Source: Author

the charging of a single capacitor is analyzed but the conclusions can be expanded for analyzing the energy transfer between two capacitors.

A differential equation can be used to describe the process of charging a capacitor:

$$-V_{sup} + RC\frac{dV_C}{dt} + V_C = 0 \tag{4.1}$$

where $C\frac{dV_C}{dt}$ is the current flowing after the switch is closed.

Solving Eq. 4.1 for $V_C(t)$ and deriving the current through the capacitor $I_C(t)$,

the following equations are obtained:

$$V_C(t) = V_{sup} - (V_{sup} - V_C(0))e^{\frac{-t}{RC}} \tag{4.2}$$

$$I_C(t) = \frac{V_{sup} - V_C(0)}{R} e^{\frac{-t}{RC}} \tag{4.3}$$

The power transferred to the capacitor is:

$$P_C(t) = V_C(t)I_C(t) = \frac{V_{sup}V_C(0) - V_C^2(0)}{R} e^{\frac{-t}{RC}} \tag{4.4}$$

And the energy added to the capacitor in this process can be obtained:

$$E_C = \int_0^\infty P(t)dt = \frac{V_{sup}^2 - V_C^2(0)}{2} C \tag{4.5}$$

Similarly the total energy delivered by the supply voltage source can be obtained:

$$E_{tot} = V_{sup}(V_{sup} - V_C(0))C \tag{4.6}$$

There is a power loss caused by the resistive losses in R, so the total energy delivered by the supply source is higher than the energy stored in the capacitor. Thus, part of the energy is lost and this is quantified by the charging efficiency $\eta_{C_{charge}}$ presented by Wens and Steyaert (2011):

$$\eta_{C_{charge}} = \frac{E_C}{E_{tot}} = \frac{V_C(0) + V_{sup}}{V_{sup}} \frac{1}{2} \tag{4.7}$$

The equations presented previously were derived considering an infinite charging period. In practice, it represents a good approximation as long as the capacitor voltage is settled within 10% of the charging voltage (BREUSSEGEM; STEYAERT, 2012).

Table 5 presents the maximum charging efficiency that can be obtained for different values of the initial capacitor voltage. This table was built using Eq. 4.7 for some cases of $V_C(0)$ as a percentage of V_{sup}. It can be noticed that charging efficiencies are higher when the initial voltage in the capacitor is near to the supply voltage.

So, using Eq. 4.7 the efficiency - and consequently the power loss - of a capacitive converter block can be estimated when considering the relation of the converter output energy and the energy delivered at its input. This estimation can be easily performed through electrical simulation considering the energy that is presented in the converter input and the energy used to charge the load capacitor connected to the converter output. It is important to note that the maximum charging efficiency is limited by the initial voltage presented in the capacitor. According to Table 5, considering the capacitor fully discharged ($V_C(0) = 0V$), the maximum possible efficiency is limited to only 50% if there is no power loss.

According to Breussegem and Steyaert (2012) the Output Impedance Model is a good model for designing a capacitive DC-DC converter. This model is composed of a DC-transformer with a fixed iVCR and with a non-zero output impedance R_{out}. The output impedance represents the losses associated with switching the capacitors and the resistive losses of the converter. It is totally related to the switches operating frequency and the charging modes mentioned before. The Full Charging Mode (FCM) governs the Slow Switching Limit (SSL) output impedance R_{SSL}. The latter is inversely proportional to the switching frequency and to the total amount of flying capacitance. The Fast Switching Limit Output Impedance R_{FSL}, governed by the Partial Charging Mode (PCM), is inversely proportional to the total switch conductance. Following the authors' idea, the output impedance of a real capacitive DC-DC converter is subject to both Slow Switching and Fast Switching Component. Therefore, we can conclude that the R_{out} of a capacitive DC-DC converter is affected directly by the sizes of flying capacitors, sizes of switches, and the switches operating frequency, which are the design parameters of the switched-capacitor converter.

In order to optimize the converter output resistance and the switching frequency, the period of time for phase 1 must be exactly the time necessary for charging flying capacitors to a value close to the input voltage. In phase 2, the charge must be completely transferred to the load (BREUSSEGEM; STEYAERT, 2012). It means that changing switching frequency affects the amount of charge that the flying capacitor receives and, consequently, the amount of charge transferred to the load at each cycle. In general, the lower the switching frequency, the longer it takes to fully charge the output capacitor since less charge is transferred at each cycle. Following this idea, there is an ideal period of time in which the flying capacitor charges near to the maximum voltage and discharges completely to the output capacitor. The ideal frequency depends on the resulting RC constant, which is related to capacitor sizes and parasitic resistances and capacitance of switches.

Table 5 – Maximum charging efficiency related to the initial capacitor voltage.

$V_C(0)$ (% of V_{sup})	Maximum Charging Efficiency (%)
0	50.00
12.5	56.25
25.0	62.50
37.5	68.75
50	75.00
62.5	81.25
75.0	87.50
87.5	93.75
100	100

Source: Author

As a practical example, electrical simulations were performed with the Adder/ Subtractor module of Fig. 14 operating as a voltage adder. Two voltage sources of 0.2 V are connected to both converter inputs ($V_{in_2} = V_{in_3}$). Flying capacitors (C_{fly_2} and C_{fly_3}) are set to 10 pF, the output load capacitor C_{out_2} is set to 250 pF, and switches are set to minimum size (W = 220 nm and L = 180 nm). Figure 34 shows the flying capacitors and the output voltages for three simulations with distinct switches operating frequencies (59 kHz, 590 kHz, and 5.9 MHz) that graphically exemplify the capacitor operation modes modes

In Fig. 34a the switching frequency is 59 kHz. With this frequency, the flying capacitors charge with a voltage very close to the input value, but after reaching this voltage they take about 7 μs to transfer their charge to the output capacitor. This is an example of the Full Charging Mode. This mode makes the charging of the output capacitor slower and the flying capacitors are unnecessarily idle during a large period of time.

The operating frequency is 5.9 MHz in the simulations of Fig. 34c. As can be noted, both flying capacitors discharge to the output capacitor before charging with a voltage very close to the input source. The sum of the voltages in capacitors C_{fly_2} and C_{fly_3} reaches approximately 0.175 V, and then they transfer their charges to the output capacitor. This is an example of the Partial Charging Mode. In this charging mode, C_{out_2} charges faster, but it implies more switching losses, worsening the efficiency of the converter.

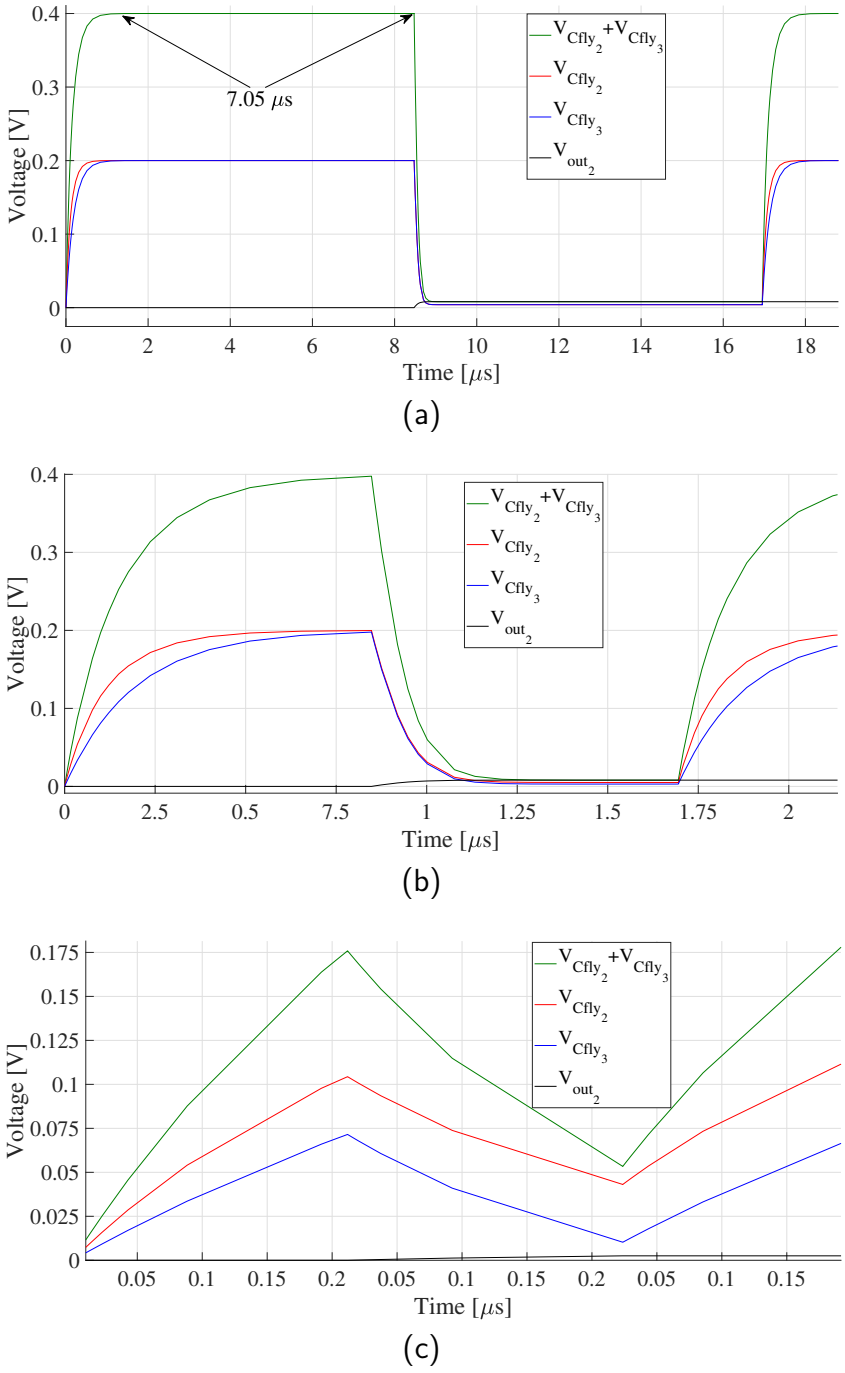
Finally, Fig. 34b presents a frequency of 590 kHz, close to the ideal operating frequency defined so far. In this case, both flying capacitors charge to the input voltage (or very near to it) and then discharge to the output capacitor, without relevant idle time. This is called the Boundary Charging Mode (BCM). It is very interesting for a switching capacitor converter to operate in this charging mode because the converter output resistance will be near to the minimum possible value with a minimum switching frequency (BREUSSEGEM; STEYAERT, 2012).

The converter output resistance can also be estimated using electrical simulations and Eq. 4.2. The voltage $V_C(t)$ is known in a transient analysis. Since V_{sup} is the voltage that charges C (which represents the output load capacitor), $V_C(0)$ can be set to any value between 0 and V_{sup} V. The only unknown variable left in the equation is the resistor R. So, we can solve Eq. 4.2 to R as:

$$R = -t \cdot (C \cdot ln(\frac{V_{sup} - V_C(t)}{V_{sup} - V_C(0)}))^{-1} \tag{4.8}$$

For the purpose of validating the estimation of the output resistance with this method, Fig. 35 presents the comparison between the output load capacitor charged by the adder converter and the output capacitor charged with the equivalent RC circuit, where R is the estimated R_{out} and C is the output load capacitor. The same switching frequencies of Fig. 34 are used here. Analyzing Fig. 35 we can observe that for a switching frequency up to 590 kHz, Figs. 36a and 36b, the R_{out} estimation represents with very good precision

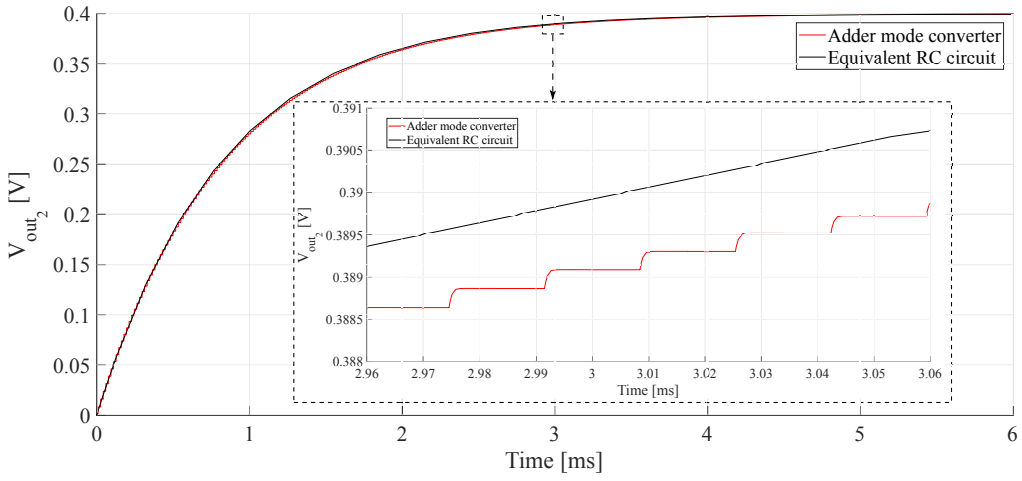
Figure 34 – Electrical simulations of the Adder/Subtractor module working as voltage adder with switches operating frequency of: 59 kHz (a), 590 kHz (b), and 5.9 MHz (c).



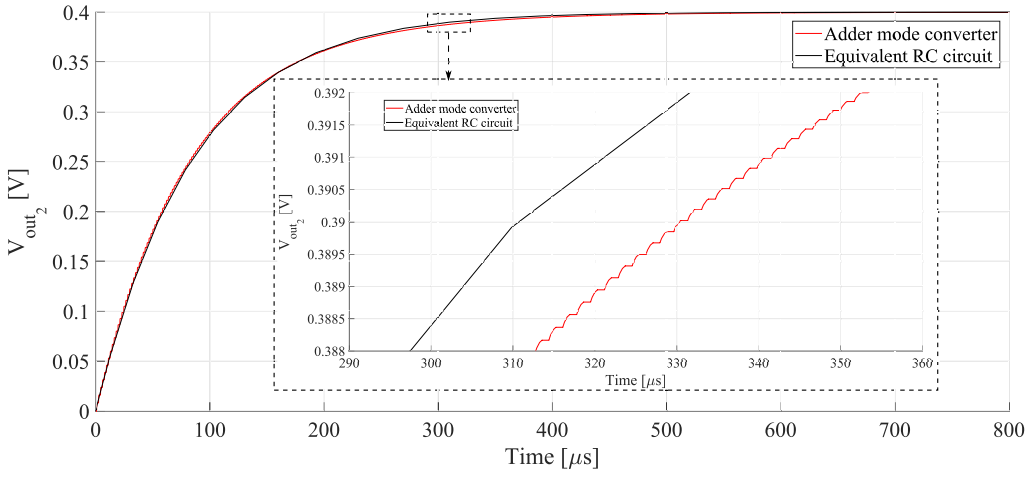
Source: Author

the entire voltage charge of the output capacitor. In Fig.36c, which has a frequency in the PCM region, there is only a small discrepancy in the initial charging of the output capacitor.

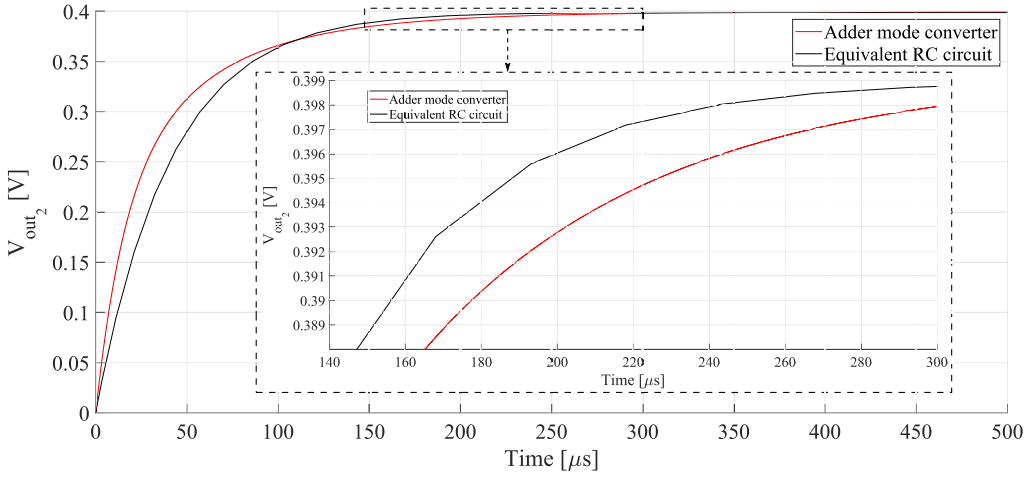
Figure 35 – Comparison between the output capacitor being charged by the adder mode converter and its equivalent RC circuit for switching frequency of: 59 kHz with R_{out}=3.28 MΩ (a), 590 kHz with R_{out}=347 kΩ (b), and 5.9 MHz with R_{out}=165 kΩ (c).



(a)



(b)

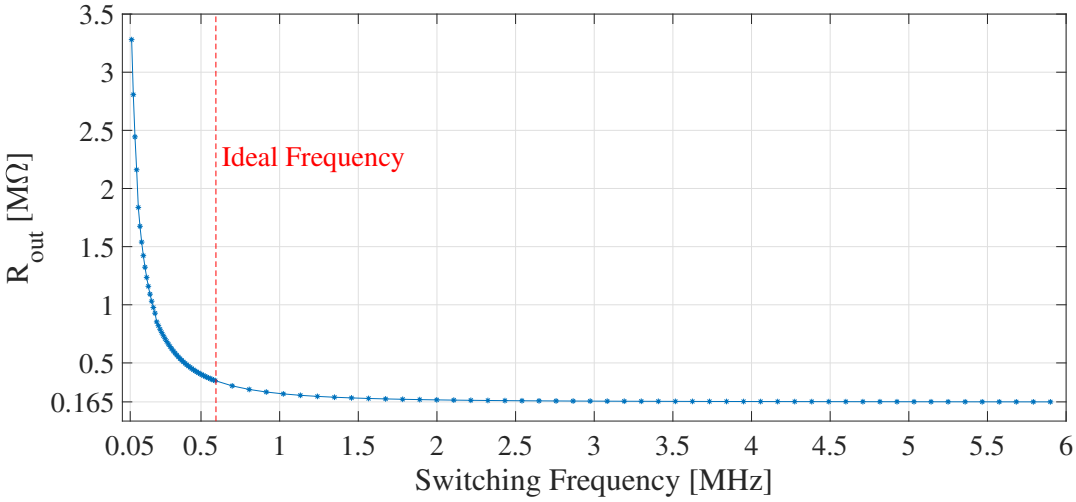


(c)

Source: Author

Another electrical simulation of the Adder/Subtractor module, working in adder mode and with the same configuration of simulations from Fig. 35, was performed to graphically exemplify the relation between the converter output resistance and the switches operating frequency. Figure 36 shows the behavior of the converter output resistance R_{out} over a switching frequency range of 59 kHz to 5.9 MHz. R_{out} was estimated using Eq. 4.8 and electrical simulations. It is possible to note that when operating in FCM, R_{out} is greatly reduced with the frequency increasing. In this case, R_{out} decreases from 3.28 M to 347.7 kΩ when the switching frequency is varied from 59 k to 590 kHz. Nevertheless, in PCM, R_{out} only reduces from 347.7 k to 165.1 kΩ when switching frequency is varied from 590 k to 5.90 MHz. The red dotted line in Fig. 36 represents the ideal frequency of 590 kHz. This frequency demarcates the BCM region, which is the transition region between the FCM to the PCM. It is advantageous to operate in BCM in order to minimize R_{out} and the switching frequency.

Figure 36 – Relation between converter R_{out} and switching frequency of the Adder/Subtractor module working in adder mode.



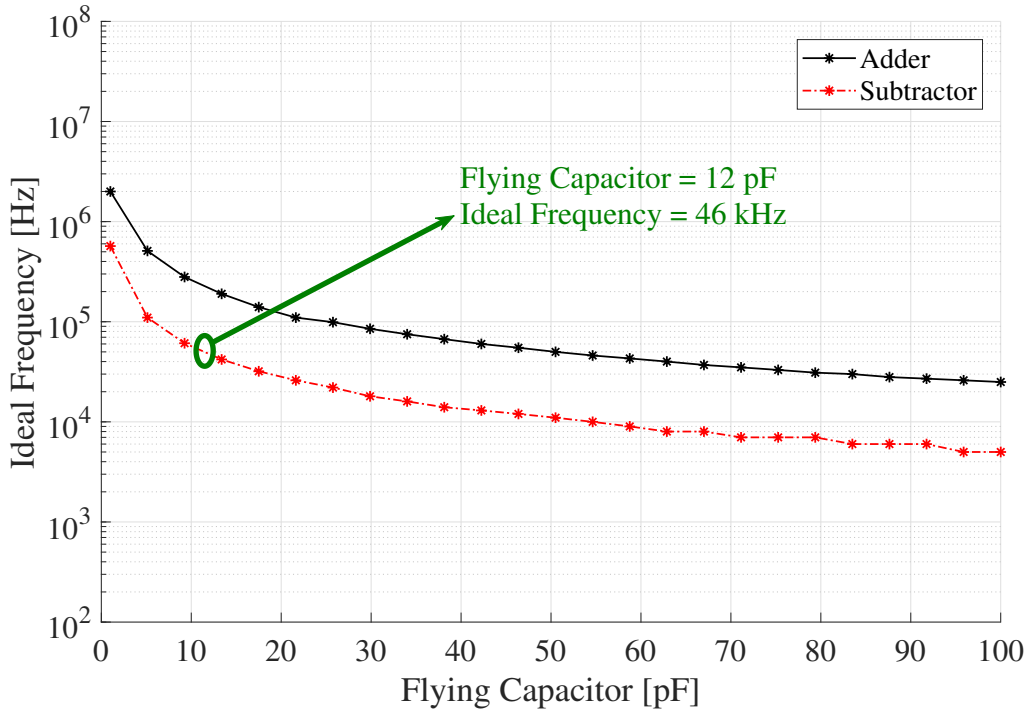
Source: Author

In the first version of our proposed design method, we included the sizing of the switches, capacitors, and switches operating frequency that make up the conversion system.

Regarding the conversion system proposed in Fig. 22 from Chapter 3, the Adder/Subtractor module is the last block in the charge path and it is responsible for charging the load capacitor. Then, the analysis for sizing flying capacitors must begin with this block. Varying the size of the two flying capacitors presented in the Adder/Subtractor module, the corresponding ideal operating frequency for each capacitor size can be estimated.

Simulations were performed with the Adder/Subtractor module working in two

Figure 37 – Ideal frequency versus flying capacitors value in the two operation modes of the Adder/Subtractor module.



Source: Author

operation modes (adder and subtractor modes). In each simulation, flying capacitors were varied from 1 pF to 100 pF and the correspondent ideal frequency was obtained. Figure 37 shows this relation for the two converter operation modes.

There is a trade-off between the capacitor value (and respective capacitor area - 2 fF / μm^2 for MiM Cap in 180 nm node) and the ideal operating frequency. As the capacitor value is reduced, the ideal operating frequency increases, which can cause more switching losses. On the other hand, if lower operating frequencies are used to minimize switching losses, larger capacitors are required, consuming more chip area.

The subtractor operation mode represents the worst-case scenario since the flying capacitors are related to lower ideal frequencies compared to the adder operation mode. With a lower switching frequency, it is possible to guarantee the operation of the converter in both Adder and Subtractor modes. This worst-case scenario can be used to choose a value of capacitance for the flying capacitors that compose the Adder/Subtractor module. In order to achieve a capacitor value suitable for integration and with a slow switching frequency, we choose a capacitance of 12 pF, which corresponds to an ideal operating frequency of nearly 46 kHz.

The next step consists of sizing the flying capacitors of Doubler/Divider mod-

ule, considering the previously selected switching frequency. Since the values for flying capacitors of Adder/Subtractor converter were already defined, simulations varying the flying capacitors of the previous blocks can be done for calculating conversion system efficiency. Based on the relation of the amount of power/energy provided by the PV cell in the converter input, and the amount of power/energy used to charge the output load capacitor, it is possible to estimate, through electrical simulation, the conversion system charging efficiency η_{CS} as:

$$\eta_{CS} = E_{out}/E_{in} \tag{4.9}$$

Equation 4.9 is based on Eq. 4.7, and since the simulated charging efficiency considers the charging of the output load capacitor starting from 0 V, η_{CS} will be normalized by the maximum achievable efficiency of 50% as explained before. It is important to emphasize that the converter efficiency considered in this work is the charging efficiency concept previously presented. Since the application circuit operation is duty-cycled and consequently there is no load connected the entire time in the converter output, this efficiency is estimated considering only the load capacitor connected all the time in the converter output. And with that, we can get a sense of how much energy is lost only in the converter block when energy is transferred from the solar cell to the capacitor.

By manually adjusting the size of the flying capacitors of the voltage Doubler/Divider module and checking the correspondent η_{CS} efficiency, capacitor values that provided the best efficiency are 90 pF for the flying capacitors of blocks A and C, and 45 pF for the flying capacitors of blocks B and D.

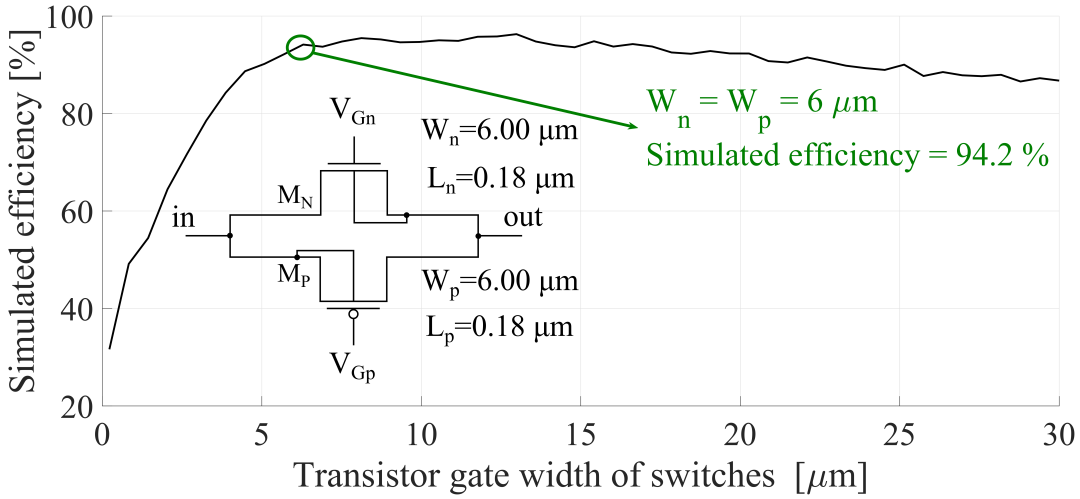
The size of switches can be varied to refine efficiency improvement. In this case, the gate length of the transistors that compose switches is fixed to a minimum size (180 nm in the target technology) and W is varied. In each simulation, the converter efficiency is obtained. Fig. 38 shows the relationship between converter efficiency and gate width of switches in a case where VCR = 1.25. It can be noticed that an improvement in the converter efficiency can be reached with the increasing of the gate width until a certain value. After this, the efficiency is reduced caused by the parasitic elements of the transistors. So, for this VCR scenario and considering only the charging efficiency of C_L, the best value for gate width for all switches which results maximum efficiency is 6 μm.

4.2 DESIGN METHOD INCLUDING CONVERTER R_{OUT} ESTIMATION

The proposed method can also include the estimation of the converter output resistance R_{out}. The output resistance is an important parameter of the converter that shows the limitations in terms of the application of this converter.

Once again, electrical simulations were performed using the Adder/Subtractor module working in adder and subtractor mode and varying the size of the flying capacitors

Figure 38 – Simulated conversion system efficiency η_{CS} in function of transistor gate width of switches.



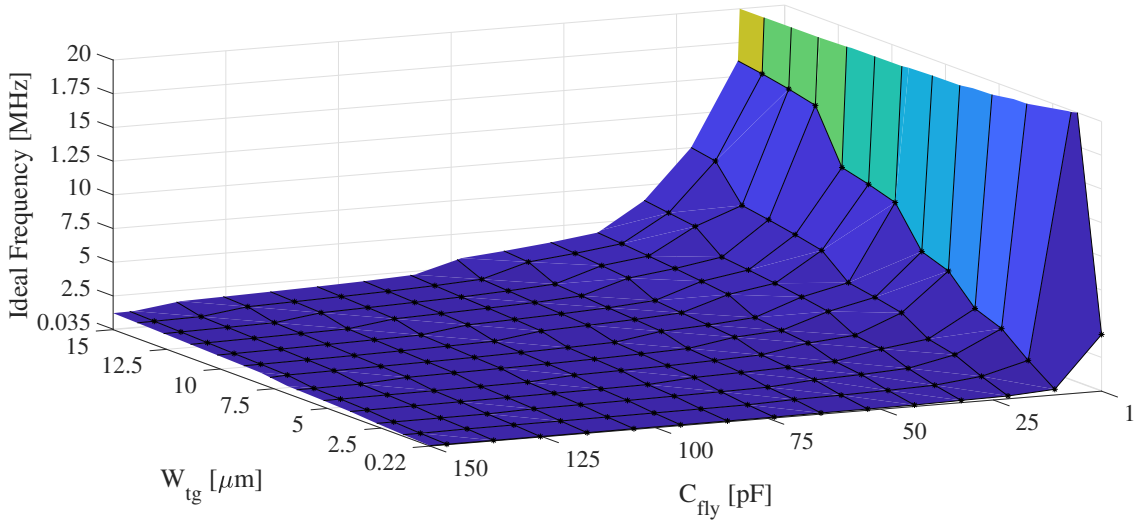
Source: Author

from 1 to 150 pF operating with the ideal switching frequency for each capacitor size. In these new simulations, switches gate width was varied from 0.22 to 15 μm. This simulation approach results in three-dimensional curves which relate flying capacitor size C_{fly} and switches gate width W_{tg} with the specifications for the ideal frequency, converter output resistance R_{out}, maximum voltage on the output load capacitor $V_{CL_{max}}$ and converter charging efficiency η_C. It was used as an output load capacitor C_L of 250 pF for both Adder/Subtractor operation modes.

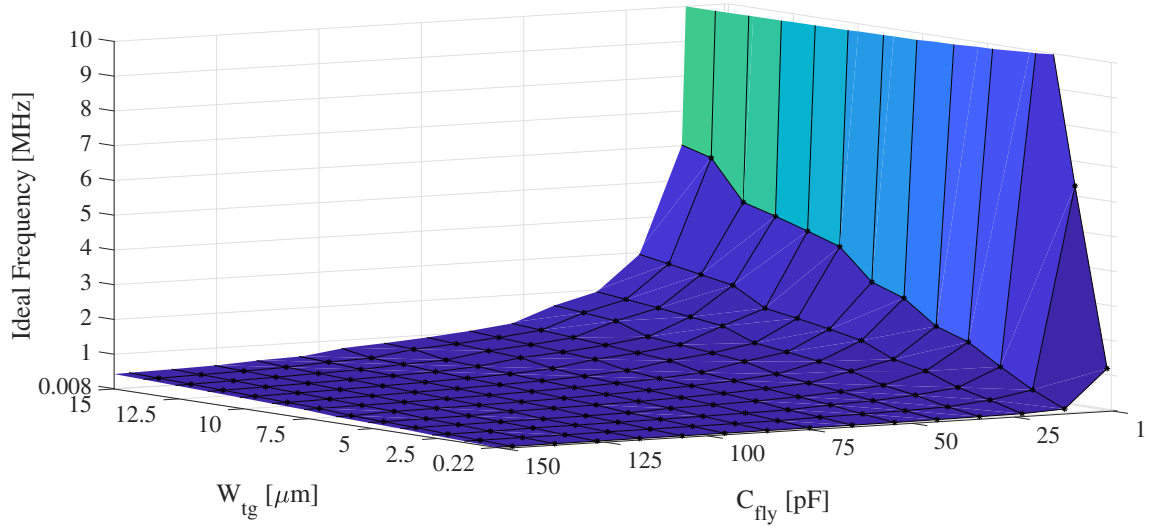
The adder operation mode is simulated using two ideal voltage sources of 0.2 V as inputs, and the subctrator operation mode is simulated using an ideal voltage source of 0.6 V in the first input and 0.2 V in the second input. Figure 39 presents the curve of the ideal frequency related to switches gate width and flying capacitor sizes for both operation modes. The trade-off shown before between capacitor size and switching frequency is also presented in these simulations. So, in order to use smaller flying capacitors, the converter must operate with higher switching frequencies that may cause more switching losses. Once again, subtractor mode is related to smaller frequencies when comparing with the adder mode. Also, the increase in the switches gate width does not cause a relevant variation in the ideal frequency for C_{fly} higher than 25 pF. For capacitors larger than this value, an increase in W_{tg} leads to a higher ideal frequency.

Figure 40 shows the curve of the converter output resistance R_{out} related with switches gate width and flying capacitor sizes for both operation modes. At a first glance, it seems that R_{out} does not vary with C_{fly} and this is because the ideal frequency is adjusted for each combination of C_{fly} and W_{tg}. The converter output resistance values are higher in the subtractor mode, but both operation modes present an equivalent R_{out} behavior.

Figure 39 – Ideal frequency versus switches gate width versus flying capacitor size for adder mode (a) and subtractor mode (b).



(a)



(b)

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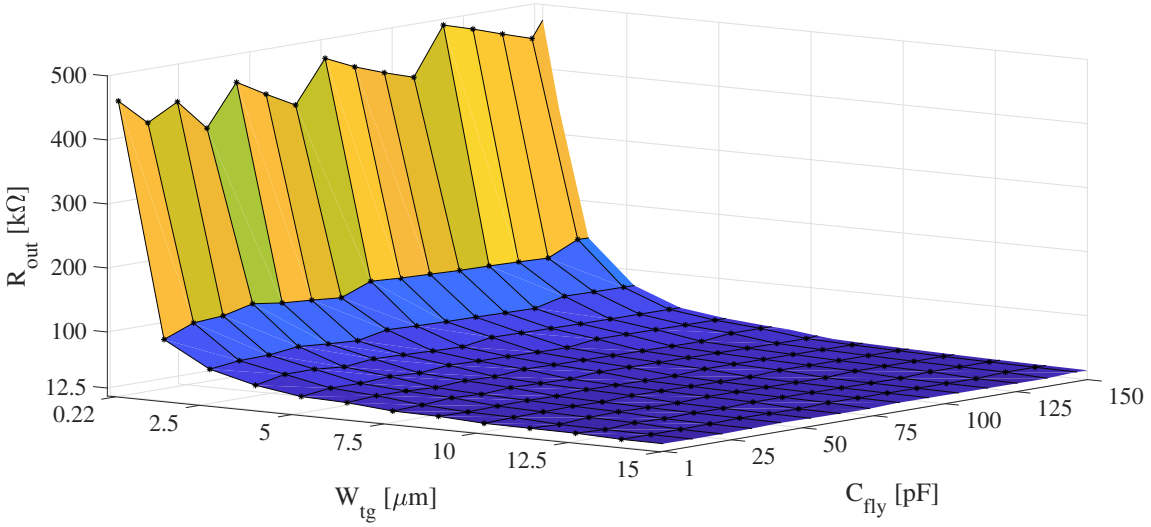
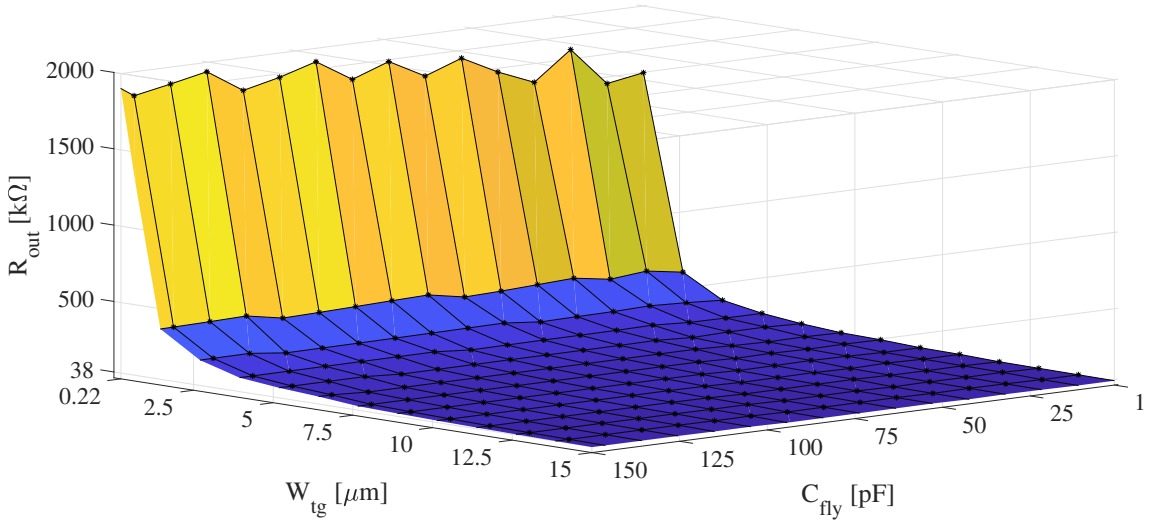
Figure 40 – Converter output resistance versus gate width versus flying capacitor size for adder mode (a) and subtractor mode (b).



(a)

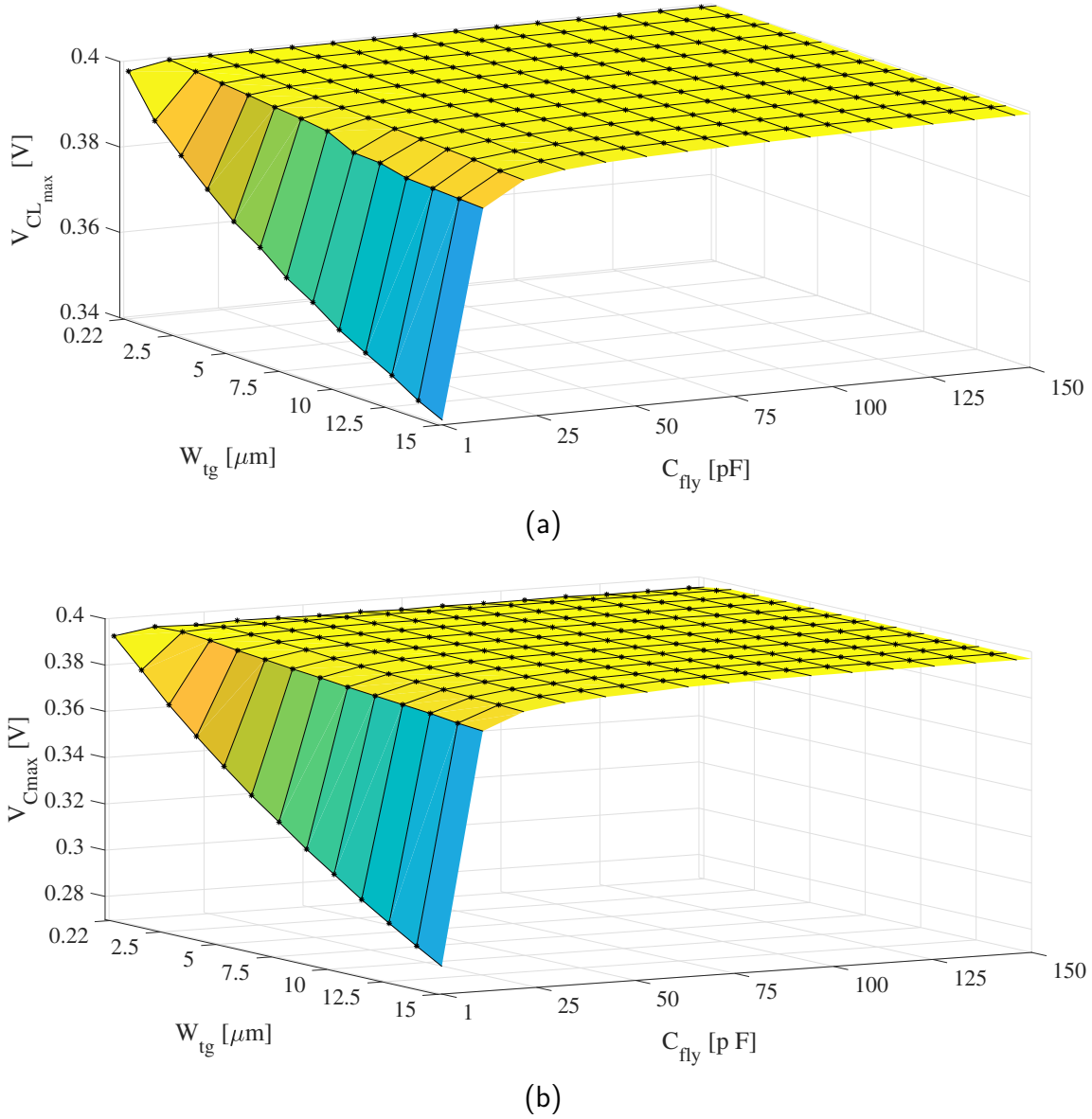


(b)

Source: Author

The maximum voltage on the output load capacitor related with switches gate width and flying capacitor sizes for both operation modes is presented in Fig. 41. Both operation Adder/Subtractor modes were adjusted in the simulation to provide an output voltage of 0.4 V to charge C_L. This is the maximum voltage on C_L in almost all C_{fly} and W_{tg} combinations. The maximum voltage on the output load capacitor becomes smaller than 0.4 V for small C_{fly} and when W_{tg} increases. This can be explained by the parasitic capacitance of the switch transistors that increase with the increasing in W_{tg}. When C_{fly} is small, these parasitic capacitance impact more in the converter operation.

Figure 41 – Maximum voltage in the output load capacitor versus gate width versus flying capacitor size for adder mode (a) and subtractor mode (b).

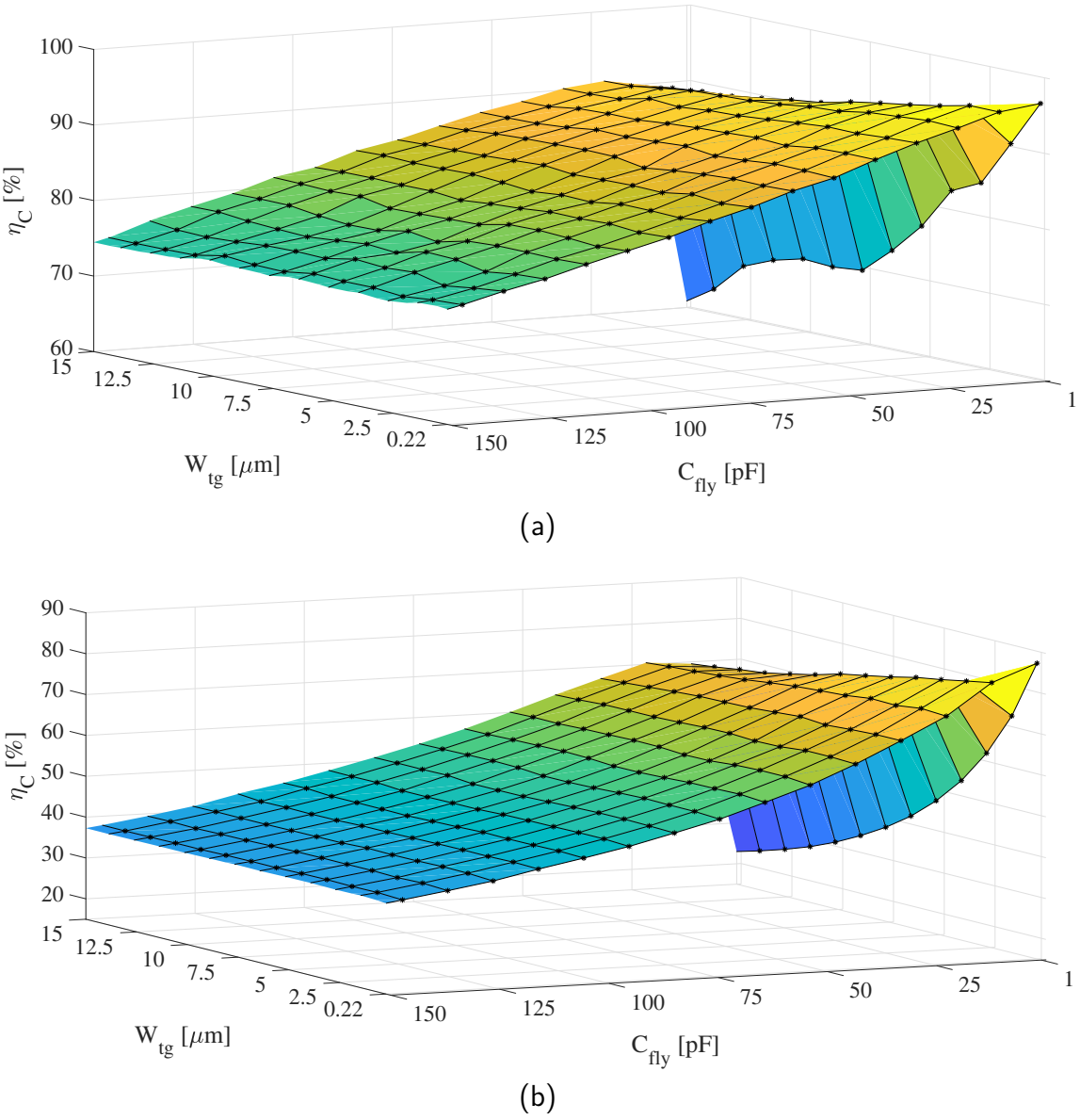


Source: Author

Finally, Fig. 42 presents the curve of the charging converter efficiency related to switches gate width and flying capacitor sizes for both operation modes. It is possible to

see that the charging efficiency depends more on the C_{fly} size in both operation modes. This efficiency increases when C_{fly} decreases, and this can be explained because larger capacitors require more time to charge, impacting on the charging efficiency. In terms of η_C, it is not advantageous to operate with a converter implemented with small C_{fly} and large switches.

Figure 42 – Converter charging efficiency versus gate width versus flying capacitor size for adder mode (a) and subtractor mode (b).



Source: Author

These simulated curves can be used to size all the proposed conversion system. As a practical example, a range can be delimited for C_{fly}, W_{tg}, and switching frequency in a way that there is some equivalence between the specifications in both Adder/Subtractor operation modes. Based on this delimited range it is possible to choose values for C_{fly}, W_{tg} and switching frequency, and then simulate the entire conversion system to verify the

specifications. In this new conversion system design, we delimited C_{fly} in the range 20 - 30 pF; W_{tg} in 3 - 7 μm; and the switching frequency in 1 - 10 MHz.

4.3 CONCLUSION

Details about the construction of the proposed DC-DC converter are addressed in this chapter. With that, it is possible to understand the decisions made about the implementation of the system components and the operation of the DC-DC converter. In addition, a systematic method based on electrical simulation is proposed to be a good starting tip for the conversion system design including the sizing of capacitors, switches, and switching frequency. The proposed method is practical and avoids the use of complex equations that model the entire conversion system.

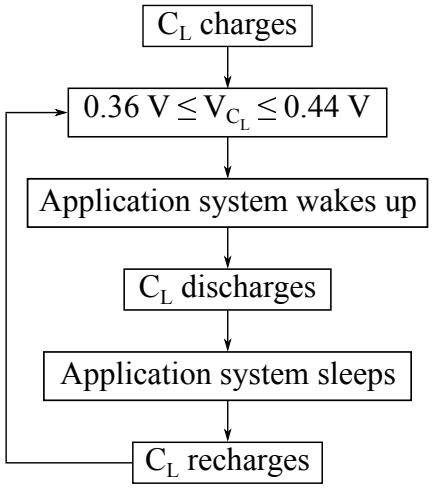
5 RESULTS AND COMPARISON WITH OTHER WORKS

In this chapter we present the simulation-based electrical characterization of the proposed DC-DC converter considering two different designs targeted to different applications. Each design considers the sizing of the converter components differently in order to fulfill the application constraints. A comparison of the proposed DC-DC converter with other DC-DC converters in the literature is also addressed in this chapter. Finally, we present an implementation suggestion for the complete energy harvesting system contemplating the interaction between all blocks.

5.1 SCHEMATIC SIMULATION RESULTS

The flowchart of Fig. 43 exemplifies the proposed converter system operation interacting with the application. It is important to note that the first step of the flowchart begins after the converter start-up, and the start-up solution is beyond the scope of this work. Then, after start-up, the output load capacitor C_L charges with a voltage in the range of 0.36 to 0.44 V (0.4± 10%). After that, the application system wakes up for a short period and C_L discharge ΔV providing the energy for the application circuit. The application system sleeps again for a much greater period of time and C_L recharge to the full voltage value. In this kind of approach, there is no constant resistive load connected all the time into the DC-DC converter output.

Figure 43 – Flowchart of the converter system operation interacting with the application.



Source: Author

5.1.1 DESIGN FOR LOW POWER CIRCUITS - DESIGN 1

The first design is intended to low power circuits such as the one composed of a sensor and a small memory processor. This design is performed using the first version of

the proposed method in Chapter 4. Recalling the method steps, the subtractor mode curve in Fig. 37 is used to start the conversion system design. Then, considering the trade-off between capacitor size and switching frequency we choose a design point where the flying capacitors of the Adder/Subtractor module were sized as 12 pF and the correspondent switching frequency for all switches was 46 kHz. By manually varying the size of the remaining flying capacitors it is possible to find the combination that generates the best efficiency. In this case, this combination was 45 pF for B and D modules, and 90 pF for A and C modules. In order to maximize converter efficiency and reduce chip area, all switches were sized with a minimum gate length and gate width equal to 6 μm.

With all parameters already sized, it is possible to simulate the entire conversion system. Then, the conversion system was configured with a VCR of 1.25 that best match the voltage provided by the target PV cell. In addition, it was used C_{in} and C_L equal to 1 nF each.

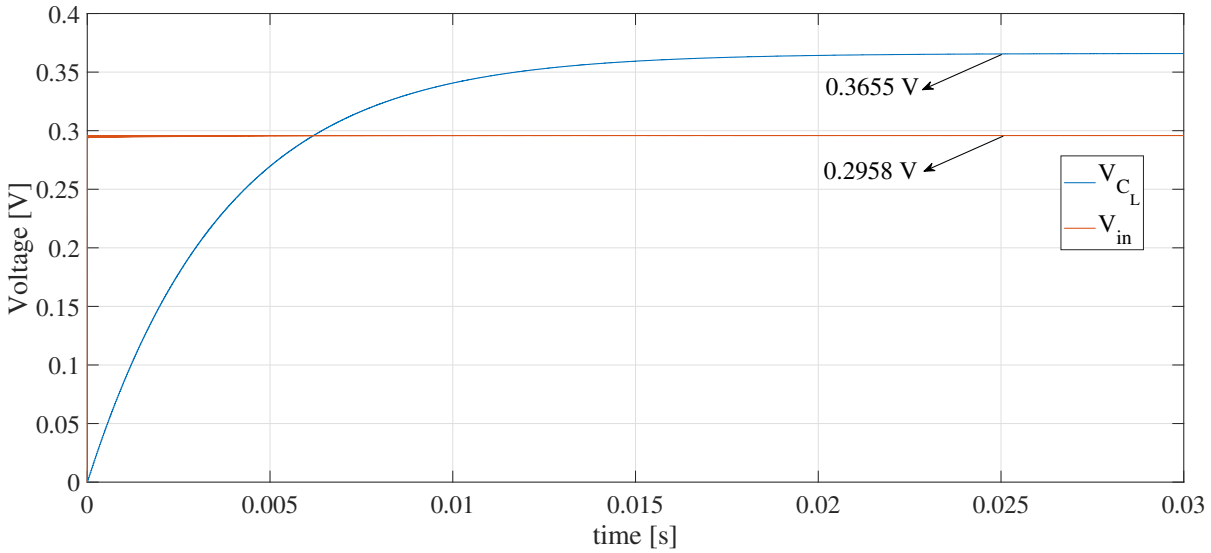
Figure 44 shows the conversion system output voltage charging C_L and the input voltage (V_{in}) provided by the PV cell. In this simulation it is possible to see the converter specifications such as converter output resistance R_{out}=3.77 MΩ, maximum voltage on the load capacitor $V_{CL_{max}}$=0.3655 V, and the converter charging efficiency η_{conv}=94.2 %. This charging efficiency is considering only the losses in the SC DC-DC converter charging the output load capacitor with no constant resistive load.

This DC-DC converter can be employed in a generic system composed of a sensor and small memory processor. This system wakes up for 100 μs to read and save the sensor value, then sleeps for 1 minute. To allow this operation it is required a maximum output converter resistance of 8.44 MΩ and a C_L of 17 nF.

Regarding the control part, the digital block was described in SistemVerilog hardware description language considering exactly the block diagram represented in Fig. 27. After testing and validating the logic operation of the digital block, a logic synthesis using Synopsys Design Compiler tool was performed in order to transform the SystemVerilog circuit description into a circuit built with standard cell logic gates. With this synthesis, it is possible to estimate the digital block power consumption and gate area. The nominal V_{DD} of the 180 nm node is 1.8 V and the results obtained with the logic synthesis are related to this nominal voltage. For this reason, the control block power consumption has to be estimated with a V_{DD}=0.8 V. Then, for this first design, the control block power consumption at V_{DD}=0.8 V is estimated in 277.88 nW, and the gate area is around 2322 μm^2. It is important to clarify that the operation of the control block composed of standard cell logic gates was note tested with the V_{DD}=0.8. The logic synthesis was performed to provide an insight into the control power consumption.

With that it is possible to perform a mixed-signal simulation in order to evaluate the interaction between the digital control block and the DC-DC converter. Figure 45 shows the converter output voltage starting from 0 V and varying over time for a varying

Figure 44 – Performance of the proposed DC-DC converter for the first design.



Source: Author

input voltage V_{in} = 0.32, 0.53 and 0.26 V (black line). This process is repeated for three cases: typical (TT) transistors and capacitors at 27^o C (green line); worst case fast (FF) transistors and capacitors at a low temperature of -40^o C (blue line); and worst case slow (SS) transistors and capacitors at a high temperature of 85^o C (red line). The low and high temperature values represent the industrial range.

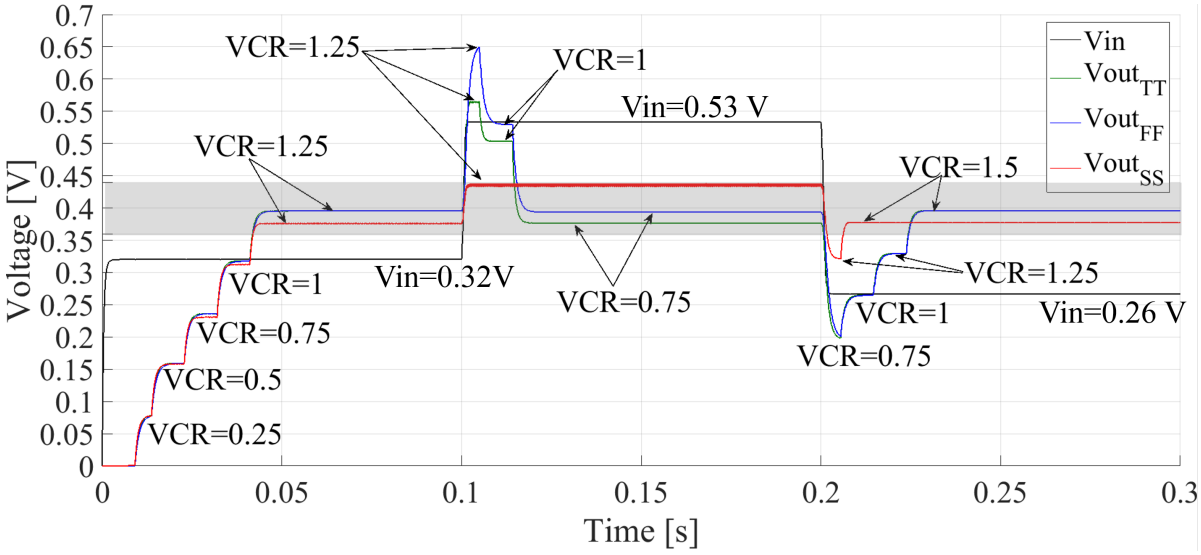
It is possible to notice the automatic reconfiguration of VCRs until V_{out} achieving a value inside the range 0.4 V $\pm\,\Delta$. As previously mentioned, Δ as defined as 10 % of the desired 0.4 V. We used ideal comparators for sensing V_{out} level and generating signals X_{up} and X_{down}, which are the inputs of the control module (Fig. 22 from Chapter 3).

Corners simulations presented the same functional behavior as the typical simulation, adjusting V_{out} into the desired range, with small variations in terms of delay. In the first case, when V_{in}=0.32, all three simulations were set up with a VCR equal to 1.25. The TT and FF simulations are overlapped and there is a small voltage discrepancy compared to SS simulation. When V_{in}=0.53, TT and FF simulations were set with a step-down VCR of 0.75, and SS simulation kept the same VCR as the first case. TT and FF simulations are close to each other and there is a large difference with respect to the SS simulation. In the last case, when V_{in}=0.26, all three simulations were set with a step-up VCR of 1.5. Once again, TT and FF simulation are overlapped.

5.1.2 DESIGN FOR LOW POWER CIRCUITS - DESIGN 2

The second converter design is targeted to a circuit with power dissipation of 1 μW and using as reference the package slot of the Bluetooth Low Energy (BLE) standard.

Figure 45 – Interaction between the digital control block and the first design of the DC-DC converter considering three different simulations.



Source: Author

This design is performed using the upgraded method presented in Chapter 4. The method provides delimited ranges for the converter parameters. In this case, the delimited ranges are: 20 - 30 pF for C_{fly}, 3 - 7 μm for W_{tg}, and 1 - 10 MHz for switching frequency. By choosing, in these ranges, C_{fly}=25 pF, W_{tg}=6 μm and switching frequency of 5 MHz, it is possible to simulate the entire conversion system to check converter performance.

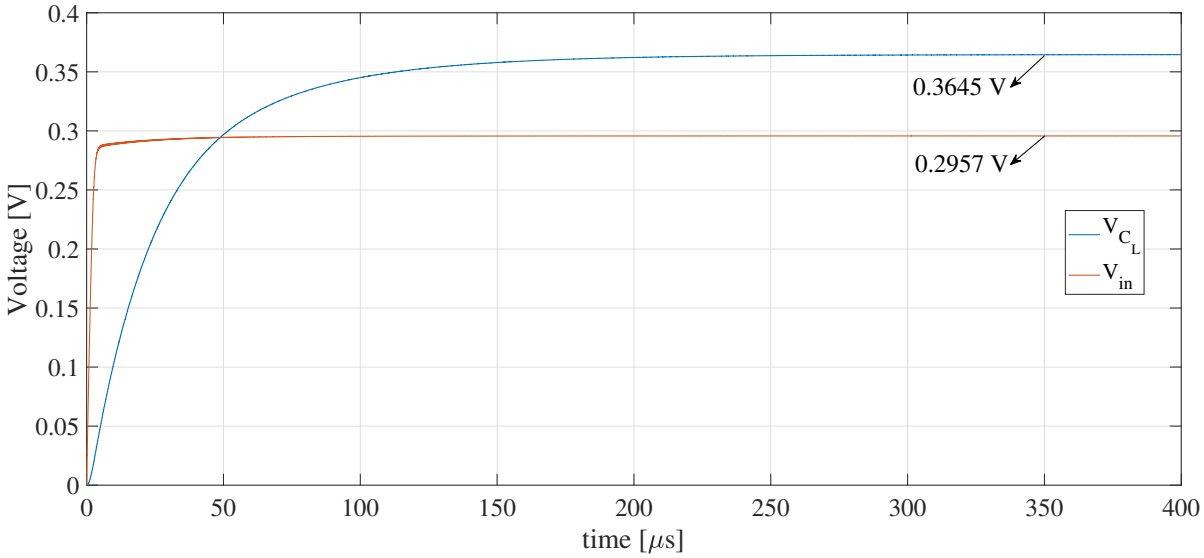
The conversion system configuration is the same as presented in the first design. In this new design, the converter output resistance R_{out} is 34.54 kΩ, maximum voltage on the load capacitor $V_{CL_{max}}$ is 0.3645 V, and the converter charging efficiency η_{conv} is 92.09%. This charging efficiency is considering only the losses in the SC DC-DC converter charging the output load capacitor with no constant resistive load. The curve for C_L charging with the voltage provided by the conversion system is presented on Fig. 46, and it is possible to note capacitor C_L charging with $V_{CL_{max}}$. This figure also presents the input voltage provided by the PV cell.

In order to use the proposed DC-DC converter using the package slot of the BLE standard, it is necessary to choose a communication scenario and estimate the required parameters. The BLE Link Layer has only one packet format used for both advertising channel packets and data channel packets, as shown in Fig. 47 (MICROCHIP..., 2020). According with this, we have:

$$Packet = 1 + 4 + 2 + D[0\ to\ 255] + 3 = 10 + D[0\ to\ 255]\ bytes$$

For example, if it is intended to transmit 2 bytes of information - D = 2 -, the

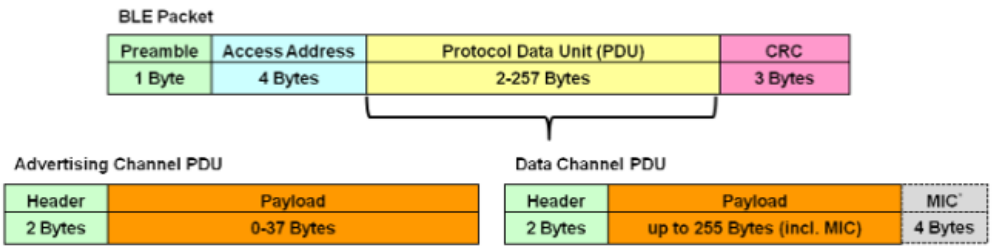
Figure 46 – Performance of the proposed DC-DC converter for the second design.



Source: Author

packet size is 12 bytes. Also, in the package slot the on time associated with that amount is T_{on}=100 μs, and the off time is T_{off} = 625 μs - 100 μs = 525 μs. T_{on} represents the time the application is awake and T_{off} represents the time the application is asleep. So, considering that C_L will charge with a voltage close to 0.4 V and considering that this capacitor will discharge ΔV=0.1 V, if the power dissipation during T_{on} is 1 μW, this scenario requires a converter output resistance that does not exceed 37.83 kΩ. This constraint makes possible for the DC-DC converter recharge C_L near to 0.4 V during the period T_{off}. In this case, a load capacitor of 2.17 nF could be used as C_L. Since the converter output resistance is 34.54 kΩ in the new design, it is feasible to use the proposed DC-DC converter in this application scenario.

Figure 47 – Top level BLE link layer packet.



Source: From (MICROCHIP..., 2020)

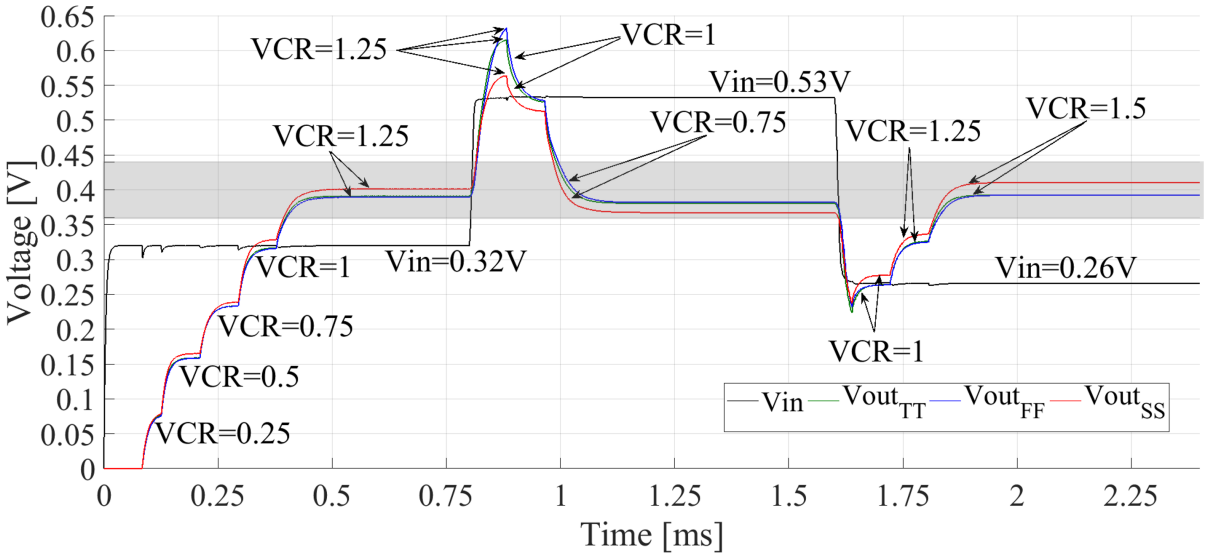
The logic synthesis of the control block for this new design was executed again since the switching frequency is different. Even though the gate area remains the same, the digital block power consumption is larger (25.18 μW). This happens because the switching

frequency is much higher than in the first design. This shows that the digital block must be optimized in terms of power consumption. In this work the control block is being used only to show the functionality of the proposed DC-DC converter, so the improvement of this digital block is part of a future work.

It is important to notice that in this new design the converter gate area is reduced from 0.282 to 0.125 mm^2, and the converter output resistance is also reduced from 3.77 M to 34.54 kΩ. By the other side, the switching frequency increases, causing additional losses in the control block. There is no major impact on the charging efficiency of the converter.

Once again, a mixed-signal simulation was executed in order to evaluate the interaction between the digital control block and the new design of the DC-DC converter. The simulations setups were the same as before and the curves are presented in Fig. 48. It is possible to observe the converter VCR adjusting so that the output voltage is within the desired voltage range. For the three cases of V_{in} all three simulations were set with the same VCR: 1.25, 0.75 and 1.5 for V_{in} equal to 0.32, 0.53 and 0.26 V, respectively. The voltage values were also very close for all simulations.

Figure 48 – Interaction between the digital control block and the second design of the DC-DC converter considering three different simulations.

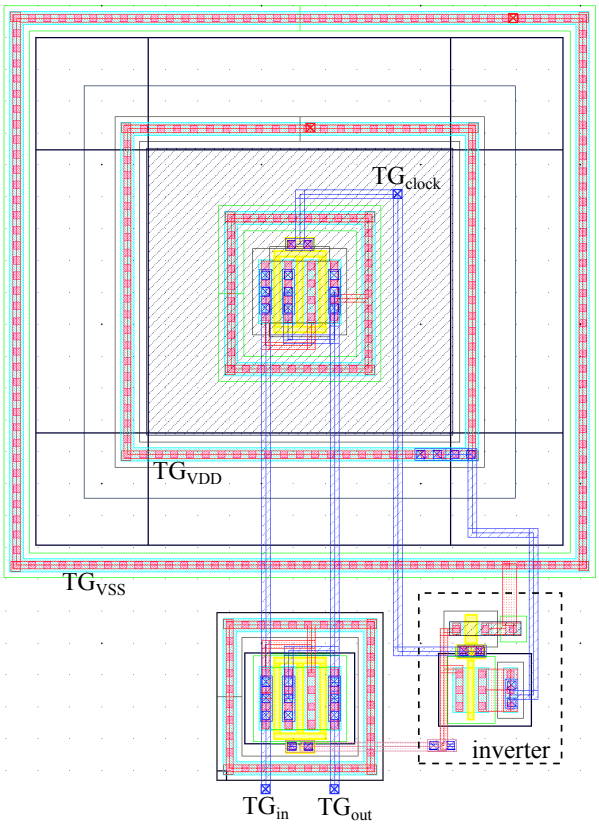


Source: Author

5.2 LAYOUT AND POST-LAYOUT SIMULATIONS

We chose the second design of the proposed converter to design its layout and validate its operation with post-layout simulations. The second design was chosen simply because the total flying capacitance and the associated converter R_{out} are smaller than the first design.

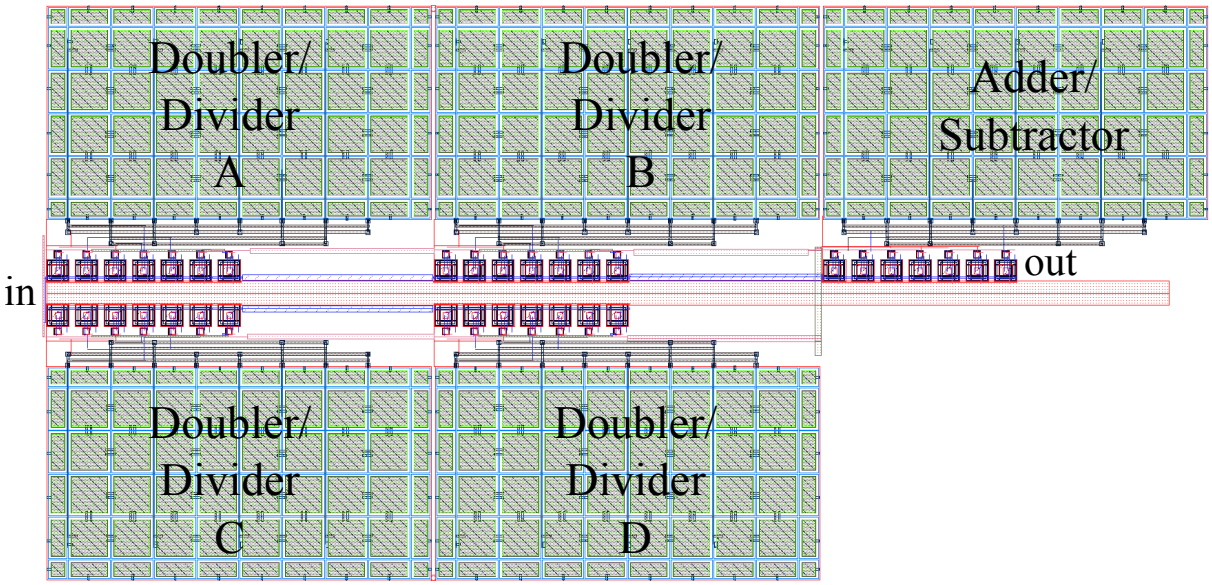
Figure 49 – Layout of the transmission gate switch that compose the proposed DC-DC converter.



Source: Author

The implementation of the transmission gate switches that compose the proposed DC-DC converter considers insulated bulks connected to the source terminals of N-type and P-type transistor. The layout of the switches was built using the deep N-well transistor model available in the TSMC 180 nm PDK. Figure 49 shows the layout of the transmission gate switch togheter with an inverter used to provide the complementary clock signal necessary for the operation of the switches.

Figure 50 – Layout of the proposed multiple-VCR SC DC-DC converter.



Source: Author

The converter modules that compose the multiple-VCR SC DC-DC converter have two flying capacitors of 25 pF each. In this case, a layout of two MiM capacitors using interdigitated and common centroid layout techniques was designed in order to have a good circuit matching. With the layout of the switch and the layout of the capacitors it is possible to design the layout of the multiple-VCR SC DC-DC converter.

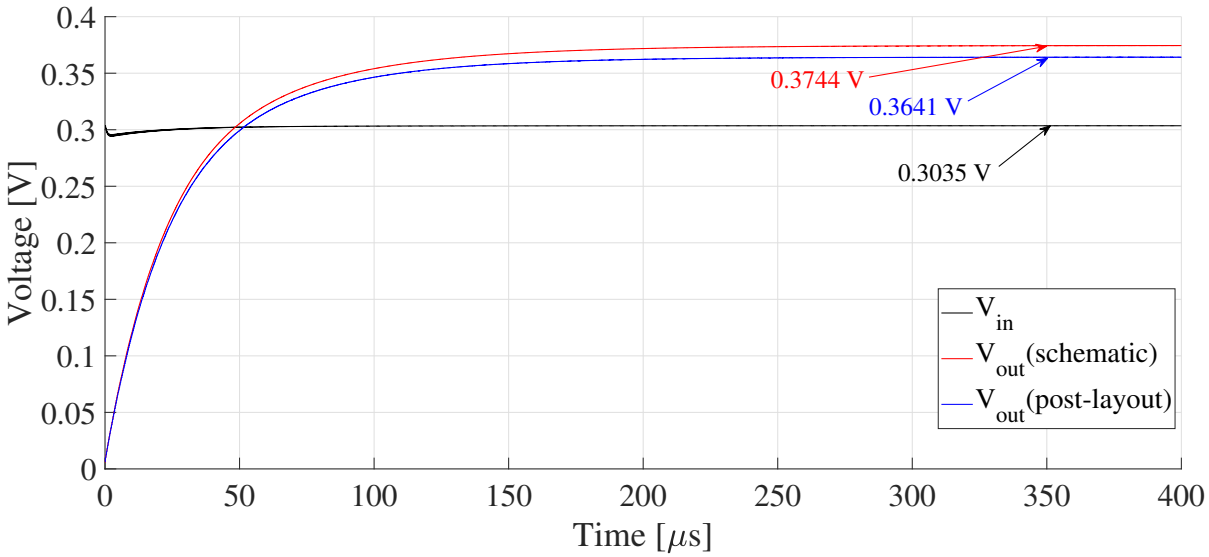
The layout of the multiple-VCR SC DC-DC converter, designed with Cadence tools, is shown in Fig. 50. The layout area is 452.26 μm x 916.38 μm, resulting in a total area of 0.4143 mm^2.

Figure 51 shows the post-layout simulation of the proposed DC-DC converter and the comparison with schematic simulation performance. This simulation was executed in Cadence Spectre with the same configuration of Figs. 44 and 46. It is possible to note that the converter output voltage curve in the post-layout simulation is very similar to the schematic simulation curve. The difference in the maximum voltage is only 10.3 mV, and this difference is due to the parasitic elements in the layout. In addition, the converter output resistance in the post-layout simulation is 32.43 kΩ and the converter charging efficiency is 90.78 %. This results are close to the schematic simulation results of 34.54 kΩ for R_{out} and 92.09 % for η_{conv}.

5.3 COMPARISON WITH OTHER WORKS

Table 6 presents a comparison with state-of-the-art DC-DC converters used in energy harvesting applications and implemented in a 180nm CMOS process. The proposed

Figure 51 – Post-layout simulation of the proposed DC-DC converter for the second design.



Source: Author

converter area is 0.414 mm^2, which is almost twice the area achieved in (Chen et al., 2019) - which also uses SC approach - but smaller than the others. The advantage is the implementation of more options of VCRs (19 against 4). The peak efficiency of 90.78 % is greater than the others, but this value is for the converter core only, not considering losses in the digital control module. Our approach achieves comparable performance even to not fully integrated converters in terms of input/output voltage ranges and operating frequency, while using artificial light as energy source.

Table 6 – Comparison with state-of-the-art harvesters DC-DC converters.

	This work	(YU et al., 2018)	(Cao et al., 2019)	(Chen et al., 2019)	(Bose; Anand; Johnston, 2019)
Technology	180 nm	180 nm	180 nm	180 nm	180 nm
Topology	SC based converter	Boost	Boost/Flyback	SC based converter	Boost
Energy source	Artificial light	Thermoelectric	Thermoelectric	Piezoelectric	Thermoelectric
Output voltage	0.4 V	1.0 - 1.6 V	0.8 V	1 and 2 V	N/A
Input voltage	0.05 - 1.60 V	50 - 300 mV	50 - 300 mV	N/A	50 - 100 mV
Number of VCRs	19	N/A	N/A	4	N/A
Converter peak efficiency	90.78 % (post-layout simulation)	60 %*	84 %*	N/A	47 %*
Fully integrated	Yes	No	No	Yes	No
Converter area	0.414 mm^2	0.549 mm^{2**}	1.625 mm^{2**}	0.200 mm^{2**}	0.96 mm^{2**}
Operating frequency	5 MHz	N/A	N/A	200 Hz	25 kHz

*: measured; **: chip area.

Source: Author

Table 7 – Comparison with indoor light harvesters DC-DC converters.

	This work	(JUNG et al., 2014)	(Liu et al., 2016)	(Mondal; Paily, 2017)
Technology	180 nm	180 nm	180 nm	180 nm
Topology	SC based converter	SC based converter	SC based converter	Capacitive boost converter
Energy transducer	PV cell	PV cell	PV cell and TEG	PV cell
Output voltage	0.4 V	2.2 - 5.2 V	3.3 V	1.0 V
Input voltage	0.05 - 1.60 V	0.14 - 0.50 V	0.45 - 3 V	0.39 - 0.43 V
Number of VCRs	19	15 (9x to 23x)	14 (only step-up)	1 (fixed)
Converter peak efficiency	90.78 % (post-layout simulation)	75.0 % (measured)	89.0 % (measured)	82.4 %*
Fully integrated	Yes	Yes	Yes	Yes
Converter area	0.414 mm^2	0.550 mm^{2}**	0.570 mm^{2}**	0.430 mm^{2}**
Switching frequency	5 MHz	70 Hz - 19 MHz	20 kHz - 1 MHz	17 - 23 MHz

TEG: Thermoelectric Generator; *: measured entire system efficiency; **: estimated from layout image.

Source: Author

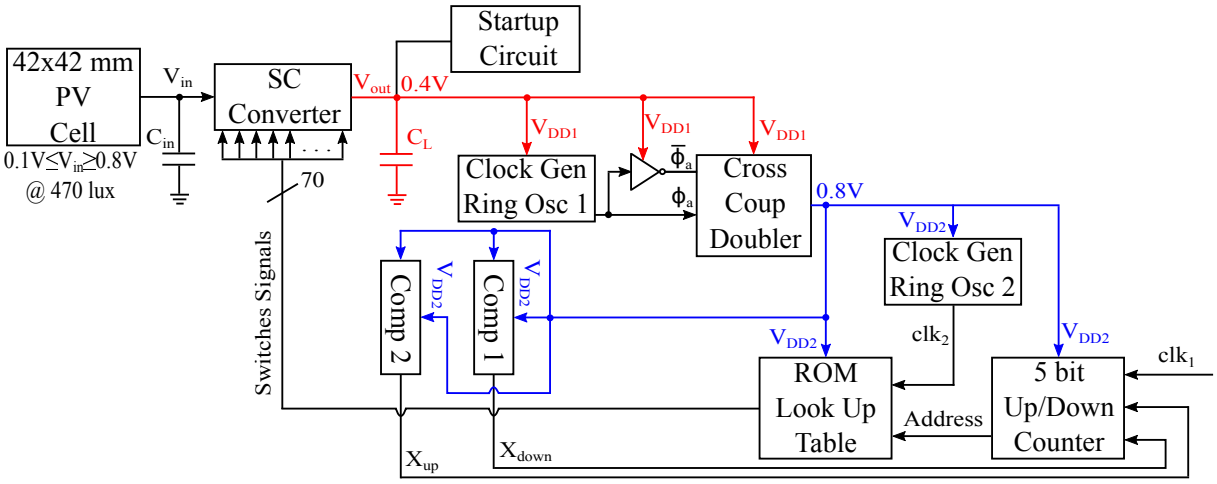
Table 7 presents a performance comparison of our work with other DC-DC converters for light energy harvesting applications in 180 nm technology node described in the literature. Our work presents 19 different VCRs, including fractional, integers, step-down and step-up configurations. In comparison, (JUNG et al., 2014) presents a converter with 15 step-up integers VCRs, (Liu et al., 2016) presents 14 different VCRs (some of them are fractional but all elevators) and (Mondal; Paily, 2017) presents a fixed voltage conversion ratio. The peak efficiency around 90.78 % achieved in our work is greater than the others, but this value does not consider losses in the digital control module. In this same scope, (Liu et al., 2016) presents a measured peak efficiency of 89 %. Other advantages of our approach are the broad input voltage range, the fixed switching frequency and the smaller converter area.

5.4 HARVESTING SYSTEM IMPLEMENTATION

A suggestion, in a block diagram, of implementation for the complete energy harvesting system is shown in Fig. 52. This proposed diagram includes all blocks necessary for the system operation. It is important to emphasize that the focus of this work is on proposing, designing, and validating the operation of the SC converter block which represents the DC-DC converter. The design and validation of the remaining blocks must be done in future work.

Since the proposed SC DC-DC converter does not work at cold start, a startup strategy is needed when C_L is initially discharged and the converter output voltage V_{out} is 0 V. The converter depends on the switches signals to start working, but the switches signals are only generated when C_L is charged. This startup circuit can be integrated with the energy harvesting chip or can be external. A simple solution for a startup could be an off-chip Li-battery and an undervoltage-lockout (UVLO) circuit used only to pre-charge C_L.

Figure 52 – Block diagram of the complete energy harvesting system.



Source: Author

In steady-state, when C_L is charged with 0.4 V (o near to it), this voltage is also used as V_{DD1} to supply the first clock generator. The clock generator could be a ring oscillator based implementation, for example. This block generates a ϕ_a pulsed signal which is also inverted ($\bar{\phi_a}$). Both signals are used with V_{DD1} in the cross-coupled doubler circuit to double V_{DD1}. This new doubled voltage is the V_{DD2} used to supply the remaining blocks. One of them is the second clock generator that generates clk_2 signal configured with the switching frequency to turn on and off the switches.

The cross-coupled doubler output voltage is used to supply the comparators, Comp 1 and Comp 2, as well as their inputs. Each comparator generates a bit that indicates whether the voltage is within the desired range or not. These bits are used in the digital control to maintain, increase, or decrease the DC-DC converter VCR. The blocks that compose the digital control, discussed in details in Chapter 3, are also supplied by V_{DD2}. The 5-bit counter receives the comparators bits and clk_1 which can be an external signal used to control the speed at which the counter executes each step. This counter sends a 5 bit address that, together with V_{DD2}, are the lookup table inputs. Finally, the lookup table provides the switches signals for each converter VCR.

5.5 CONCLUSION

The results of the proposed DC-DC converter electrical schematic are presented in this chapter. We considered two different designs for two different applications showing a good versatility of the proposed converter. Layout and post-layout simulations were also addressed and indicating that the post-layout converter performance is close to its schematic performance. The proposed DC-DC converter was compared with other state-

of-the-art DC-DC converters and it can be identified that the converter proposed by this work is competitive and promising for integration. Finally, it was given a suggestion for the complete energy harvesting system implementation, contemplating the interaction between all the blocks responsible for the functioning of the harvesting system.

6 CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORKS

6.1 CONCLUSIONS

Various topologies of DC-DC converters can be used in applications ranging from generating variable voltage supply for system-on-a-chip to energy harvesting systems. Energy harvesting is a promissing alternative to harness energy from the environment by using natural energy sources as solar, thermal, vibration, and ambient radio-frequency. Inductive and capacitive types of converters are widely used as the main topology. However, complete single-chip integration is easier to be reached using capacitive converters. The majority of the conversion systems focused on energy harvesting, mainly for indoor lighting, presented at least one energy storage element, such as a rechargeable battery, in their topology structures. Since capacitive converters are limited in terms of adjustment of the voltage conversion ratio, reconfigurable topologies must be explored in order to provide a capacitive based conversion system with different VCRs.

After the study and electrical characterization of the PV cells, it was noticed that the operation with lower voltages is advantageous to provide higher power. The maximum obtained power of a small PV cell operating indoor only with artificial light is limited to some dozens of μW.

A novel topology of a reconfigurable DC-DC converter based on a switched-capacitor was proposed for indoor PV cell energy harvesters. The conversion system is fully integrated and digitally adjustable, capable of providing 19 different VCRs, including step-down, step-up, fractional and integers conversion ratios. It is based on four Divider/Doubler modules and one Adder/Subtractor module arranged to offer VCRs from 0.25 to 8.

It was demonstrated that using only basic switched-capacitor topologies it is possible to obtain a conversion system capable of providing a range of various voltage conversion ratios. Also, the proposed system can be easily expanded to get other combinations of VCRs.

It was also proposed a systematic simulation-based method suitable to design the DC-DC converter including the sizing of internal flying capacitors, switches, and switching frequency. With this approach, it was not necessary to use complex models to design the switched capacitor converter modules. The proposed method was also upgraded to include the estimation of the converter output resistance. With these methods, it was possible to obtain two different design versions of the DC-DC converter aimed at two distinct applications.

Post-layout results demonstrate that it is possible to achieve a conversion efficiency of 90.78% for an output voltage around 0.4 V. Our results have also shown to be promising and competitive in terms of input voltage range and converter area in comparison to other works described in the literature. This DC-DC converter can be applied for an ultra-low-voltage sensor node system.

6.2 FUTURE WORK

The following suggestions for continuing this work are proposed here:

Improvement in the design of the digital control block in order to reduce its power consumption. Also, a physical synthesis of this digital control is needed to integrate it on chip.

Design, implementation and testing of the cross-coupled doubler circuit which is responsible for doubling the DC-DC converter output voltage to supply the control block.

Design and implementation of the clock generators, both for the cross-coupled doubler circuit, and for turning on and off the converter switches.

Proposal, design and implementation of the comparators responsible for sensing if the converter output voltage is within, below or above the desired range.

Proposal of a start-up method responsible for charging the output load capacitor, or just generating initial sufficient energy capable of waking the system so that it can operate on its own.

Complete integration of the entire energy harvesting system blocks in order to validate its functionality. For a second version of the energy harvesting system it could be employed a maximum power point tracking circuit to perform the matching between the PV cell and the DC-DC converter, and with that, be able to extract the maximum PV cell power to improve the overall energy harvesting system efficiency.

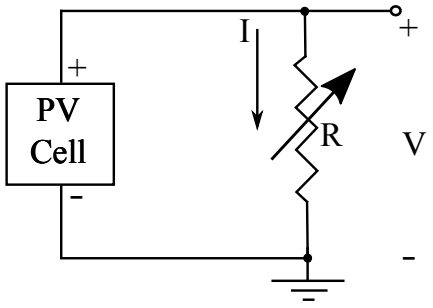
Appendix

APPENDIX A – ELECTRICAL CHARACTERIZATION OF PHOTOVOLTAIC CELLS

This appendix presents a practical and systematic method for photovoltaic cell electrical characterization operating indoor. A characterization example of two low cost photovoltaic (PV) cells is performed, and consequently, curves that represent the electrical behavior of the cells are obtained. Hence, an understanding about PV cells operation capacity when just artificial lighting is employed. Also, some examples of scenarios on variations in PV cells operation are given, as well as some hypothetical voltage conversion ratios for each case.

A very simple way to characterize a photovoltaic cell is connecting it in parallel with a variable resistor, as depicted in Fig. 53.

Figure 53 – Simple PV cell characterization circuit.



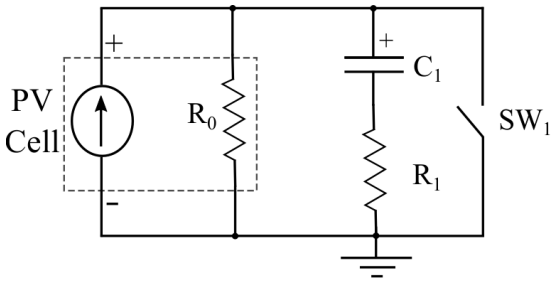
Source: Author

A voltmeter is necessary to measure the variable resistor voltage drop, and this measure represents the PV cell output voltage. In order to obtain the PV cell output current, an ammeter can be connected in series with the variable resistor. This way, varying the resistor, it is possible to measure directly the output voltage and current of the PV cell. This approach presents a problem, for indoor conditions, where the PV cell output values are very low compared to the outdoor condition, the ammeter internal resistance can affect the measurements.

One way to mitigate this problem is using an ohmmeter to measure the resistance that is being varied whit the variable resistor. With the resistance value and the voltage drop, the current can be simply calculated by Ohm's law. There is also a problem with this approach, when the resistance is adjusted, the variable resistor must be disconnected from the circuit in order to measure its resistance using the ohmmeter and connected again. It consists in a laborious process and almost impossible to perform if several measurements need to be executed.

A more elaborated circuit can be used to solve all these problems, the circuit depicted in Fig. 54 can be used to facilitate and expedite the PV cell characterization process (APOSTOLOU; VERWAAL; REINDERS, 2014).

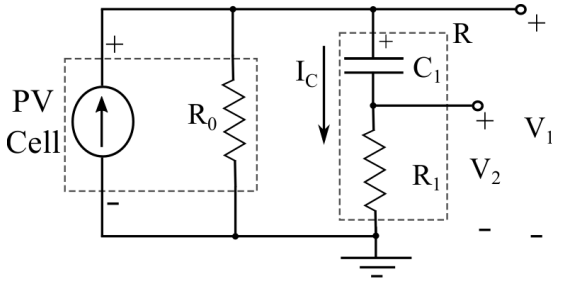
Figure 54 – PV cell characterization circuit.



Source: Author

Fig. 55 presents the equivalent circuit when the switch SW_1 is opened.

Figure 55 – PV cell equivalent characterization circuit for the capacitor charging phase.



Source: Author

This circuit emulate the variable resistor by using the charging of a capacitor which in DC can vary from a short circuit to an open circuit, that is, $R_{C1_{DC}} = \infty - 0\ \Omega$. There is a resistor R_1 in series with the capacitor C_1, so the equivalent resistance variation will range from ∞ to $R_1\ \Omega$:

$$R = R_1 + \frac{V_C}{I_C} \tag{A.1}$$

With the aid of an oscilloscope the curves of the voltages V_1 and V_2 can be obtained. The current I_C and the voltage V_C can be obtained by the following relations:

$$I_C = \frac{V_2}{R_1} \tag{A.2}$$

$$V_C = V_1 - V_2 \tag{A.3}$$

Using V_1 and I_C that represents the PV cell output voltage and current, respectively, the PV cell output power P can be calculated by simply multiplying V_1 by I_C.

The equivalent resistance variation can be obtained by substituting Eq. A.2 and A.3 in Eq. A.1:

$$R = R_1 + \frac{V_1 - V_2}{\frac{V_2}{R_1}} \tag{A.4}$$

Rearranging the terms in order to simplify Eq. A.4, the following relation can be obtained:

$$R = R1 \cdot \frac{V_1}{V_2} \tag{A.5}$$

Relating the resistance variation and the PV cell output power in one graph, R x P, we can discover which value of resistance provide the maximum output power. Through the maximum power transfer theorem we can find the PV cell internal resistance R_0 simply by matching it with the resistance that provides the maximum output power: $R_0 = R_{Pmax}$.

As an experiment example, the PV cell characterization was performed at night in the university research room which is illuminated by an arrangement of six luminaries containing two 32 W tubular fluorescent lamps each.

The flat surface of the test bench where the tests were performed is about 1.7m away from the luminaries.

A capacitor of 69μ F was used for C_1 and the series resistor R_1 was 1 kΩ, this value was chosen so that the $V2$ voltage drop could be easily identified by the oscilloscope resolution. The constant R_1C_1 must be adjusted depending on the PV cell to be characterized and the illuminance level employed.

Two distinct PV cell were tested, a 42x42 mm and a 45x45 mm PV cell depicted in Fig. 56. As well their parallel and series combinations.

Figure 56 – Chosen PV cells for electrical characterization.

Source: Author

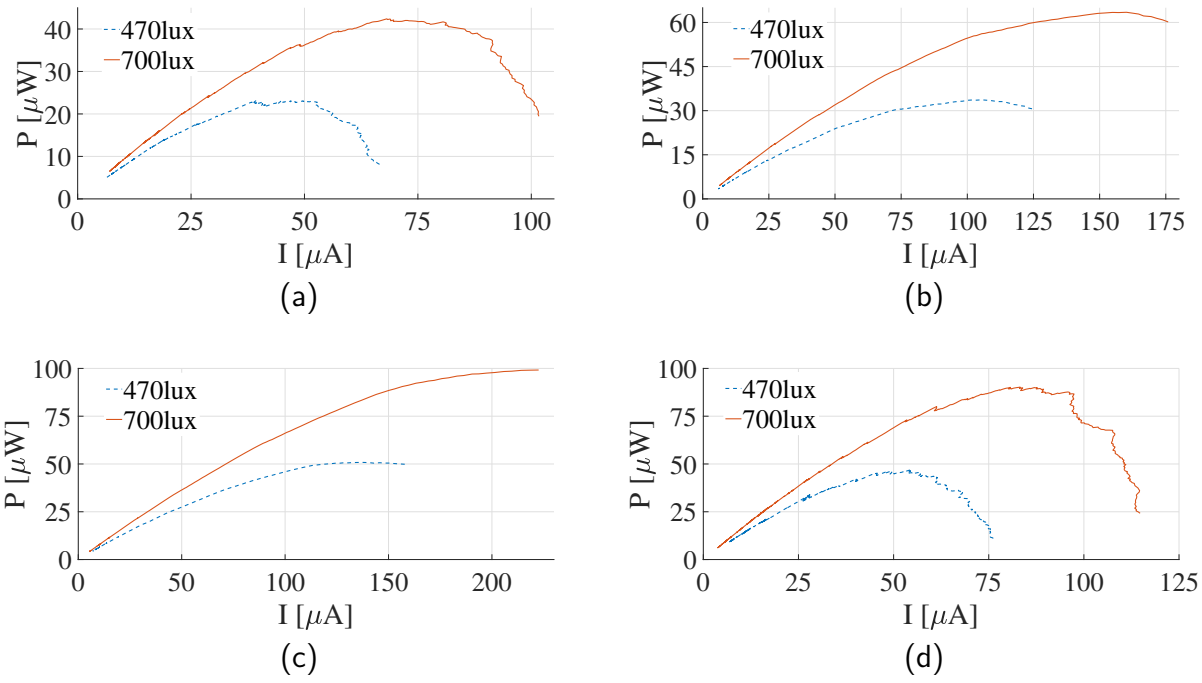
According to (CIE, 2002) the illuminance in offices must range from 200 to 750 lux, depending on the task. For example, a minimum illuminance of 200 lux is required for archives storage and a minimum illuminance of 750 lux is required for technical drawing.

Two illuminance levels were applied in the tests, an intensity of 470 lux obtained at the test bench level and an intensity of 700 lux that was obtained approximating the PV cell to the luminaries.

The curves obtained with the PV cell characterization were IxP, VxI, RxP and VxP. The tests were performed with a single 42x42 mm PV cell, a single 45x45 mm PV cell, their parallel connection and series connection. So, there are 16 curves in total.

Figure 57 shows the IxP curves for the single 42x42 mm PV cell, single 45x45 mm PV cell, PV cells parallel connection and PV cells series connection. For Figs. 57(a) and 57(d) there is a complete quadratic relation between current and power. While for Figs. 58b and 57(c), power increases linearly with the current until it saturates and reaches a maximum value. Observing Fig. 57(a) it can be noted that the maximum obtained power is around 23 μW and its correspondent current is about 47 μA for a 470 lux of illuminance, for 700 lux the maximum power is around 42 μW with 69 μA of current. In Fig. 57(b) the maximum power for 470 lux is around 33.5μ W with a current of 102μ A, and for 700 lux is about 63.5μ W with a current of 160.1μ A. For both tested cells, the obtained power almost doubled with an increase of approximately 50% in the illuminance level. As it can be noted in Fig. 57(c), with the PV cells parallel connection, the maximum obtained power increased to 50.5μ W with a current of 125μ A for 470 lux, and to 99 μW with a current of 225.5μ A for 700 lux. The series connection maximum obtained power is around 54.5μ W with 47μ A of current for 470 lux, and 90μ W with 83μ A of current for 700 lux.

Figure 57 – IxP curve for: Single 42x42 mm PV cell (a), Single 45x45 mm PV cell (b), PV cells parallel connection (c), and PV cells series connection (d).

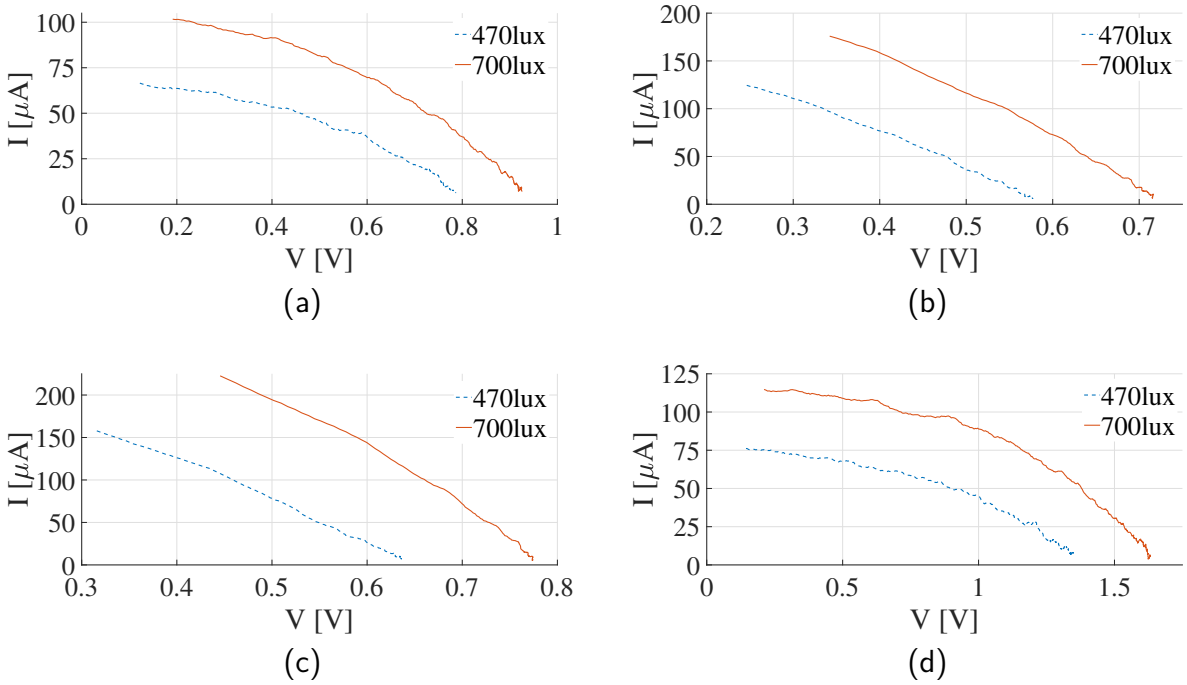


Source: Author

Figure 58 shows the VxI curves for the single 42x42 mm PV cell, single 45x45 mm PV cell, PV cells parallel connection and PV cells series connection. It can be noted

in all curves that there is a linear relation between the voltages and currents of the tested PV cells. In Fig. 58(b), 58(c) this linear relationship is more accentuated.

Figure 58 – VxI curve for: Single 42x42 mm PV cell (a), Single 45x45 mm PV cell (b), PV cells parallel connection (c), and PV cells series connection (d).

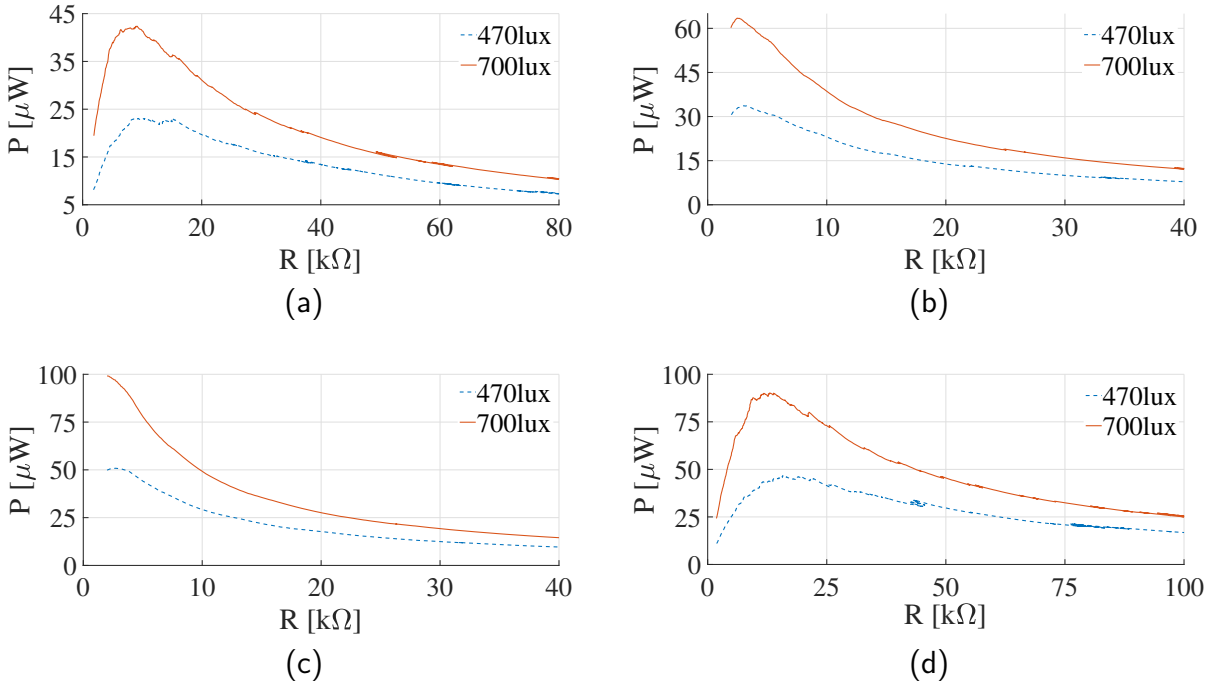


Source: Author

Figure 59 presents the RxP curves for the single 42x42 mm PV cell, single 45x45 mm PV cell, PV cells parallel connection and PV cells series connection. As expected, the curves show that the power starts at a lower value, increases with the resistance increasing, reaches a maximum value and then decreases. The PV cell internal resistance can be estimated through this maximum power point. Observing Fig. 59(a), for the single 42x42 mm PV cell the maximum power in 470 lux is around 23μ W with the correspondent resistance about 10k Ω, in 700 lux is 42μ W with a 9.5k Ω correspondent resistance. The single 45x45 mm PV cell maximum power in Fig. 59(b) is nearly 33.5μ W with a 2.8k Ω correspondent resistance for 470 lux, and for 700 lux, the maximum power is close to 63.5μ W with a 2.5k Ω correspondent resistance. Analyzing Fig. 59(c) it can be noted that for the parallel connection of the PV cells the maximum power is near to 51μ W with the correspondent resistance around 2.7k Ω in 470 lux. For 700 lux illuminance level, RxP curve did not behave in the same way as the others, the power increasing followed by a decreasing over resistance can not be observed in this curve. But the maximum power of the PV cells parallel connection was already presented, its value is around 99μ W and the correspondent resistance is close to 2k Ω. Regarding the PV cells series connection, it can be noticed in Fig. 59(d) that the maximum power for 470 lux is nearly 47μ W with a 16k

Ω correspondent resistance, and for 700 lux the maximum power is close to 90μ W with a correspondent resistance approximately of 14k Ω. The PV cells series connection presents a equivalent resistance which differs from the sum of the PV cells single resistances. Lastly, it can be also observed that the resistance of the same cell may change slightly with the illuminance level variation.

Figure 59 – RxP curve for: Single 42x42 mm PV cell (a), Single 45x45 mm PV cell (b), PV cells parallel connection (c), and PV cells series connection (d).

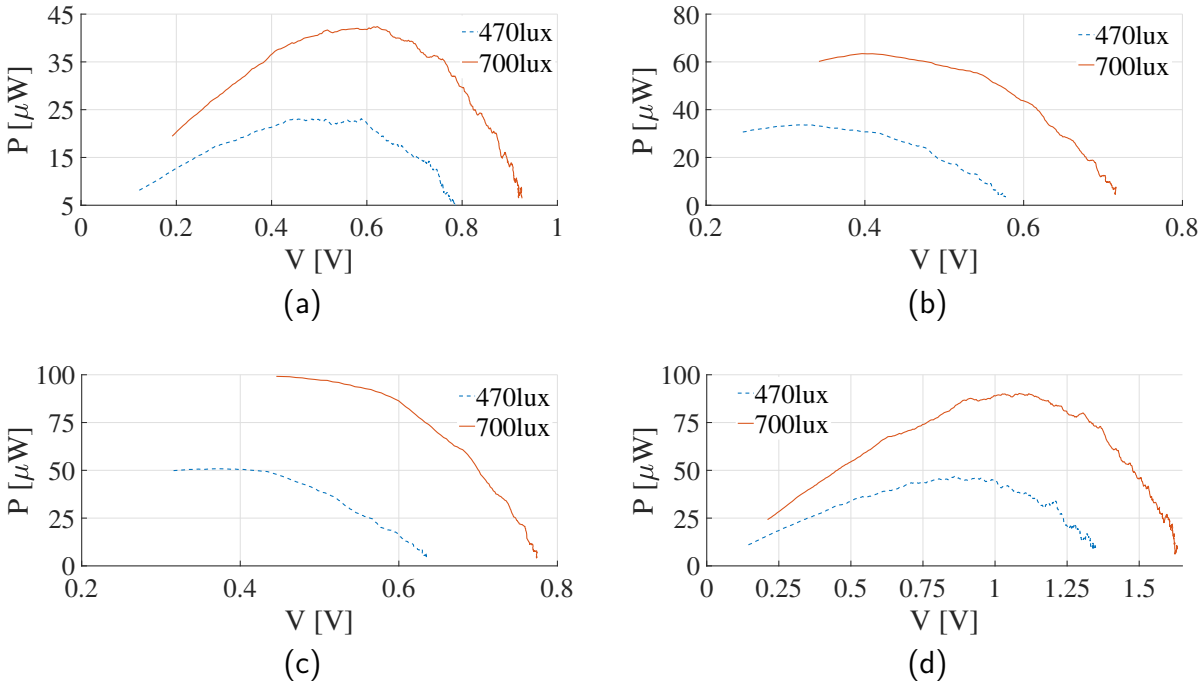


Source: Author

Figure 60 presents the VxP curves for the single 42x42 mm PV cell, single 45x45 mm PV cell, PV cells parallel connection and PV cells series connection. The curves present a quadratic relation between PV cells voltage and power, but in Fig. 60(c) this characteristic is not so visibly exposed. Observing Fig. 60(a), it can be noted that the 42x42 mm PV cell voltage for the maximum power is around 0.59 V in 470 lux and close to 0.6 V in 700 lux. For the 45x45 mm PV cell the correspondent voltage for the maximum power is nearly 0.33 V in 470 lux and about 0.39 V in 700 lux. The correspondent voltage for the PV cells parallel connection maximum power is approximately 0.37 V in 470 lux and almost 0.45 V in 700 lux. Regarding the PV cell series connection, the correspondent voltage for the maximum power is near to 0.93 V and around 1 V in 470 lux and 700 lux, respectively. It is interesting to note that, disregarding the configuration in series, all the other cases presented a maximum obtained power with correspondent voltages until 0.6 V, and low voltage applications may benefit greatly from this characteristic.

The PV cells characterization also showed that the maximum extracted power can

Figure 60 – VxP curve for: Single 42x42 mm PV cell (a), Single 45x45 mm PV cell (b), PV cells parallel connection (c), and PV cells series connection (d).



Source: Author

be increasing by connecting the PV cells in parallel or in series. If more current is needed, so a series connection is more appropriate. On the other hand, a parallel connection is more adequate for providing a higher voltage.

Taking into account the maximum obtained power for the PV cells, their power density can be estimated. For the 42x42 mm PV cell which has an area of 1764 mm^2, power density is around 0.013μ W/mm^2 in 470 lux, and approximately 0.024μ W/mm^2 in 700 lux of illuminance. For the 45x45 mm PV cell which has an area of 2025 mm^2, power density is about 0.016μ W/mm^2 in 470 lux, and close to 0.031μ W/mm^2 in 700 lux of illuminance.

Considering an application where the PV cell will provide the power and also its voltage will be converted by an DC-DC converter, for example, some DC-DC converter input voltages can be estimated with this characterization. Considering, as example, a 42x42 mm PV cell minimum output power of 20μ W in 470 lux, the PV cell output voltage ranges from 0.35 to 0.63 V. In 700 lux, PV cell output voltage ranges from 0.47 to 0.65 V for a minimum output power of 40μ W. Taking into account a 45x45mm PV cell minimum output power of 30μ W in 470 lux, the PV cell output voltage ranges from 0.24 to 0.41 V. In 700lux, PV cell output voltage ranges from 0.34 to 0.47 V for a minimum output power of 60μ W.

If the mentioned application, for example, requires a DC-DC converter output

voltage from 0.4 to 0.5 V, some voltage conversion ratios were estimated as well, and Table 8 presents them.

Table 8 – Estimated voltage conversion ratios.

PV cell	DC-DC converter output voltage	Voltage conversion ratio
42x42mm	0.4V	0.64 to 1.14 @470 lux 0.61 to 0.85 @700 lux
	0.5V	0.8 to 1.42 @470 lux 0.77 to 1.06 @700 lux
45x45mm	0.4 V	0.97 to 1.66 @470 lux 0.85 to 1.17 @700 lux
	0.5V	1.22 to 2.08 @470 lux 1.06 to 1.47 @700 lux

Source: Author

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