Marcelo Pereira Magalhães

Design and Analysis of an Antenna Array System for Communication Using High-Altitude Platforms

Alegrete, RS

12.05.2017

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Master thesis presented to the Graduate Program in Electrical Engineering, major subject Energy Systems, of Universidade Federal do Pampa (UNIPAMPA, RS), as a partial requirement to obtain the degree of **Master in Electrical Engineering**.

Universidade Federal do Pampa – UNIPAMPA

Graduate Program in Electrical Engineering

Advisor: Prof. Dr. Marcos Vinício Thomas Heckler

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Sistema GURI (Gestão Unificada de Recursos Institucionais) .

M188d Magalhães, Marcelo Pereira
Design and Analysis of an Antenna Array System for Communication Using High-Altitude Platforms / Marcelo Pereira Magalhães.
105 p.

Dissertação(Mestrado)-- Universidade Federal do Pampa, MESTRADO EM ENGENHARIA ELÉTRICA, 2017.
"Orientação: Marcos Vinício Thomas Heckler".

1. Rede de antenas em microfita. 2. Serviços de comunicações móveis. 3. Dupla-banda e dupla-polarização. 4. Circuitos em alta frequência. 5. Simulações eletromagnéticas. I. Título.

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12.05.2017

I dedicate this work to my family, especially to my parents, Joel and Vânia Magalhães for all the support and affection in the difficult moments.

Acknowledgements

First of all, I thank Prof. Dr. Marcos Vinício Thomas Heckler, for the dedication in supervising, encouraging, understanding and teaching the technical concepts of the study area, which made possible the accomplishment of this work. I also would like to thank the granted opportunities as travel abroad bringing new knowledge and life experience, for advice and the confidence placed in me during all the work.

To my family, especially to my parents Joel and Vânia Magalhães, which are essential for my academic life. To my brothers Guilherme and Vinícius Magalhães, for support, affection, advice, encouragement and for always being willing to help me when necessary.

To the professors and friends of the Universidade Federal do Pampa, to all laboratory and research group (LEMA) colleagues in particular to Cleiton Lucatel and Diego Fumagalli which were essential in the experimental developments, as well as to the German Aerospace Center (DLR) colleagues in particular to Andreas Winterstein and Lukasz Greda, and all who contributed in some way, always being willing to assist when necessary, providing enriching tips that helped in the accomplishment of the work.

To all, thank you very much!

"Happiness is only real when shared "
(Christopher McCandless)

Abstract

This thesis presents the design and analysis of an antenna array system for mobile communication services in a scenario using high altitude platforms (HAPs). For this purpose, a dual-band and dual-polarized microstrip antenna array has been designed, whereby the array should receive the signal in one band and resend it in the other operating band. These requirements have been fulfilled by using a stacked arrangement, whereby each patch has been fed by independent feed lines. Circular polarization was obtained by the use of square patches with truncated corners. Optimizations were needed so as to compensate the effects of mutual coupling on the axial ratio level. To perform the radiation pattern synthesis for the transmission function, an algorithm to calculate the required excitation coefficients was employed to steer the main beam and to control the side lobe level.

Additionally to the array design, the development of the high-frequency (HF) circuitry for the retransmission is described. The design of the transmitter was done using off-the-shelf components, which have been tested individually prior to the final integration into the final layout. During the tests, the need of knowledge of the electromagnetic properties of the printed circuit layout and the active/passive components is crucial for a successful design. In order to accelerate the development of HF circuitry, a procedure to perform electromagnetic simulations of HF printed circuit boards is proposed. Experimental results demonstrated that this procedure yielded accurate engineering predictions.

Keywords: microstrip antenna array, mobile communication services, dual-band and dual-polarized antennas, high-frequency circuitry, electromagnetic simulations.

Resumo

Projeto e Análise de um Sistema de Rede de Antenas para Comunicação Utilizando Plataformas de Alta Altitude

Este trabalho apresenta o projeto e análise de um sistema de rede de antenas para serviços de comunicações móveis em um cenário empregando plataformas de alta altitude (HAPs). Para este fim, uma rede de antenas de microfita foi projetada para operar em dupla-banda e dupla-polarização, onde a rede deve receber o sinal em uma banda e reenviá-lo em outra. Esses requisitos foram cumpridos usando uma rede de antenas com múltiplas camadas, onde cada patch foi alimentado por linhas de alimentação independentes. A polarização circular foi obtida pelo uso de patches quadrados com os cantos truncados. Foram necessárias otimizações para compensar os efeitos de acoplamento mútuo no nível da razão axial. Para realizar o controle do diagrama de irradiação para o modo de transmissão, utilizou-se um algoritmo para calcular os pesos necessários para apontar o lóbulo principal e controlar o nível dos lóbulos laterais.

Adicionalmente ao projeto da rede, o desenvolvimento de um circuito em alta frequência (HF) para a retransmissão foi descrito. O projeto do circuito transmissor foi realizado empregando componentes comerciais, que foram testados individualmente antes da integração final. Durante os testes em bancada, ficou evidente a necessidade de predição do comportamento eletromagnético do layout da placa de circuito impresso e dos componentes ativos/passivos para obtenção de bons resultados. Com o intuito de acelerar o processo de desenvolvimento de circuitos em HF, um procedimento para a realização de simulações eletromagnéticas de placas de circuito impresso foi proposto. Os resultados experimentais demonstraram que este procedimento produziu bons resultados.

Palavras-chave: rede de antenas em microfita, serviços de comunicações móveis, antenas com dupla-banda e dupla-polarização, circuitos operando em alta frequência, simulações eletromagnéticas.

List of Figures

List of Tables

Content

1 Introduction

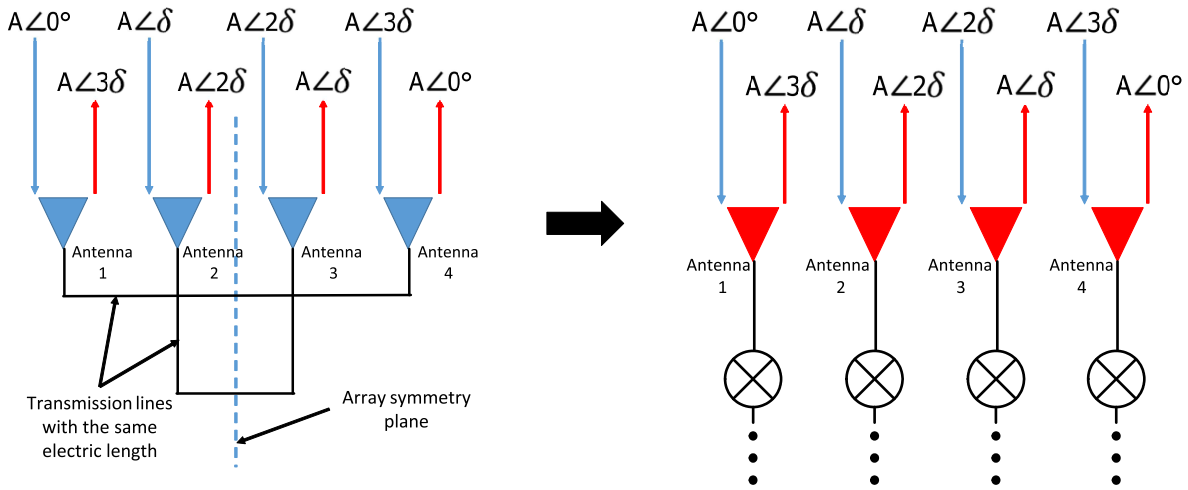
Adaptive antenna systems have been widely used in recent years and have become an alternative for applications that require efficiency and high quality of signal, such as in mobile communications systems and aerospace applications (CHANDRAN, 2004). This type of antenna has become attractive due to the possibility of performing the beamsteering of the main lobe in the desired direction and suppressing the side lobes simultaneously only by means of electronic control of the excitation of each antenna, thus avoiding the need to mechanically steer the antenna to point its main beam in the desired direction. This feature prompted a growing development of beamforming and beamshaping techniques, in order to allow the implementation of adaptive antennas (CHANDRAN, 2004).

Fully adaptive antennas demand the use of an algorithm to estimate the direction of arrival and another for shaping the radiation pattern. Pattern synthesis may be challenging especially for applications where the system must have a fast update rate. For the particular case of data relay systems, this problem can be overcome by the use of retrodirective arrays, which are a particular class of adaptive antennas that is able to retransmit the received signal without any signal processing to estimate the direction of arrival. This is achieved by means of phase conjugation of the signals received by the array elements (MAGALHÃES et al., 2015). The classical example of retrodirective antennas is the Van Atta configuration, which is a passive array where the phase conjugation is obtained simply by interconnecting the array elements directly through lines with the same electrical length (MIYAMOTO; ITOH, 2002). However, for long-distance communications where large free space losses are present, the use of active devices cannot be avoided. Moreover, the Van Atta array does not allow frequency translation, which may be required if the array is to be installed on a sattelite or on a high altitude platform (HAP), whereby uplink and downlink frequencies are normally different. Fig. 1 depicts the Van Atta and an active reflectarray topologies.

The synthesis of antennas and arrays based on optimization algorithms such as PSO has been reported in some recent studies. In (REN; CHANG, 2006), the design of a planar array of retrodirective antennas operating at 5.8 GHz for wireless application is presented, while (HOOD; TOPSAKAL, 2007) discusses the implementation of PSO in MATLAB to design a microstrip antenna operating with dual-band behaviour. Also, in (PAPADOPOULOS et al., 2006) and (ZUNIGA; ERDOGAN; ARSLAN, 2010), PSO has been used to synthesize radiation patterns. The development of some architectures of retrodirective antennas for different scenarios of communication is presented in (GOSHI; ITOH, 2008). An interesting approach is reported in (HSU et al., 2010) using adaptive antennas in order to synthesize the radiation pattern through PSO algorithm. In

Figure 1 – Typical retrodirective antenna configurations.

(a) Van Atta array. (b) Active array.



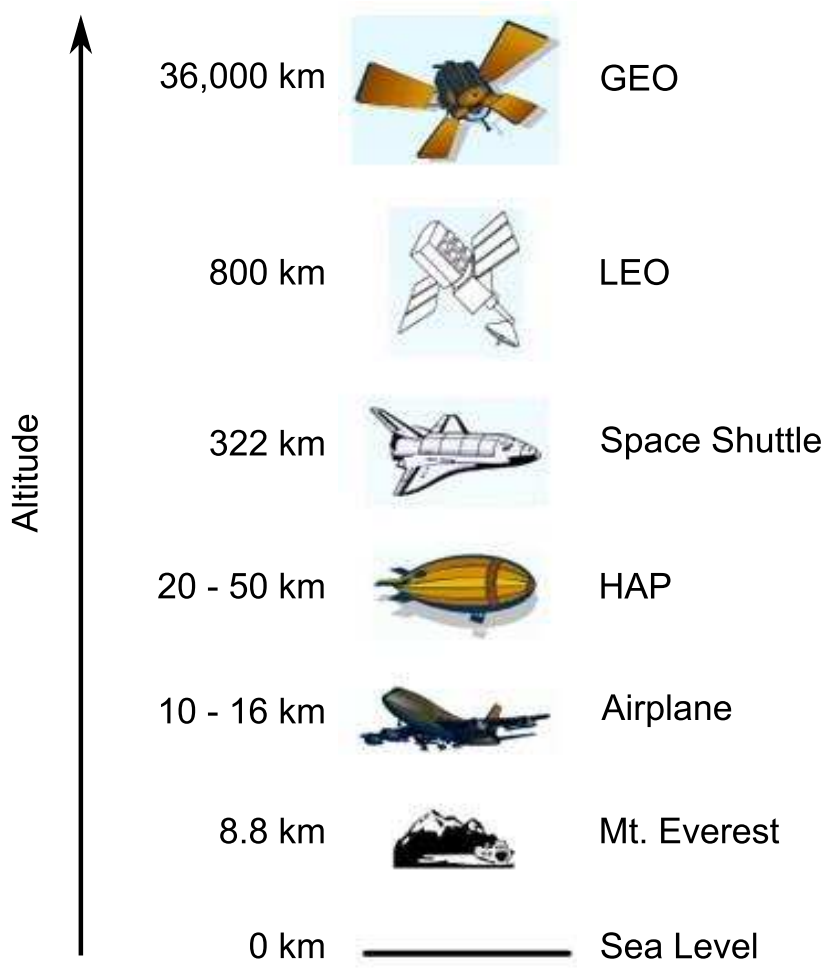
Source: The author.

(ANDRE; LEONARD, 1964), the study of an retrodirective system and RF circuit considering element failures are presented, while (MIYAMOTO et al., 2003) and (CHEN; YAN, 2009) present the design of a smart antenna/retrodirective array applied to wireless sensor systems. The approach of a 60 GHz retrodirective array system with an efficient power management of the LO for wireless multimedia sensor server applications is presented in (LIM; ITOH, 2008). In (KAWAZOE et al., 2005) and (OKAZAKI et al., 2007), the design of a reconfigurable RF circuit architecture for dynamic power reduction and future band-free mobile terminals are presented, respectively.

Retrodirective systems used on HAPs or sattelites can be employed in several applications, such as: replacing communication base stations when they are broken, transponders to relay a signal back to the interrogator, collision avoidance systems, disaster scenarios, and also in regional television systems (BISCHL, 2008). An alternative approach using retrodirective antennas on HAPs could replace most of the current available ground infrastructure (VHF/UHF repeaters) for broadcasting. As it can be observed in Fig. 2, high altitude plataforms work at altitudes between 20 km and 50 km from the Earth surface, while other systems work at higher altitudes such as geostacionary-earth orbit (GEO) and low-earth orbit (LEO) satellites (PARK, 2008). For this reason, HAPs tend to be more cost effective than satellite-based communications. Another advantage is the possibility to do maintenance periodically.

The particle swarm optimization (PSO) algorithm has been used to calculate the excitations of each antenna. The PSO was chosen due to the advantages compared to other techniques. In (SCHLOSSER; TOLFO; HECKLER, 2015), the PSO has been applied to radiation pattern synthesis with faster convergence in comparison to the genetic

Figure 2 – Different altitude levels for geographic and communication systems examples.



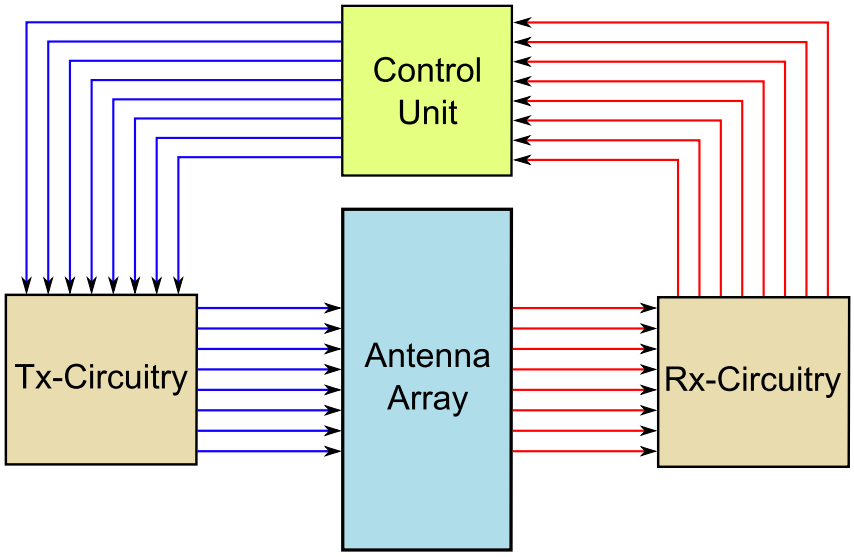
Source: Adapted from (PEREIRA, 2015).

algorithm (GA). PSO is an evolutionary technique inspired in the social behaviour of birds (KENNEDY; EBERHART, 1995). The name ”swarm”comes from the irregular movement of the particles in the computational domain (CARTWRIGHT, 2002). The PSO is based on studies in artificial life and social psychology, as well as in engineering and computer science. It utilizes a population of individuals, referred to as particles, that fly in a hyperspace with variable speed. In each iteration, the speed and position of each particle are adjusted by taking into account the best overall historical position and their relative distance to the particle that is assumed to be closest to the optimum solution (best place). By doing so, each particle evolves naturally to the optimum or to a near-optimum solution (CARTWRIGHT, 2002).

The defined antenna array for the present study is composed of circularly polarized microstrip antennas, designed to operate in dual-band and with dual-polarization. These features are suitable for installation on HAPs, which is one the main goals of the proposed design. The retrodirective system works basically with the antenna array receiving the

signal at 5.8 GHz and transmitting at 7.0 GHz. The received signal should be processed by a control unit. Algorithms such as PSO or Taguchi (WENG; YANG; ELSHERBENI, 2007) can be used in order to perform the beamforming of the radiation pattern for the retransmission. Thus, with the calculated excitations, the signal is processed using a Tx-circuit that provides each array element with the required magnitude and phase. Fig. 3 presents a flow chart showing the steps described previously. The main focus of this work are the investigation of the antenna array properties and of the needed Tx-circuitry. The optimization with PSO is carried out with the active patterns of the array elements, which have been computed using the electromagnetic simulator Ansys HFSS (ANSYS Corp., 2013). The Tx-circuitry is composed of 8 channels that perform the frequency translation from the control unit outputs (31 MHz) to the antenna array (7.0 GHz). This work was developed at UNIPAMPA and partially at the German Aerospace Center (DLR), in Germany. The scientific contributions of this work are the design of an antenna array that operates with dual-band and dual-polarization, and the procedure to accelerate the design of printed circuit boards operating at microwave frequencies.

Figure 3 – Flow chart of a retrodirective system.



Source: The author.

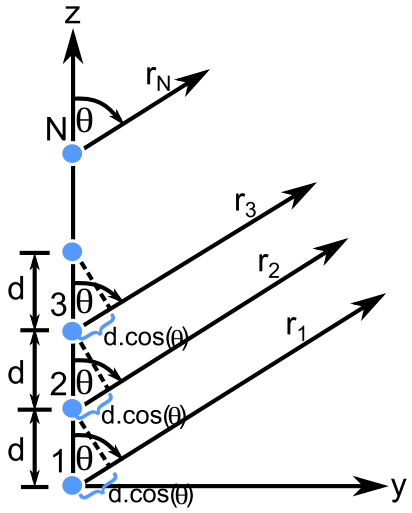
The work is divided into the following chapters: Chapter 2 presents the design of a dual-band and dual-polarized antenna array suitable for retrodirective systems. Chapter 3 discusses the development and measurements of the designed RF circuitry for the retransmitting function. Chapter 4 presents a procedure explaining how to simulate high frequency (HF) printed circuit boards using ANSYS Designer and ANSYS HFSS software. Finally, in Chapter 5 the concluding remarks are described.

2 Dual-Band and Dual-Polarized Antenna

2.1 Design Specifications

Antenna arrays are widely used due to advantages such as the possibility to shape the radiation pattern, increasing the directivity and higher flexibility in the design, which are characteristics that are not possible by using standalone antennas. The special class of retrodirective microstrip arrays exhibit the feature to retransmit a signal back to the direction of arrival. Among several other applications, the target investigated in this work is a retrodirective array for high altitude platforms, which are allowed to operate at 5.8 GHz for the uplink (receiving mode) and at 7.0 GHz for the downlink (transmitting mode). In order to increase isolation between the uplink and downlink channels, the array shall operate with right-hand circular polarization (RHCP) in the receiving mode and with left-hand circular polarization (LHCP) to transmit the signal back. The bandwidth has been specified to be 100 MHz for the antenna array and 50 MHz for the RF circuits.

Figure 4 – Linear array with approximation valid for the far-field region.



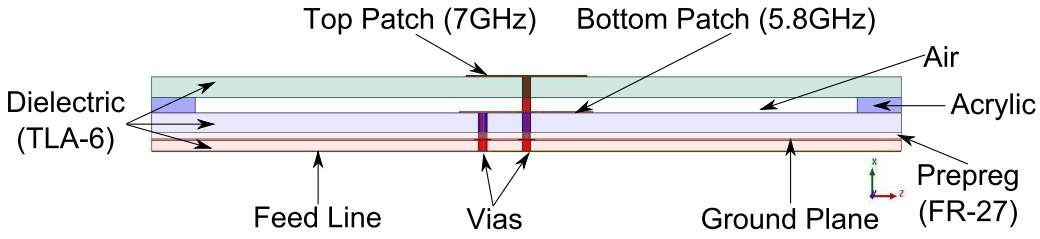
Source: The author.

Considering the radiation pattern of only one element, it is not possible to perform the beamforming or beamsteering. For long distance communications the required gain must be high, and an antena array structure is necessary. Antenna arrays can be composed of linear or planar structures. A linear arrangement is shown in Fig. 4 for the case of N antennas. The total electric field is calculated by the vector sum of the electric fields radiated by each element. Therefore, it is necessary that the fields interfere constructively in the desired direction θ_p. The parameters to realize the radiation pattern control are: number of elements, antenna array geometric distribution, magnitude and phase of each

element excitation, distance between the elements and the electric field that is particular for each single element (BALANIS, 2012).

In order to fulfill the specifications above, the array element has been designed with two stacked corners-truncated patches (POZAR, 1992; PEREIRA; HECKLER, 2015). In order to improve isolation between the receiving (Rx) and transmitting (Tx) channels, each patch has been fed by independent microstrip lines, which are connected to the respective patch by means of conducting vias. Fig. 5 presents the antenna geometry, where the dielectric layers are composed of two layers of the laminate Taconic TLA-6 (Taconic Corp., 2008) with thicknesses of 1.96 mm (top and middle layers) and 1.02 mm (bottom layer). This material was chosen due to its low losses, low and stable dielectric constant $\varepsilon_r = 2.62$, and good mechanical and thermal properties, which are interesting features for the antennas to be installed on HAPs. The bottom and the middle layers were glued using FastRise-FR27 (Taconic, 2013), which is a prepreg with thickness of 0.107 mm and dielectric constant of $\varepsilon_r = 2.75$. Two of FR27 layers have been used in this implementation. In order to achieve the desired bandwidth, an 1.4 mm thick air layer has been inserted between the stacked patches. The thicknesses of all layers are summarized in Table 1.

Figure 5 – Structure of an retrodirective antenna, cross-section view.



Source: The author.

Table 1 – Thicknesses of the antenna layers.

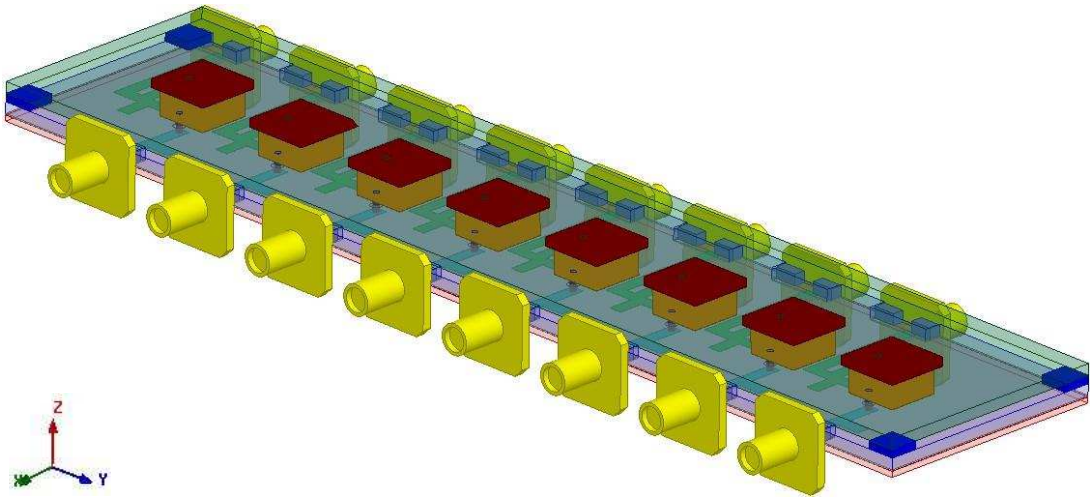
Layer	Thickness (mm)
Top Patch	0.035
Top TLA-6 Layer	1.960
Air	1.400
Bottom Patch	0.035
Middle TLA-6 Layer	1.960
Glue (Prepreg) 2	0.107
Glue (Prepreg) 1	0.107
Ground Plane	0.035
Bottom TLA-6 Layer	1.020
Feed Line	0.035

Source: The author.

2.2 Simulation Results

An adaptive antenna array system basically works by controlling the amplitude and phase of each antenna. The first step of optimization consists in simulating the antenna array considering uniform distribution of power for each antenna, by setting the same amplitude and phase at the inputs of each element. In order to compute the embedded patterns of each radiator, the 1x8 antenna array structure shown in Fig. 6 has been simulated in Ansys HFSS. The 8 elements were defined due to the compromise between the array dimensions and the possibility to perform the radiation pattern beamsteering up to 45 ° from the boresight direction. The use of few elements allows only the steering in a small angular range, whilst more elements would require a lot of Tx-channels, increasing the project complexity and costs.

Figure 6 – Retrodirective antenna array structure, isometric view.



Source: The author.

Table 2 – Initial dimensions for the antenna array simulation.

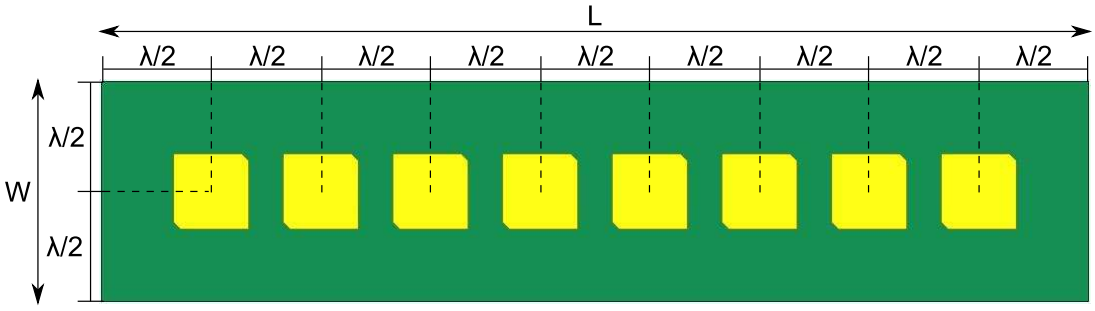
Parameter	Initial Dimension (mm)
L Bottom Patch	15.115
A Bottom Patch	5.634
L Top Patch	13.744
A Top Patch	1.453
W Feed Line	2.350

Source: The author.

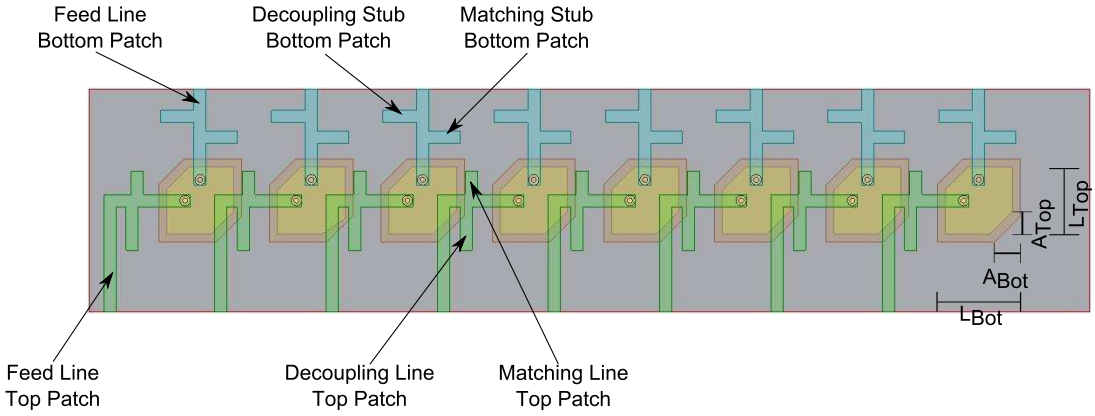
As it can be observed in Fig. 7, a spacing between the center of each element and the edges of $d = \lambda/2$ was used, where λ is the wavelength in free space at 7.0 GHz. This results in $d = 2.143$ cm. The array exhibits total length of $L = 19.286$ cm and total width of $W = 4.286$ cm. To perform the antenna excitation, vias with radius of $r = 0.5$ mm were used. To decrease the losses due to coupling between the Rx and the Tx channels, two kinds of stubs were used. Finally, to obtain the circular polarization, it is necessary to use the technique of corners-truncated patches, where the axial ratio can be controlled by the parameters (cuts) A_{Bot} and A_{Top}. The initial parameters for this design were defined from the optimized single antenna in (PEREIRA, 2015) with the dimensions listed in Table 2.

Figure 7 – Designed retrodirective antenna array, in different views.

(a) Spacing between elements and edges, top view.



(b) Feed lines schematic, bottom view.



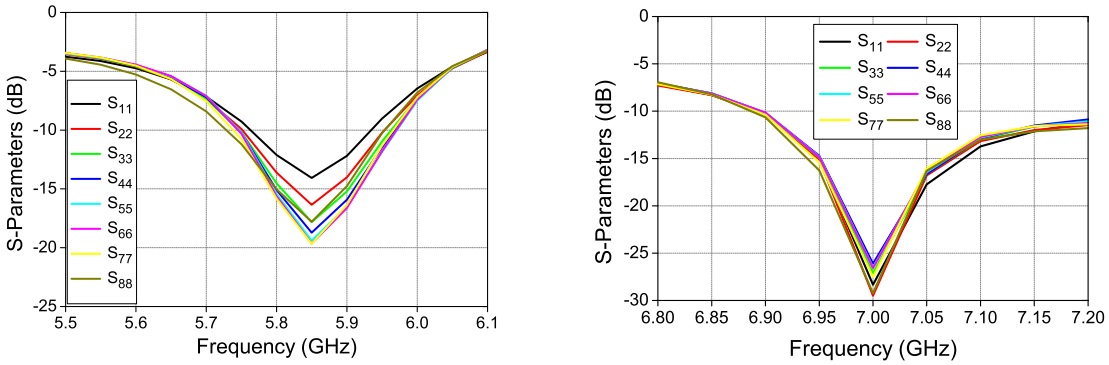
Source: The author.

Due to the large simulation time, the analysis for each frequency range was made separately. Firstly, the optimization for the lower band at 5.8 GHz (receiving mode) was performed. Since the radiated fields can affect the receiving channels, all the ports were excited with magnitude $A = 1$ and phase $\theta = 0\,^{\circ}$. After some optimizations, results in terms of S-parameters, axial ratio and radiation pattern are shown in Figs. 8 - 10. One can observe that good results were obtained in terms of impedance matching and axial ratio in the required specifications. The radiation pattern at 5.8 GHz presents gain of 13.0 dBi and large cross-polarization decoupling has been achieved.

Figure 8 – Reflection coefficient as a function of the frequency for the dual-band antenna array.

(a) Results at lower band - 5.8 GHz.

(b) Results at upper band - 7.0 GHz.

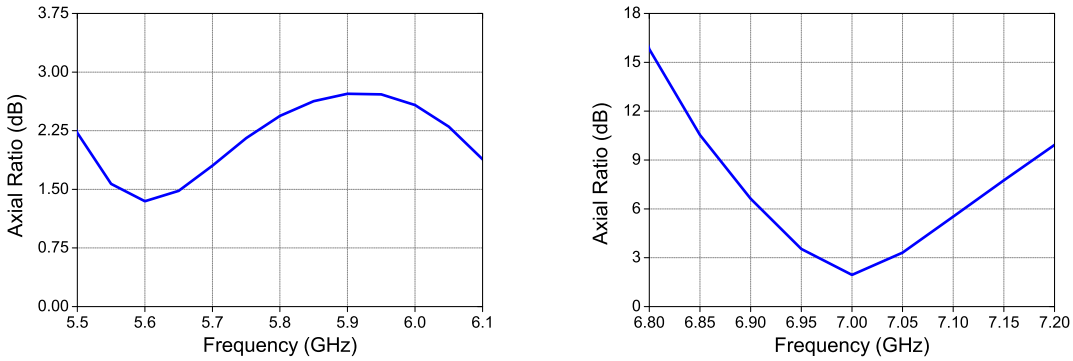


Source: The author.

Figure 9 – Axial ratio as a function of the frequency for the dual-band antenna array.

(a) Results at lower band - 5.8 GHz.

(b) Results at upper band - 7.0 GHz.

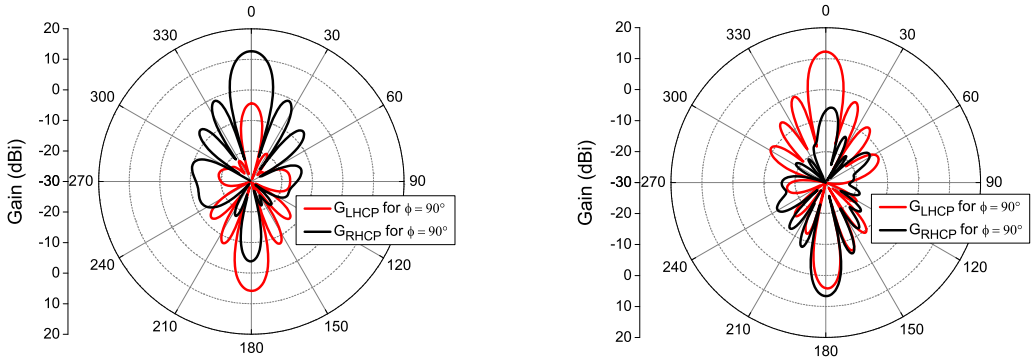


Source: The author.

Figure 10 – Radiation pattern for the dual-band antenna array.

(a) Results at lower band - 5.8 GHz.

(b) Results at upper band - 7.0 GHz.



Source: The author.

The second step consisted in an analysis at the upper frequency range at 7.0 GHz (transmitting mode). Differently than for the previous step, the receiving antennas do not affect the radiation pattern at the transmission mode. Therefore, the ports for the Rx channels were disabled (magnitude $A = 0$ and phase $\theta = 0\,^{\circ}$). At the transmission ports, $A = 1$ and $\theta = 0\,^{\circ}$ was set. Good results based on the specifications were obtained in terms of impedance matching and axial ratio in the required bandwidth. The radiation pattern at 7.0 GHz presents maximum gain of 13.0 dBi. By optimizing the array at 7.0 GHz, the antenna became slightly detuned at 5.8 GHz, due to the mutual coupling between antennas and axial ratio deterioration. For this reason, the procedure described above had to be carried out repeatedly until acceptable performance has been obtained. The optimized dimensions are listed in Table 3.

Table 3 – Final dimensions for the antenna array simulation.

Parameter	Final Dimension
L Bottom Patch	15.270
A Bottom Patch	5.689
L Top Patch	13.771
A Top Patch	0.938
W Feed Line	2.350

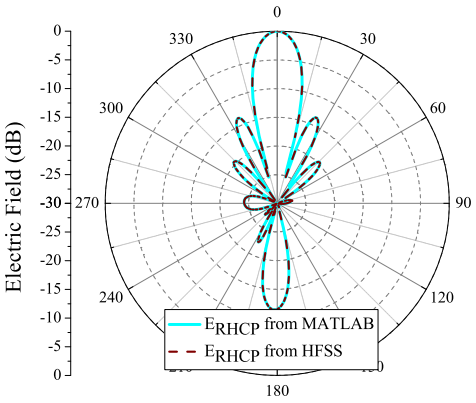
Source: The author.

2.3 Parametric Study of the Antenna Array

2.3.1 Impact of the RF components resolution

In any practical communication system, active components are needed in the front-end chain in order to allow the signal to be received or transmitted and then demodulated. In adaptive antennas, beamforming may be obtained in the digital or in the analog domain (MAGALHÃES et al., 2015). In the second case, the magnitudes of the signals received by each antenna may be controlled by introducing a variable gain amplifier (VGA) in the Rx chain of each array element. In the present study, simulations were carried out to assess the performance of the array in receiving mode. The radiation pattern of the array at 5.8 GHz with uniform current distribution and steering to the boresight is shown in Fig. 11, where the calculated radiation pattern and coded in MATLAB fits the results obtained directly with HFSS. This pattern is not optimized and, therefore, the level of the first side lobe is around 13 dB below the main beam.

Figure 11 – Normalized radiation pattern of the retrodirective antenna array at 5.8 GHz without optimization, in dB.



Source: The author.

By using PSO, the pattern can be optimized by reducing the side lobe level. To demonstrate the technique, radiation patterns were synthesized for the cases of steering the main beam to 0 °, 15 ° and 30 ° from the array boresight ($\theta = 0\,^\circ$) and by setting $SLL = -20$ dB. The patterns generated after the optimization of the currents and calculated by the developed tool in MATLAB are shown in Fig. 12, where one can see that the levels of the side lobes satisfied the requirements (MAGALHÃES et al., 2015). The currents calculated by PSO for these three cases are presented in Table 4. It should be pointed out that the angular range considered for the optimization is lonely the upper hemisphere. The lobe in the lower part of the pattern ($90\,^\circ \leq \theta \leq 180\,^\circ$) is a result of back radiation that cannot be suppressed by array synthesis techniques, since it is an intrinsic property of the designed array elements. For validation purposes, the calculated currents have been introduced in the HFSS model, with the resulting pattern shown in dotted lines in Fig. 12. Excellent agreement between the results provided with the MATLAB code and those from HFSS can be verified.

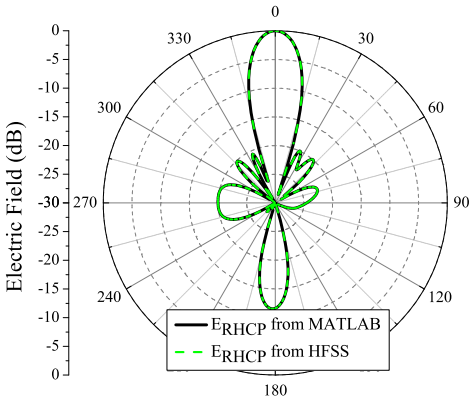
Table 4 – Magnitude and phase of the calculated currents using the PSO algorithm for different cases of beamsteering.

Element	**Steering of** 0 °		**Steering of** 15 °		**Steering of** 30 °	
	Mag.	**Phase**	**Mag.**	**Phase**	**Mag.**	**Phase**
1	0.793	0 °	0.462	0 °	0.177	0 °
2	0.507	0 °	0.363	−38.60 °	0.211	−76.82 °
3	0.862	0 °	0.842	−77.20 °	0.773	−153.6 °
4	1.000	0 °	1.000	−115.8 °	1.000	−230.4 °
5	0.966	0 °	0.936	−154.4 °	0.771	−307.3 °
6	0.909	0 °	0.806	−193.0 °	0.826	−24.08 °
7	0.212	0 °	0.381	−231.6 °	0.519	−100.9 °
8	0.419	0 °	0.343	−270.2 °	0.285	−177.7 °

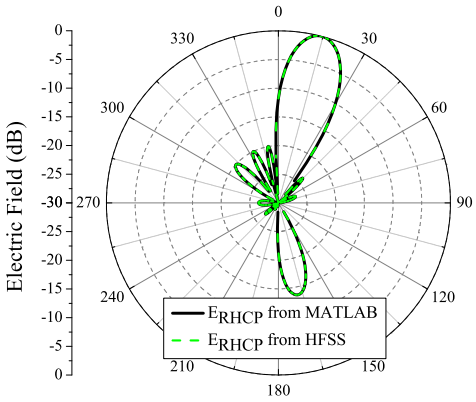
Source: The author.

Figure 12 – Normalized electric field for the code implemented in MATLAB and HFSS solution for $\phi = 90\,^{\circ}$, in dB.

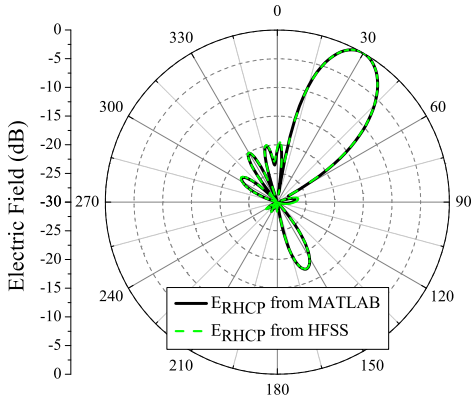
(a) Beamsteering of $0\,^{\circ}$.



(b) Beamsteering of $15\,^{\circ}$.



(c) Beamsteering of $30\,^{\circ}$.

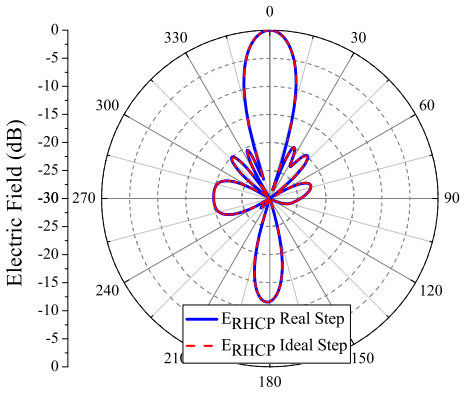


Source: The author.

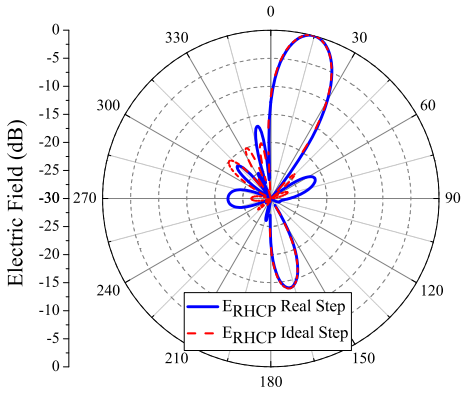
For practical implementation, an analysis including the effects of discretizing the magnitudes of the receiving signals has been performed. The analysis assumes the use of VGAs of the type DVGA1-24PP+. By considering that this device allows 64 levels of discretization and that the maximum gain is 31.5 dB, the gain step is $\frac{31.5}{64} = 0.5$ dB (the minimum gain is 0.5 dB). The same three cases have been considered for optimization with PSO. However, for this analysis, PSO has been set up to consider only the 64 discretized magnitude levels allowed by the 6-bit digitally controlled VGA. The ideal and discrete magnitudes of the currents for the three synthesized radiation patterns are presented in Table 5. Fig. 13 shows the normalized electric fields obtained for the $\phi = 90\,^{\circ}$ plane, where the continuous lines stand for PSO without considering discretization of the currents and the dotted lines represent the patterns obtained considering the performance of the VGA (MAGALHÃES et al., 2015). It can be observed that there was good suppression of the side lobes, but the SLL requirement could not be completely fulfilled in all the three analyzed cases.

Figure 13 – Normalized electric field for discrete and ideal control of the current magnitudes for $\phi = 90\,°$, in dB.

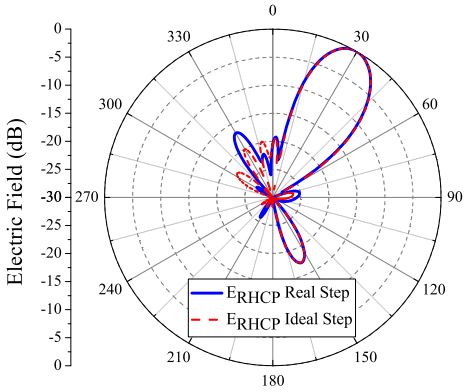
(a) Beamsteering of $0\,°$.



(b) Beamsteering of $15\,°$.



(c) Beamsteering of $30\,°$.



Source: The author.

Table 5 – Ideal and discrete current magnitudes for the cases of steering.

Element	**Steering of** $0\,°$		**Steering of** $15\,°$		**Steering of** $30\,°$	
	Ideal	**Discrete**	**Ideal**	**Discrete**	**Ideal**	**Discrete**
1	0.7935	0.7943	0.4620	0.4732	0.1776	0.1778
2	0.5067	0.5012	0.3635	0.3548	0.2113	0.2113
3	0.8620	0.8414	0.8424	0.8414	0.7733	0.7499
4	1.0000	1.0000	1.0000	1.0000	1.0000	1.0000
5	0.9656	0.9441	0.9360	0.9441	0.7712	0.7499
6	0.9086	0.8913	0.8058	0.7943	0.8264	0.8414
7	0.2122	0.2113	0.3809	0.3758	0.5190	0.5309
8	0.4198	0.4217	0.3425	0.3350	0.2852	0.2818

Source: The author.

Due to the need of precision at the main lobe steering, it is interesting to perform an analysis about the impact of the phase shifter resolution at the final radiation pattern of the antenna array. Since the chosen phase shifter has 4-bit of control, there are $2^4 = 16$ possible phase-shift values, in steps of $\frac{360}{16} = 22.5\,°$. In order to analyze the best and worst

cases, some tests were carried out. The best cases are achieved when the phase shift β is multiple of 22.5°, or $\beta = n * 22.5\,^\circ$ for $n = 0, 1, 2, 3, ...$ Considering an antenna array with 8 isotropic elements, distance $d = 0.5\lambda$ between the antennas and phase shift of $\beta = 22.5\,^\circ$, it is known that the main beam will be pointed to

$$\beta = -2\pi d cos\theta \longrightarrow \theta = cos^{-1}(-\frac{\beta}{2\pi d}) = 97.18\,^\circ \tag{2.1}$$

Therefore, the diference between the ideal and the discretized cases for the best case is

$$\Delta\theta = \theta_{ideal} - \theta_{step} = 97.18\,^\circ - 97.18\,^\circ = 0\,^\circ \tag{2.2}$$

The worst cases occur when the phase shift β is an odd multiple of $\frac{22.5\,^\circ}{2}$, or $\beta = n * 11.25\,^\circ$ for $n = 1, 3, 5, ...$ In this case, by assuming $\beta = 11.25\,^\circ$, it comes out that

$$\beta = -2\pi d cos\theta \longrightarrow \theta = cos^{-1}(-\frac{\beta}{2\pi d}) = 93.58\,^\circ \tag{2.3}$$

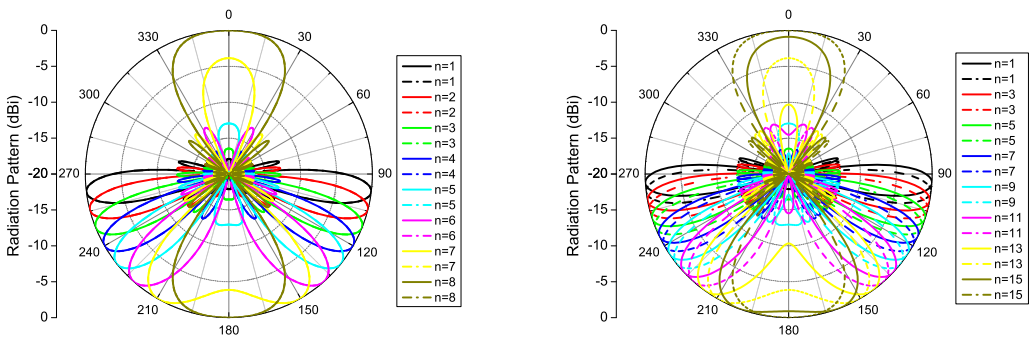
The diference between the ideal and the discretized cases is

$$\Delta\theta = \theta_{ideal} - \theta_{step} = 93.58\,^\circ - 90\,^\circ = 3.58\,^\circ \tag{2.4}$$

As it can be observed at the worst case, the desired steering diference for the supplied step of the phase shifter is of 3.58° error in pointing the main beam close to the boresight ($\theta = 90\,^\circ$), where the beam presents minimum beamwidth. Fig. 14 shows the normalized radiation pattern in dBi for the ideal and discretized cases for different steering directions, where the straight lines are pattern with the ideal values and the dotted lines are the ones for discretized phases.

Figure 14 – Normalized radiation pattern for ideal and discrete control, in dBi.

(a) Best cases. (b) Worst cases.

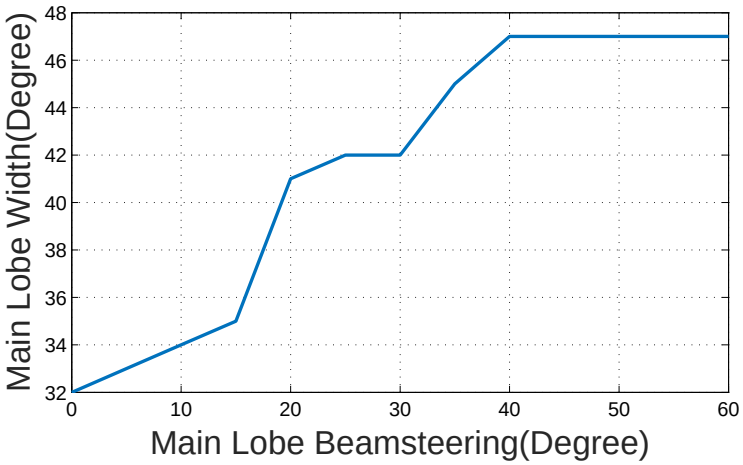


Source: The author.

2.3.2 Failure of one or more elements

This parametric study was based on the antenna array behaviour using MATLAB software. The phase behaviour of the Rx-circuitry, the truncation phase and power amplitude of the Tx-circuit were included in the analysis performed by the heuristic PSO. The analysis is divided in two parts: the first presents results for a fully functional array, where all the elements are working properly and the second one was performed to consider the case where one element is off, so that the optimization methods try to adjust the amplitude of the excitation coefficients so as to compensate element failure. For comparison, the array patterns using amplitude tapering with the standard Dolph-Chebyshev weights were included (ENGROFF et al., 2016). The main lobe width is a function of the beamsteering as can be seen in Fig. 15. This relation is obtained from the average width of the main lobe through the supplied currents defined from Dolph-Chebyshev. A low penalty region of 1° was defined farther the limit set for the main lobe in the mask, which is necessary to model the main lobe shape in this region (ENGROFF et al., 2016).

Figure 15 – Width of the main lobe as a function of the beamsteering.



Source: The author.

The optimization algorithm goal is to maximize the directivity for the main lobe steering angle. The maximum directivity used as a reference was 13 dBi. Thus, the cost function meets the following equation

$$F_{cost} = DD \cdot P_1 + LPA \cdot P_2 + HPA \cdot P_3 \tag{2.5}$$

Where DD is the difference between the obtained and desired directivity, LPA is the area above the mask in the low penalty region, HPA is the area above the mask in the high penalty region, P_1, P_2 and P_3 are the weights for each parameter. The weights $P_1 = 0.2$, $P_2 = 0.5$ and $P_3 = 1$ were obtained empirically by seeking the best cost results.

2.3.2.1 Fully functional array

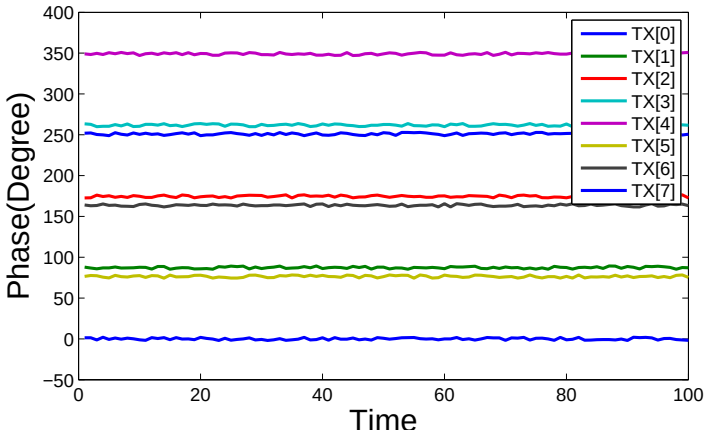
To simulate a fully functional array, a phase noise of ±4° was introduced with random variation for the case of steering the main beam to −30°. Fig. 16a shows the simulated phases for each element of the Rx-circuit. The calculation of the mean difference of the phases (β) for the Tx-circuit is shown in Fig. 16b, with the reference value indicating the actual β, that is calculated by the following equations

$$\beta = \frac{\sum_{i=1}^{8} \beta_i}{8} \tag{2.6}$$

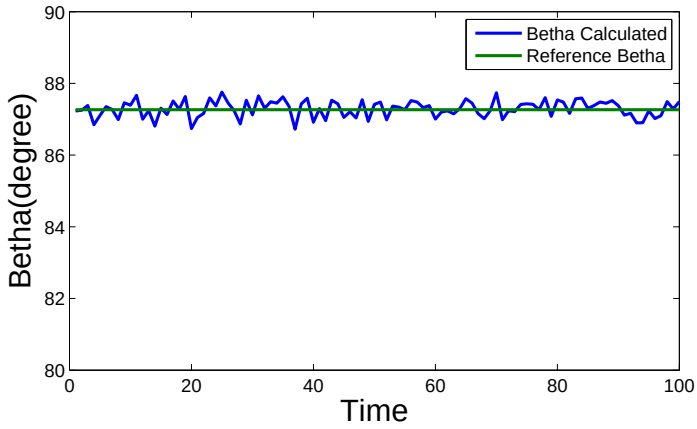
$$\beta_i = Phase_i - Phase_{i+1} \tag{2.7}$$

Figure 16 – Analysis for beamsteering to −30° for a fully functional array.

(a) Phases along of time of each antenna.



(b) Calculation of β along of time.

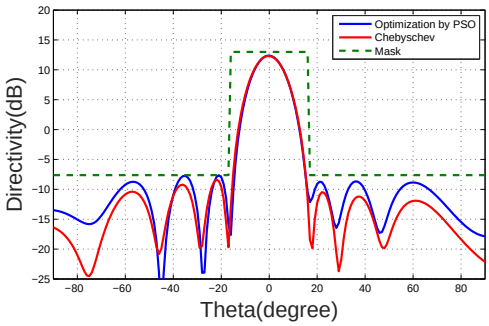


Source: The author.

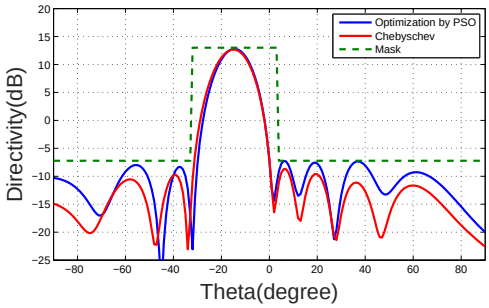
The optimized patterns are shown in Fig. 17 for different beamsteering direction and $SLL = -20$ dB. For the first two cases, the algorithm could optimize the pattern and fulfill the specifications. By steering the main beam to $-45°$ and $-60°$, one can see that the constraints regarding the side lobe levels could not be fully fulfilled.

Figure 17 – Optimized patterns for different beamsteering angles considering $SLL = -20$ dB.

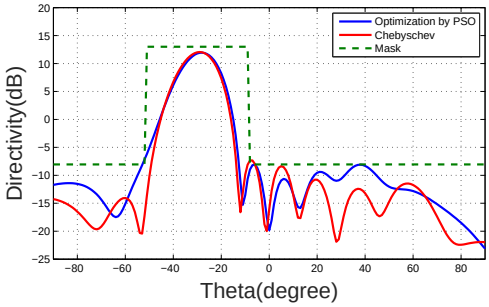
(a) Beamsteering of 0 °.



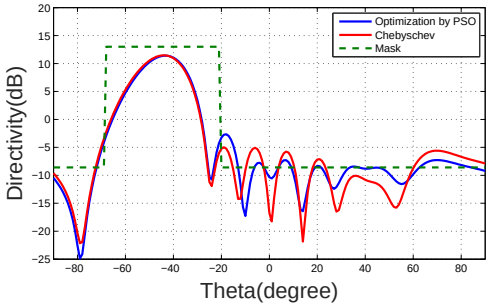
(b) Beamsteering of 15 °.



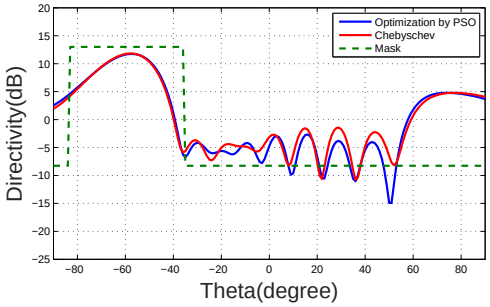
(c) Beamsteering of 30 °.



(d) Beamsteering of 45 °.



(e) Beamsteering of 60 °.



Source: The author.

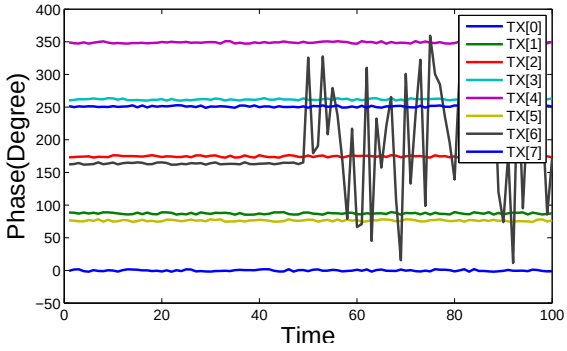
2.3.2.2 Array with faulty element in the receiver

In order to test the ability of determining the β values with tolerance to failure in the Tx-circuit, tests with loss of one and two elements in the Rx-circuit were performed. The main lobe is steered to $-30°$. The obtained results for the phases of each element of the Rx-circuit are shown in Fig. 18a. The value of the calculated β for the Rx-circuit is

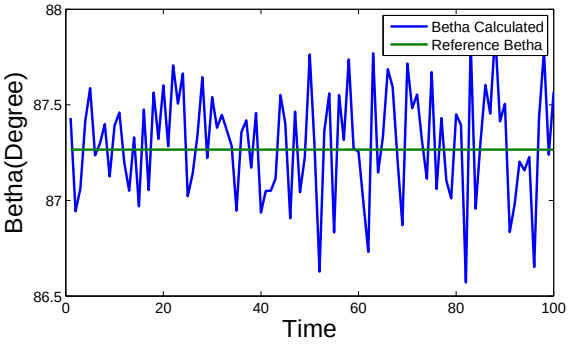
shown in Fig. 18b. As it can be seen, the variation of β is estimated between $\pm 4°$. For the failure of two elements, the phases of the elements are shown in Fig. 19a. The calculated β for the Rx-circuit is shown in Fig. 19b. The variation of β is in the range of $\pm 4°$. This demonstrates that the average calculation for determining the β is robust to loss of up to two elements.

Figure 18 – Analysis for beamsteering to $-30°$ with loss of one element of Rx-circuit.

(a) Phases along of time of each antenna.



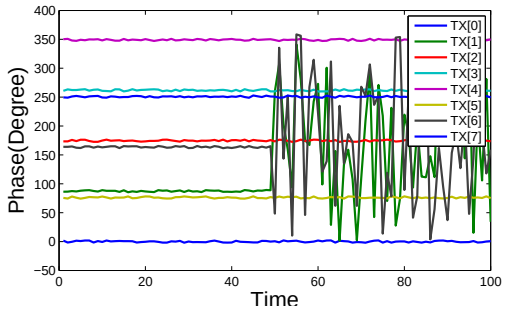
(b) Calculation of β in time.



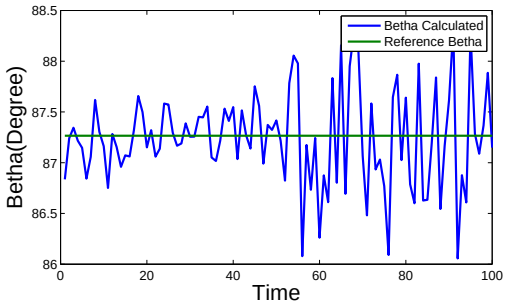
Source: The author.

Figure 19 – Analysis for beamsteering to $-30°$ with loss of two elements of Rx-circuit.

(a) Phases along of time of each antenna.



(b) Calculation of β in time.



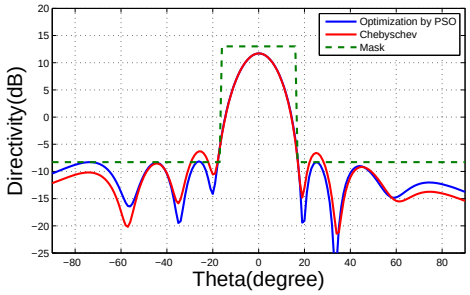
Source: The author.

2.3.2.3 Array with faulty element in the transmitter

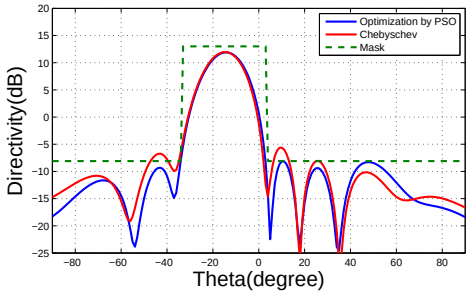
In order to test the beamforming capabilities under the case of one faulty element in the array, two situations were considered: failure of element 1 and element 4. In the same steering cases considered in the previous analysis, the optimized patterns are shown in Figs. 20 and 21. To visualize the impact of element failure, the pattern obtained with Dolph-Chebyshev distribution is plotted as a reference (ENGROFF et al., 2016). The graphics show that the loss of element 1 is not as critical as it is for the case of losing element 4, since better results are obtained for the first case in comparison to the latter. This can be expected, since failure of element 1 results in a still uniform linear array with reduced size. Finally, for beam steering to $-45°$, $-60°$ and failure of element 4, the PSO fails to achieve the desired specifications.

Figure 20 – Optimized patterns for different beamsteering angles considering $SLL = -20$ dB, and failure of element 1.

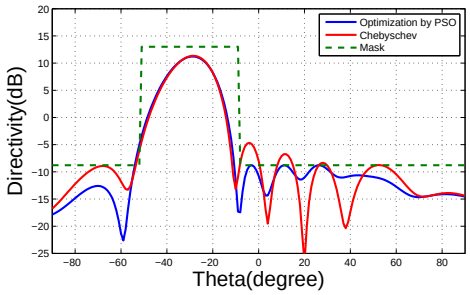
(a) Beamsteering of 0 °.



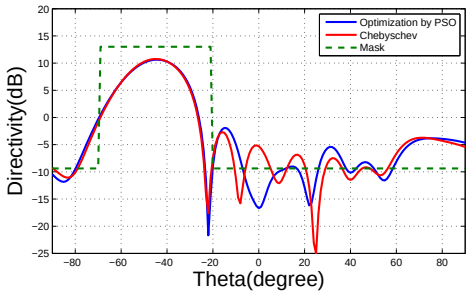
(b) Beamsteering of −15 °.



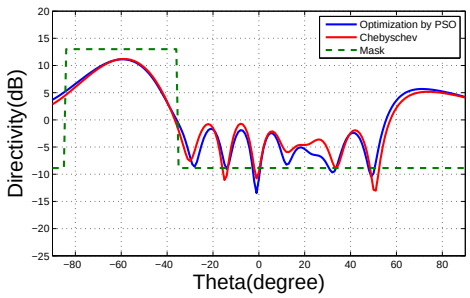
(c) Beamsteering of −30 °.



(d) Beamsteering of −45 °.



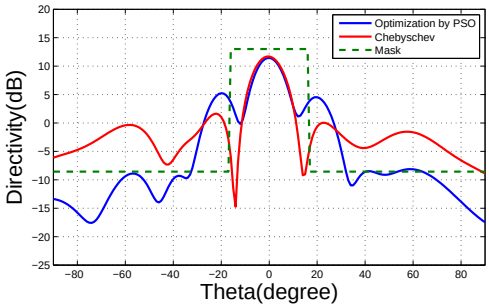
(e) Beamsteering of −60 °.



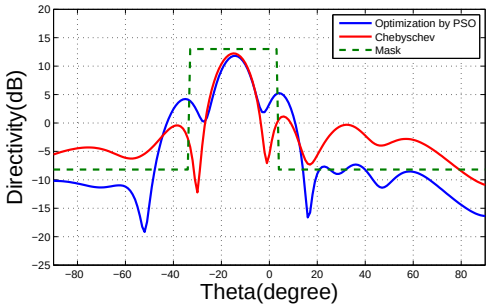
Source: The author.

Figure 21 – Optimized patterns for different beamsteering angles considering $SLL = -20$ dB, and failure of element 4.

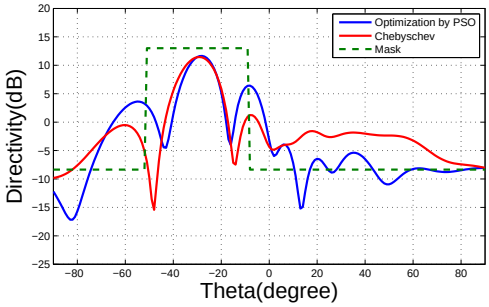
(a) Beamsteering of $-0\,°$.



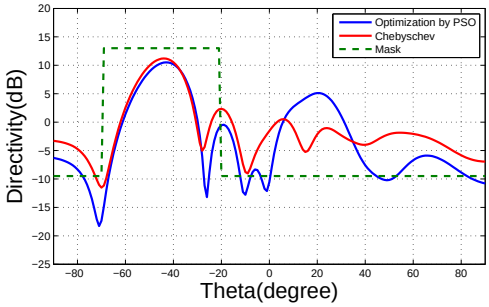
(b) Beamsteering of $-15\,°$.



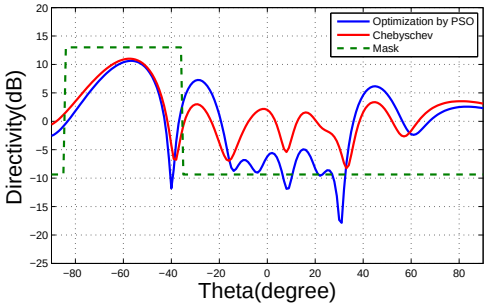
(c) Beamsteering of $-30\,°$.



(d) Beamsteering of $-45\,°$.



(e) Beamsteering of $-60\,°$.

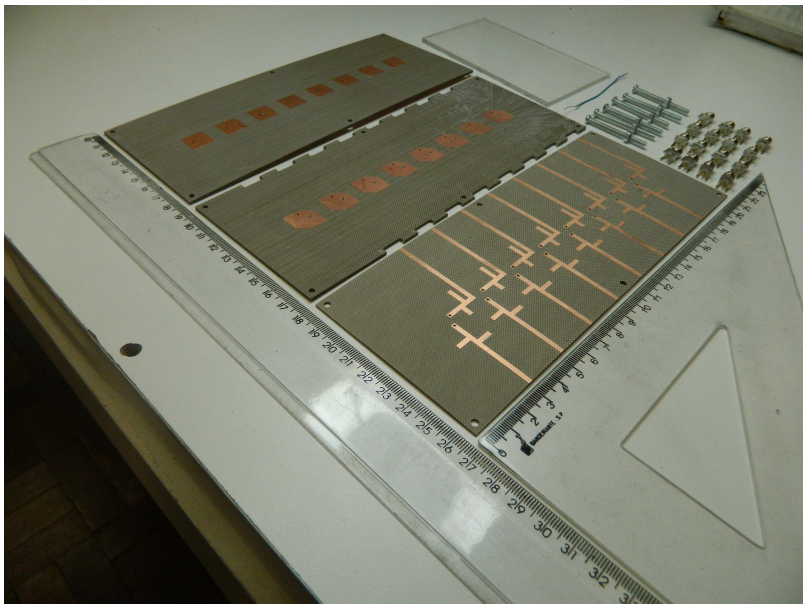


Source: The author.

2.4 Antenna Array Prototype and Measured Results

Based on the antenna array design specifications stated previously, the simulated topology was prototyped. All the specifications were followed in order to obtain the best agreement between simulation and measurement as possible. As well known, antennas operating at high frequencies are not easily prototyped, because of the high sensitivity to fabrication tolerances. The first step consisted on prototyping the three layers of patches and transmission lines as shown in Fig. 22.

Figure 22 – Prototyped antenna array layers.



Source: The author.

After that, the transmission line layer (bottom layer) was glued to the bottom patches that operate at 5.8 GHz (medium layer) with the prepreg (FR27). For good alignment between layers, four screws were used at the corners during the gluing process. The two layers were placed in the oven at conditions of pressure and temperature recommended by the glue manufacturer, as it can be seen in Fig. 23. The next step consisted on soldering the SMA connectors and the vias between the transmission lines to the patches working at 5.8 GHz, as shown in Fig. 24.

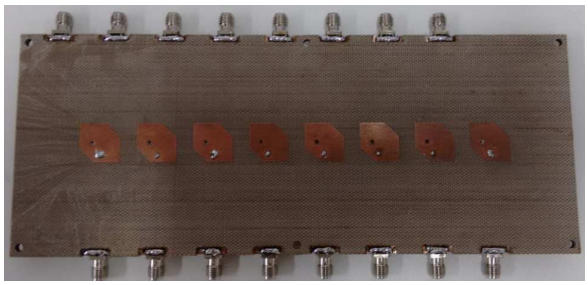
Figure 23 – Prototype prior to and after glueing.

(a) Oven view. (b) Top view.

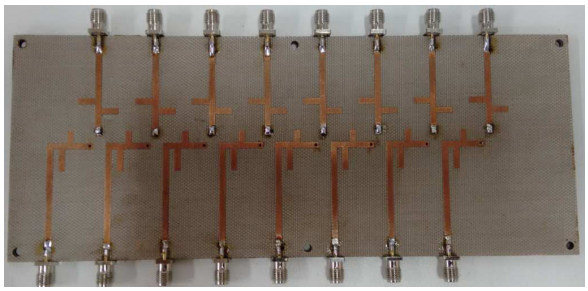
Source: The author.

Figure 24 – Soldered vias for lower frequency patches.

(a) Top view.



(b) Bottom view.

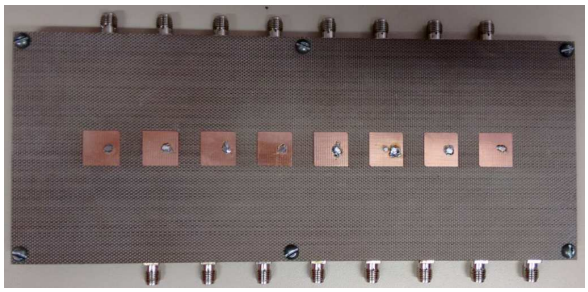


Source: The author.

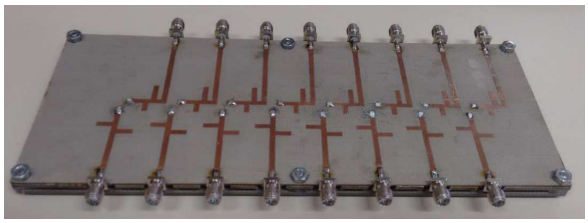
Finally, the top layer was attached to the two glued layers. An important issue is to keep the air gap exactly the same as for the simulated structure. In this case, acrylic blocks were used during the soldering process. The vias were soldered first, since they also help to keep the correct air gap. The final prototype structure is shown in Fig. 25.

Figure 25 – Prototyped final structure for the retrodirective antenna array.

(a) Top view.



(b) Bottom view.

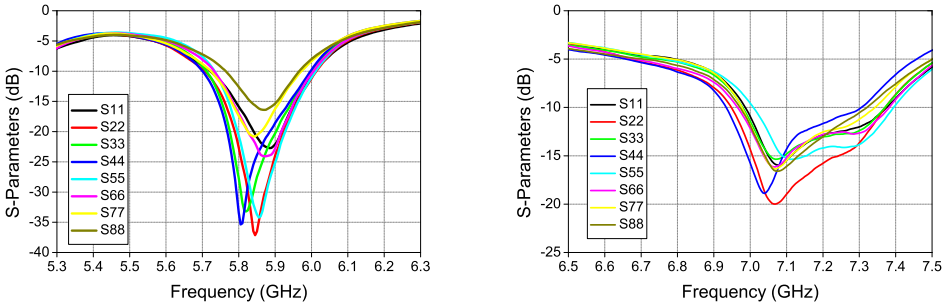


Source: The author.

The measured S-parameters at both bands were performed and small deviations between the ports were verified in both operating frequencies, as it can be seen in Fig. 26. A slight frequency shift can be observed in both bands, but the required bandwidth was still achieved. The main reason for that is the inaccuracy of the air layer thickness of the prototype, especially for dual-frequency and dual-polarization antennas. Therefore, taking into account such difficulties, the results are considered to be acceptable.

Figure 26 – Measured reflection coefficient for both frequencies.

(a) Results at 5.8 GHz. (b) Results at 7.0 GHz.

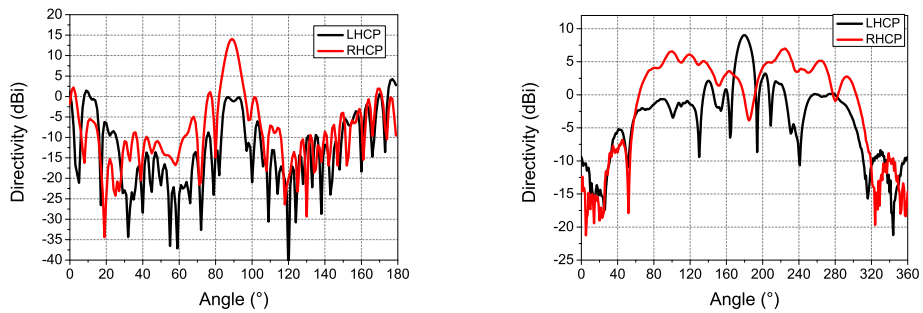


Source: The author.

The radiation patterns were measured at the DLR anechoic chamber and are shown in Fig. 27. The radiation pattern measurements were carried out for each element separately, while the other elements were terminated with matched loads. Then, the resultant radiation pattern was calculated from the vector sum of the measured patterns. One can see that the cross-polarization decoupling is degraded compared to the simulated results. This is also a consequence of the tolerance in the fabircation process, as alignment between the dielectric layers and the air gap thickness. This conclusion were drawn based on the parametric analysis for the dual-band and dual-polarized antenna behaviour described in (PEREIRA, 2015) for the single antenna.

Figure 27 – Measured radiation pattern for both frequencies.

(a) Results at 5.8 GHz. (b) Results at 7.0 GHz.



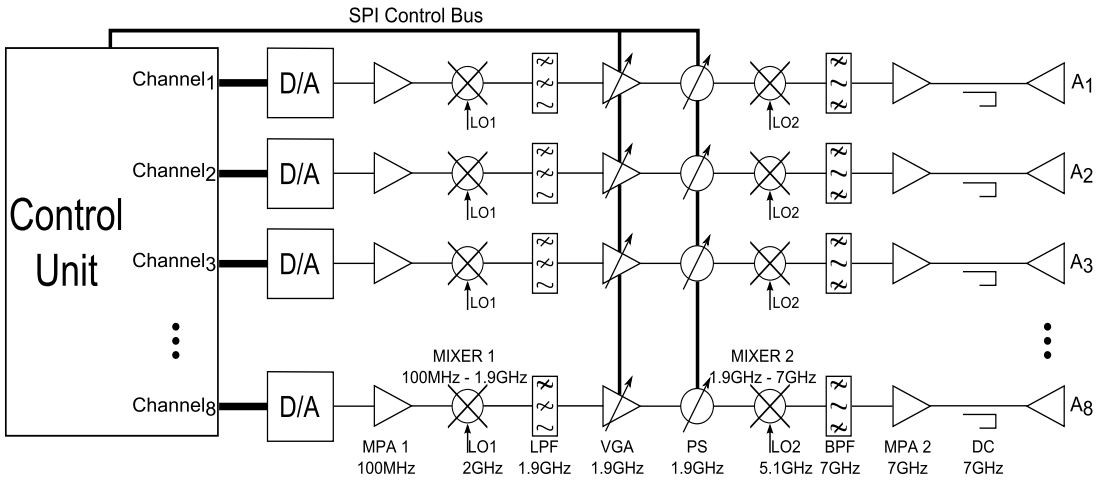
Source: The author.

3 RF Front-end Circuits

The second goal of this work is the design of Tx-circuitry. This work has been partially done in collaboration with the German Aerospace Center (DLR). In the following sections, the design and measurements of the RF components are presented. The goal is to develop the Tx-circuitry with low cost and by using off-the-shelf components.

The initial architecture of the Tx-circuitry is shown in Fig. 28. It is composed of two stages of amplification (MPA1 and MPA2) to compensate the insertion loss of the passive components, and to amplify the signal that is generated by the FPGA. Also, two stages of mixers (MIXER1 and MIXER2) are necessary due to the low operation frequency of the digital-to-analog converters (D/As) (100 MHz) compared to the RF frequency required for the transmission signal. Then, the variable gain amplifiers (VGA) and the phase shifters (PS) are used to control the amplitude and phase to be provided to each antenna to perform the beamforming. Some stages of filters (LPF and BPF) to cutoff the undesired frequency range and directional couplers (DC) for calibration and verification of the signal were desgined.

Figure 28 – Initial architecture for the Tx-circuitry.



Source: The author.

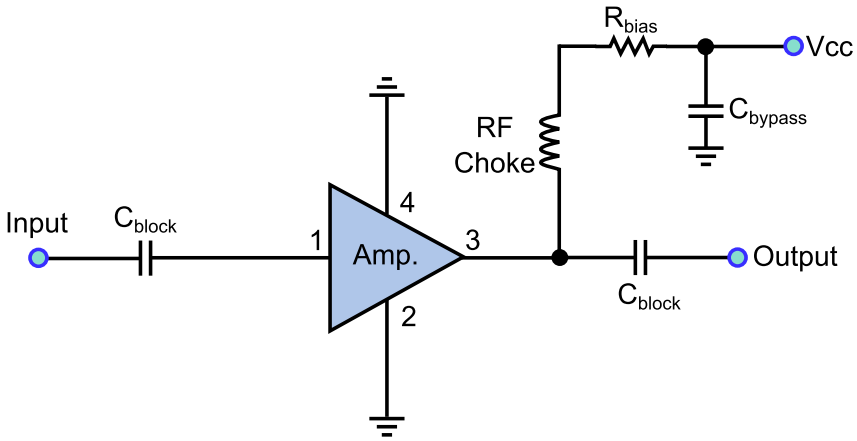
For the designed PCBs, some specifications to reach the best performance as possible were followed. The RF chokes must be positioned near of the RF lines in order to decrease the losses. For good impedance matching, the RF lines (coplanar waveguides - CPW) must be designed with width of 1.5 mm and gap of 0.5 mm. The lines were designed with bends of exactly 45 ° of inclination in the corners to keep a good signal propagation. Connections to ground using via holes to reduce ground path inductance were used.

3.1 Design of the Individual Components

3.1.1 Medium power amplifier - first stage

The first stage of medium power amplifier (MPA1) was designed in order to reach the required power level, since the mixers and filtering stages have significant insertion loss. The signal is provided by the digital-to-analog at a maximum frequency of 100 MHz. In this case, the component ERA-1SM+ from Mini-Circuits was chosen. This component is a broadband amplifier that works from DC to 8 GHz, hence being flexible to use in any frequency range of the transmitting channel. Fig. 29 shows the recommended application circuit for ERA-1SM+.

Figure 29 – Electric circuit for the medium power amplifier ERA-1SM+.



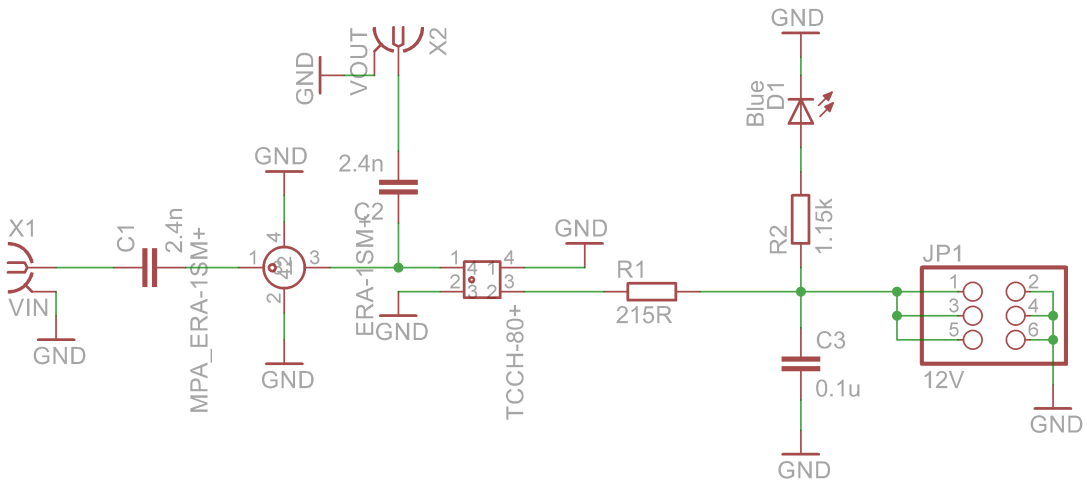
Source: The author.

The external components have the following functions: for the RF_{in}, the use of an external DC-blocking capacitor is required. Regarding the RF_{out}, a blocking capacitor and an RF choke were necessary for the DC feeding. According to the datasheet, the DC feeding can be chosen in a flexible way. In this case, a DC supply of 12 V was used. A resistor for optimum biasing and a capacitor for bypass were used. This capacitor is used to filter out the AC signals. The provided S-parameters specifications from the datasheet are $S_{11} = -30.0$ dB, $S_{12} = -17.0$ dB, $S_{21} = 12.3$ dB and $S_{22} = -26$ dB.

3.1.1.1 First prototype

The second step consists on the electrical schematic design. Following the defined specifications, the schematic was designed and is shown in Fig. 30. As it can be observed, for the MPA1 circuit, the following components were used: pinheads for DC feeding, SMA connectors for the RF input and output, capacitors of 100 pF for DC blocking and 0.1 μF for bypass, resistor of 215 Ω and RF choke TCCH-80+ for biasing.

Figure 30 – Designed schematic for the medium power amplifier ERA-1SM+, first prototype.

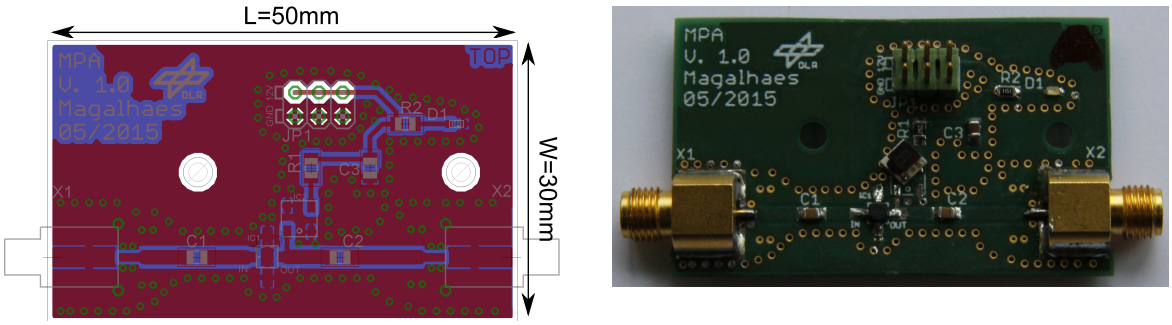


Source: The author.

Once the schematic has been created, the layout has been generated. The components have been organized in order to save space as much as possible, respecting the following rules to keep good performance: adequate spacing between adjacent lines, correct width of the lines and the insertion of vias. Fig. 31 shows the final layout designed on EAGLE and the prototype.

Figure 31 – Layout designed for the medium power amplifier ERA-1SM+, first prototype.

(a) EAGLE layout. (b) Prototype.

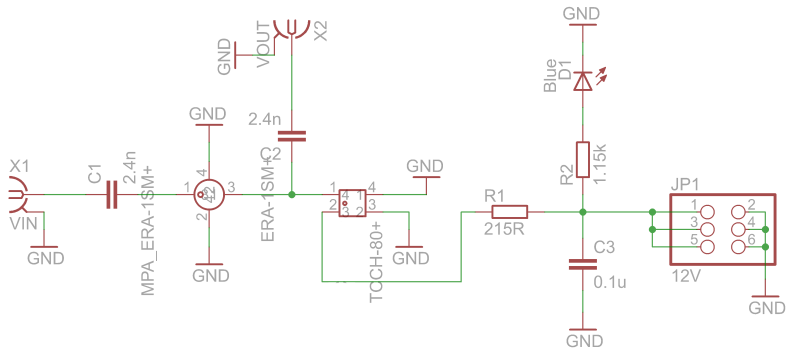


Source: The author.

3.1.1.2 Second prototype

In the first stage of medium power amplifier, a new design was necessary to improve the performance and correct the RF choke soldering, which was provided wrongly in the datasheet of the component. The final schematic is shown in Fig. 32. Fig. 33 shows the final layout designed on EAGLE and the new prototype.

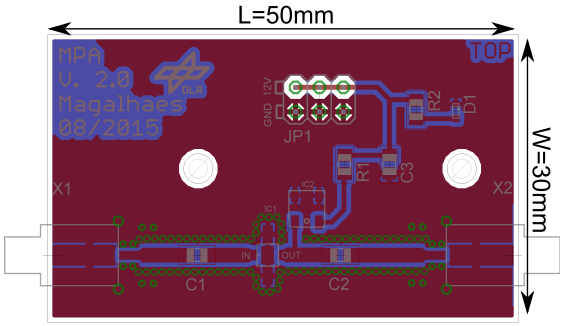
Figure 32 – Schematic designed for the medium power amplifier ERA-1SM+, second prototype.



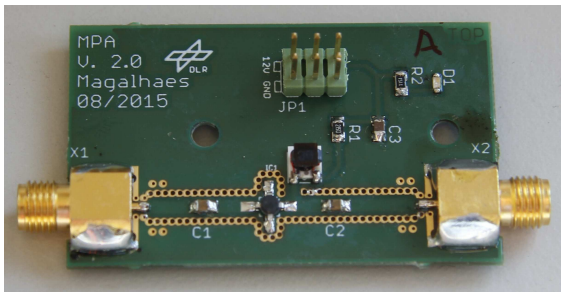
Source: The author.

Figure 33 – Layout designed for the MPA ERA-1SM+, second prototype.

(a) EAGLE layout.



(b) Prototype.

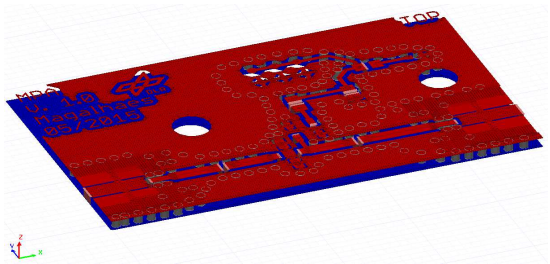


Source: The author.

3.1.1.3 Measurement and simulation results

For the first production of medium power amplifier, the PCB simulation was performed. The details about PCB simulation are described in Chapter 4, where a step-by-step procedure on how to simulate PCBs using Ansys software is given. Fig. 34 shows the simulated PCB in the HFSS/Designer software.

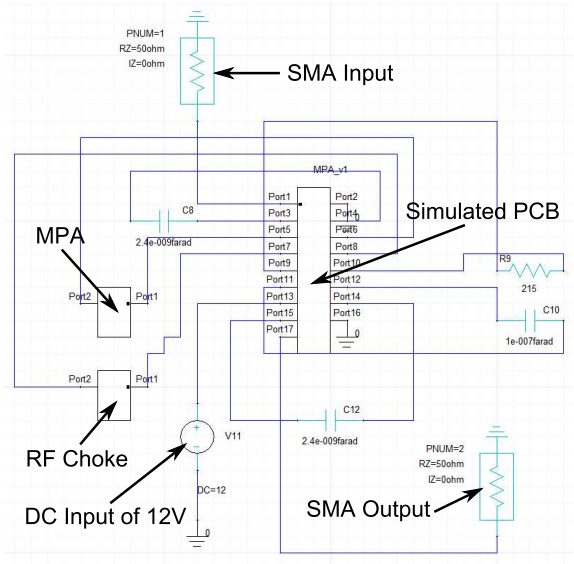
Figure 34 – Electromagnetic model of the PCB for the medium power amplifier ERA-1SM+, first prototype.



Source: The author.

Then, with the simulated PCB and the definition as an N-Port model in the circuit design, the components ERA-1SM+, resistors and capacitors may be connected to perform the final simulation. The simulated circuit is shown in Fig. 35.

Figure 35 – Schematic circuit for the MPA ERA-1SM+, first prototype.

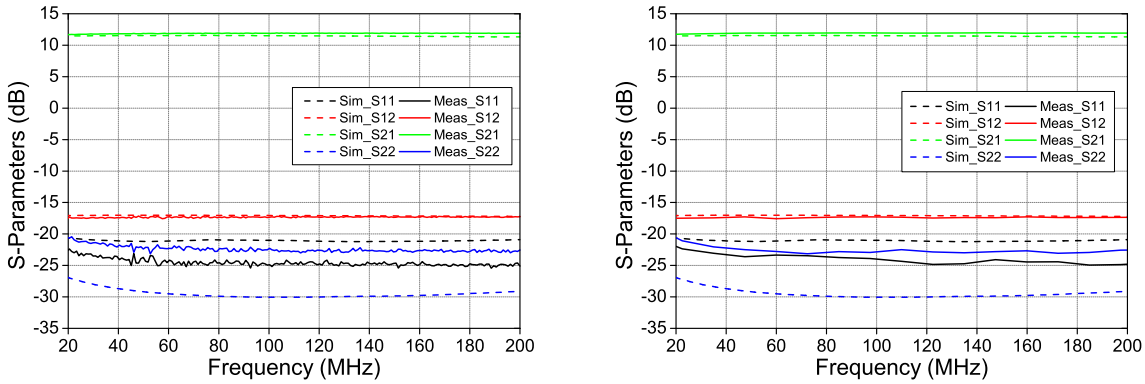


Source: The author.

In order to compare the simulation and measured results, the S-parameters were traced in the same graph. As it can be observed in Fig. 36, the simulated and measured results are similar, hence proving that the simulation is a good option to analyze the RF behaviour before the assembly. To check the reproducibility, more than one PCB were soldered and measured. Therefore, the letters A and B stand for the different PCBs assembled.

Figure 36 – Simulated and measured results for the assembled PCBs of medium power amplifier ERA-1SM+, first prototype.

(a) PCB-A. (b) PCB-B.

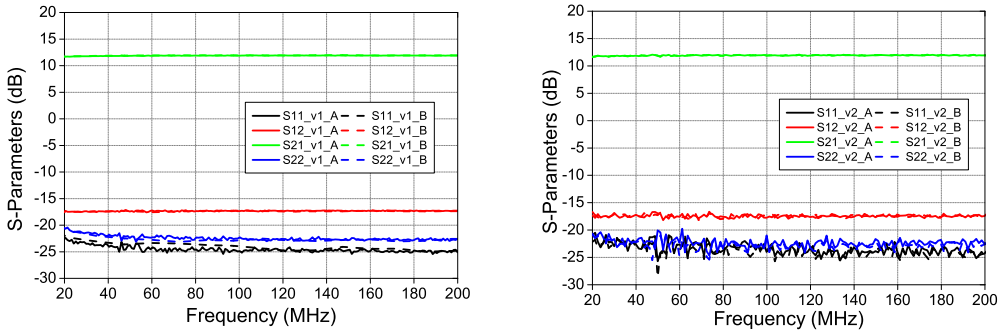


Source: The author.

Fig. 37 shows the measured S-parameters for both prototype versions. As it can be observed, good results based on the component specifications in terms of reflection and transmission coefficients were obtained. The gain in the operation frequency of 100 MHz was 12.3 dB, which is in agreement with the performance given by the manufacturer.

Figure 37 – Measured results for both prototypes of medium power amplifier ERA-1SM+.

(a) First prototype (v_1). (b) Second prototype (v_2).



Source: The author.

3.1.2 Mixer - first stage

The first stage of frequency translation (MIXER1) has the function to convert the signal from 100 MHz to 1.9 GHz. This is needed due to the operating band of the phase shifter. To design the mixer electrical circuit, some specifications must be defined. The local oscilator (LO) frequency is chosen from the required intermediate frequency (IF) and RF signals, generating an output at 1.9 GHz. For this purpose, the LO frequency chosen was 2.0 GHz, and the two RF output signals are given by:

$$RF_{out1} = LO - RF_{in} = 1.9 \text{ GHz} \tag{3.1}$$

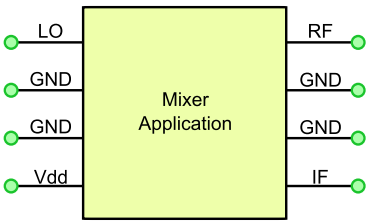
$$RF_{out2} = LO + RF_{in} = 2.1 \text{ GHz} \tag{3.2}$$

For active circuits (DC feeding system), the use of external DC blocking capacitor is necessary at the IF_{in} and RF_{out} signals. For passive circuits (without DC feeding), this is not necessary, since there is no DC signal through the circuit. In the active case, the DC voltage for the LO amplifier was 3.3 V. Also, one external RF bypass capacitor is required as for the MPA. For the MIXER1 stage, two prototypes were desgined. In the first prototype, the active mixer device HMC422 was used. The manufacturer specifications are conversion loss of 8 dB and LO power of 0 dBm. For the second prototype, the passive mixer device HMC316 was tested. The manufacturer specifications are conversion loss of 8 dB and LO power of 15 dBm.

3.1.2.1 First prototype

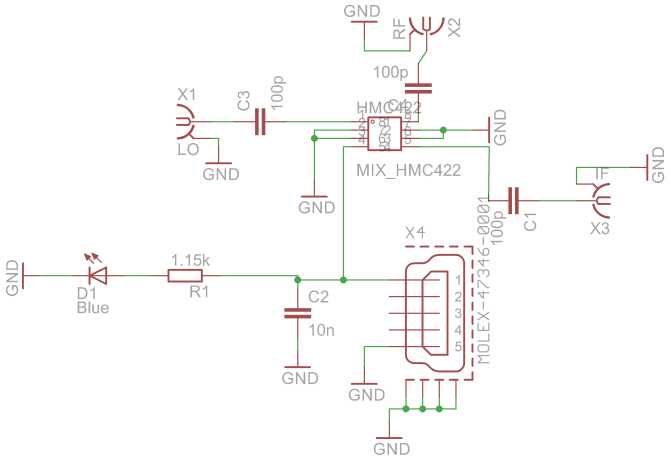
Fig. 38 shows the connections of the active mixer. The schematic is shown in Fig. 39. For proper operation, components as mini USB for DC feeding, SMD capacitors of 100 pF for DC blocking, capacitor of 0.1μF for bypass and SMA connectors of 50 Ω for LO, IF and RF were used. Fig. 40 shows the final layout designed and the prototype produced for the MIXER1 stage.

Figure 38 – Device connections for the MIXER1 stage, first prototype.



Source: The author.

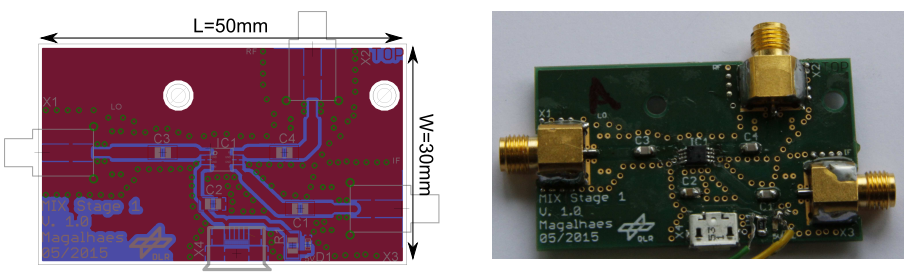
Figure 39 – Schematic designed for the MIXER1 stage, first prototype.



Source: The author.

Figure 40 – Layout designed for the MIXER1 stage, first prototype.

(a) EAGLE layout. (b) Prototype.

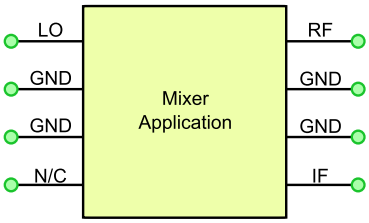


Source: The author.

3.1.2.2 Second prototype

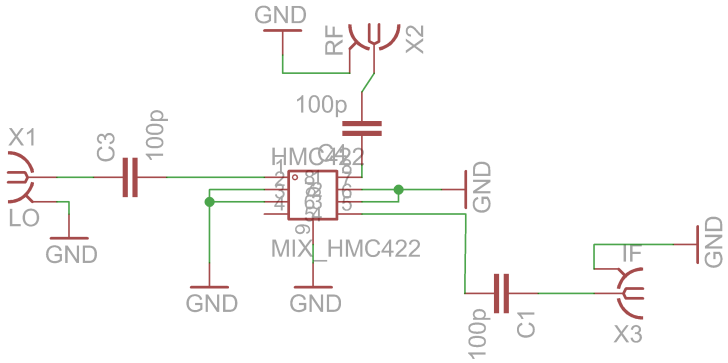
In the second prototype of the same MIXER1 stage, some adjustments in the PCB layout were required due the different device characteristics. Fig. 41 shows the device connections of the passive mixer. The schematic is shown in Fig. 42. As it can be observed, by comparing both productions, this component does not need a DC feeding nor bypass or blocking capacitors due the presence of only AC signal. Fig. 43 shows the final layout designed and the prototype.

Figure 41 – Device connections for the MIXER1 stage, second prototype.



Source: The author.

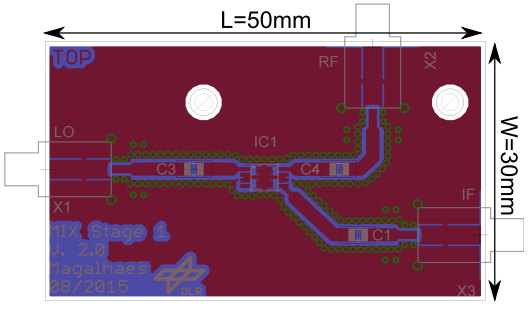
Figure 42 – Schematic designed for the MIXER1 stage, second prototype.



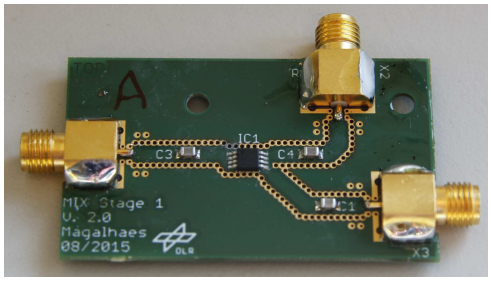
Source: The author.

Figure 43 – Layout designed for the MIXER1 stage, second prototype.

(a) EAGLE layout.



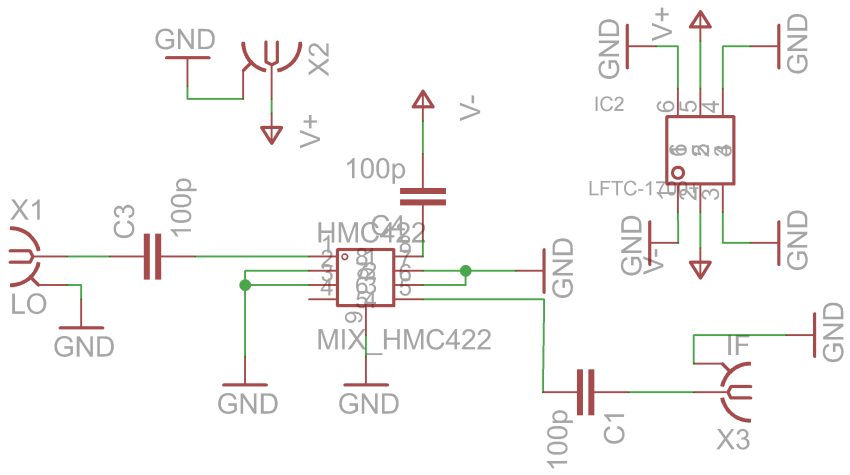
(b) Protoype.



Source: The author.

Another test was done with the mixer with an integrated monolitic filter. The used low-pass filter is the LFTC-1700, which was used to cutoff the image frequency higher than 1.95 GHz. For this design, the passive mixer used for the second production was considered. The electrical schematic circuit was designed and is shown in Fig. 44. Fig. 45 shows the final layout designed and the prototype.

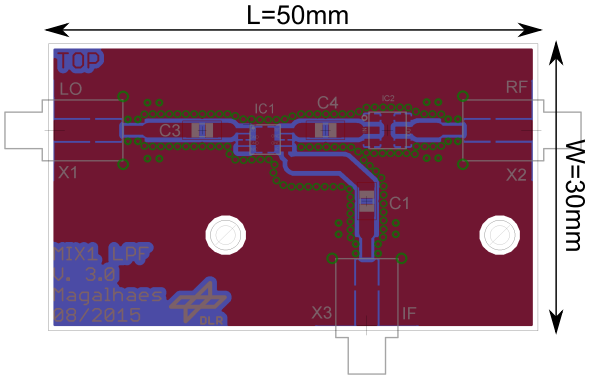
Figure 44 – Schematic designed for the MIXER1 stage with filtering, second prototype.



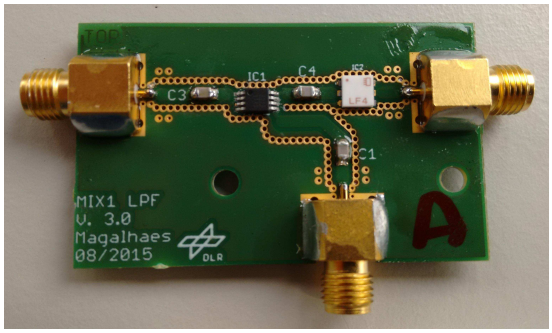
Source: The author.

Figure 45 – Layout designed for the MIXER1 stage with filtering, second prototype.

(a) EAGLE layout.



(b) Prototype.



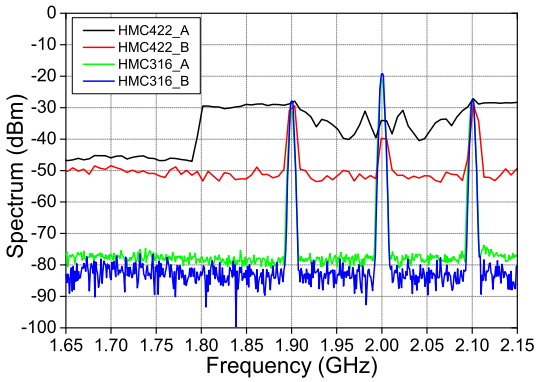
Source: The author.

3.1.2.3 Measurement results

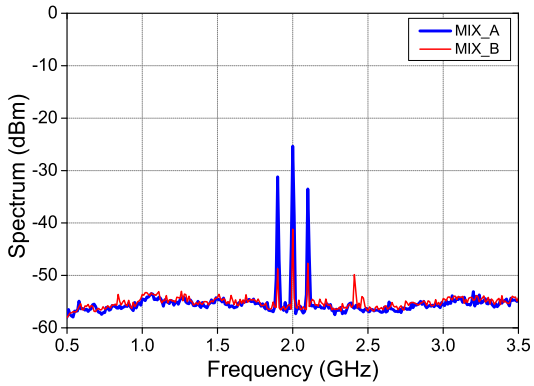
Since the manufacturers of the employed mixers do not provide the required S-parameters files (.s3p or touchstone format), it was not possible to simulate the PCB. Therefore, only the measurement results are shown in Fig. 46, where the cases with and without filtering stage are plotted.

Figure 46 – Measurement results for the MIXER1 stage.

(a) Without filtering stage, both prototypes.



(b) With filtering stage, second prototype.



Source: The author.

As it can be observed in Fig. 46, the results are presented in terms of spectrum as a function of the frequency. The RF output signal is a combination of the LO and IF as commented previously. Therefore, there are two generated signals by the combination of the $LO = 2$ GHz and the $IF = 100$ MHz: the sum resulting at 2.1 GHz and the subtraction resulting at 1.9 GHz, which is the desired frequency for the RF output. The active mixer did not present good results based on the component specifications in terms of spectrum. Although the needed LO power is lower than the RF signal level, the disadvantage of such circuit is the sensibility. During the tests, several mixers burned and, therefore, it was not possible to check the reproducibility. For two prototypes of this PCB (A and B), just one worked properly.

Both passive mixers worked well based on the component specifications as shown in Fig. 46. Due to the stability of passive devices, this mixer was chosen to the implementation of the Tx-circuitry. Also, the expected performance was reached in terms of conversion loss (around 8 dB). Prototypes A and B for the passive mixer resulted in very similar results; hence reproducibility has been verified.

3.1.3 Low-pass filter operating at 1.9 GHz

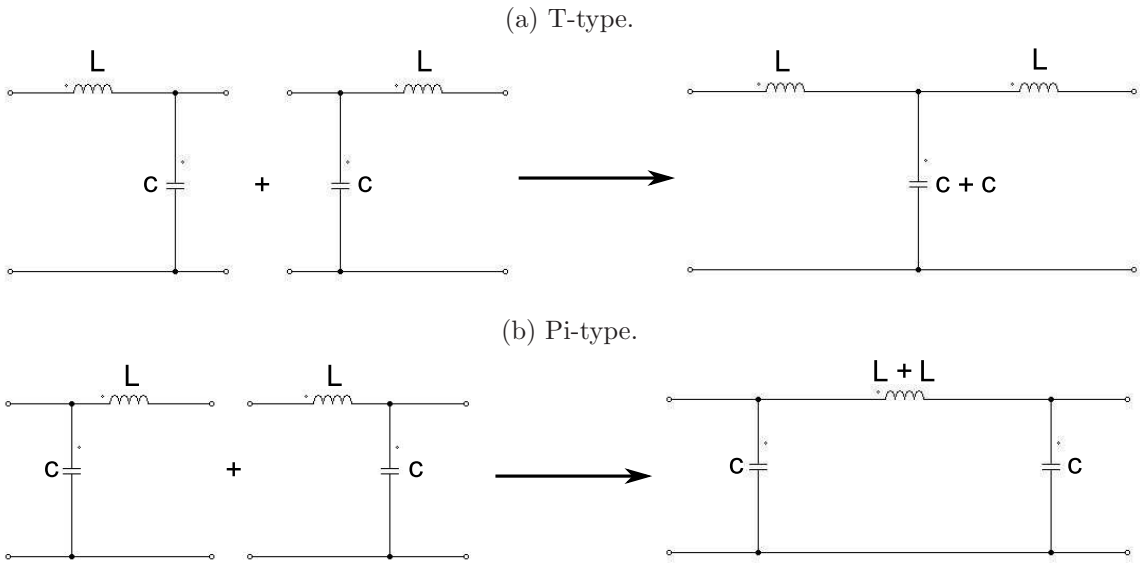
In many projects, the use of filters are of extreme importance, since just a desired frequency range can be processed, decreasing the performance deterioration generated by interferences. The use of filters allows keeping the frequency range and cutoff the undesired signal. However, is not easy to find a filter that operates at 5.8 GHz and 7.0 GHz with small size and low cost. A design of Low-Pass Filter (LPF) and Band-Pass Filter (BPF) using coplanar waveguide (CPW) technology were defined. For frequencies of 7.0 GHz and 1.9 GHz, the FR4 substrate was chosen. This substrate is commonly used for circuit applications, since it is cheap and easily available in the market. Also, this allows integra-

ting the filters directly into the Tx-circuitry. One technique to design filters in CPW is to convert an electrical circuit into a distributed equivalent microstrip. As known from the literature, low-pass filters can be formed by the association of capacitors and inductors (SAYRE, 2001).

The first step consists in defining the design specifications for the LPF: operation frequency of $f = 1.9$ GHz, input and output impedance of $R_0 = 50\ \Omega$, inductors impedance of $Z_1 = 120\ \Omega$, and capacitors impedance of $Z_2 = 20\ \Omega$. The FR4 material used at DLR has the dielectric constant of $\varepsilon_r = 4.4$, loss tangent of $\delta = 0.02$ and thickness of 1.0 mm. The FR4 material used at UNIPAMPA has different thickness of 1.6 mm. For this reason, new optimizations of the model were necessary. This choice was made considering that this filter will be integrated into the Tx-circuitry to cutoff the undesired frequency range generated by the MIXER1 stage.

For the LPF, a ninth order topology was chosen. As known, when the order is increased, the attenuation also increases. The inductances and capacitances necessary to design the filter will be defined in the next sections. For such kind of filter, two configurations of series inductors and shunt capacitors were used: the LPF T-type and Pi-Type. Fig. 47 shows the different topologies.

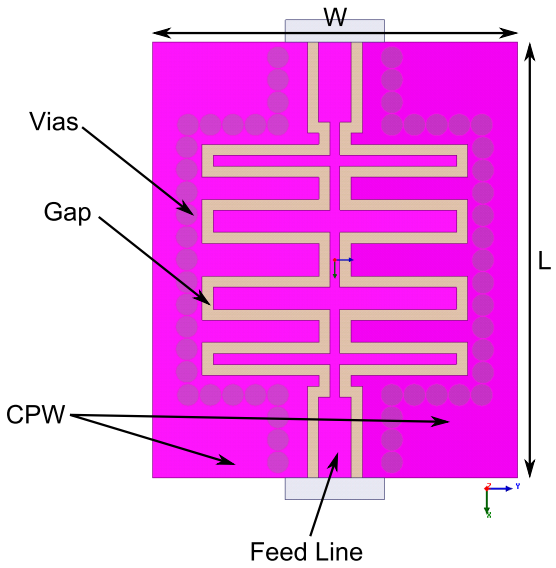
Figure 47 – Different techniques to merge LC circuits in LPF designs.



Source: The author.

The LPF was designed considering the coplanar waveguide technology, as shown in Fig. 48. As it can be seen, such model is composed of the feed line composed coplanar waveguide with gap of 0.5 mm between the feed line and ground. The vias act as a shield for the RF signal around the RF lines, thereby, decreasing the losses.

Figure 48 – Adopted structure for the LPF design.



Source: The author.

3.1.3.1 Calculation of the initial parameters

To define the cutoff frequency (f_c), it is necessary to multiply f by a correction factor (ADJ) to avoid that f_c decreases with the increase of the filter order. This is referred as the cascade effect, when there are two or more combinations of half-sections (SAYRE, 2001). Table 6 shows the ADJ factor as a function of the number of sections.

Table 6 – Correction factor for different number of sections.

Number of Sections (1/2 Section = 2 Poles)	ADJ Factor
0.5	1.00
1.0	1.05
1.5	1.10
2.0	1.15
2.5	1.20
3.0	1.25

Source: The author.

If one pole is equivalent to 1/4 sections, then the number of sections for a ninth order filter is $9/4 = 2.25$ and the ADJ factor will be 1.175. In order to guarantee that the center frequency of the IF signal is located in the pass-band of the filter, a margin of $BW = 100$ MHz has been considered. Therefore, the cutoff frequency will be

$$f_c = (f + BW)ADJ = (1.9 \text{ GHz} + 100 \text{ MHz})1.175 = 2.35 \text{ GHz} \tag{3.3}$$

After calculating the cutoff frequency, it is possible to define the primary inductances and capacitances using the following equations

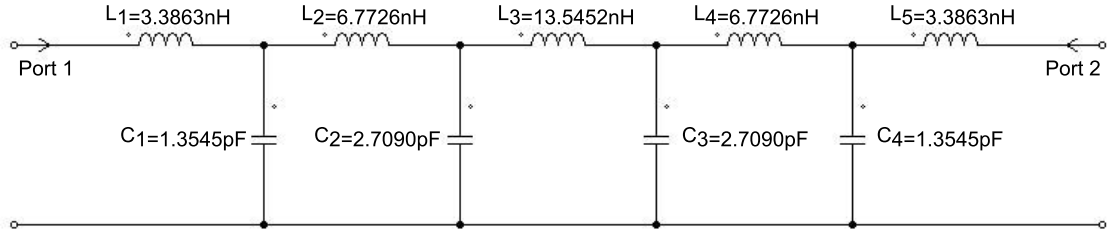
$$L = \frac{R_0}{2\pi f_c} = 3.3863 \text{ nH} \tag{3.4}$$

$$C = \frac{1}{2\pi f_c R_0} = 1.3545 \text{ pF} \tag{3.5}$$

3.1.3.2 Definition of the electrical circuit

Using the logic of half-sections applied to a ninth order LPF, the resulting electrical circuit considering the inductances and capacitances calculated above is shown in Fig. 49.

Figure 49 – Defined electrical circuit for the LPF operating at 1.9 GHz.

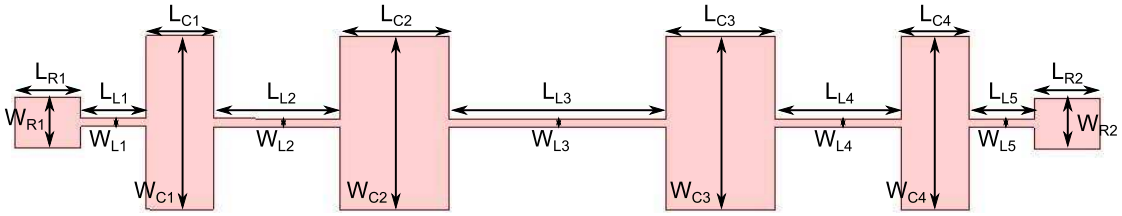


Source: The author.

3.1.3.3 Convertion of the components to equivalent microstrip lines

After the LPF electrical circuit has been designed, it is necessary to convert the lumped model to an equivalent distributed structure. Some calculations can be performed to estimate the width and the length of each microstrip line. Fig. 50 shows a microstrip structure using equivalent microstrip sections.

Figure 50 – Microstrip lines equivalent to lumped components.



Source: The author.

The lengths and widths can be calculated using the proper equations to calculate the electrical lengths, and determinating the width through the required impedance; or using an estimation software as Txline (free software available online) to estimate both

parameters considering the defined specifications. If the first method is chosen, Eq. (3.6) for capacitors and (3.7) for inductors can be used.

$$L_C = \lambda(tan^{-1}(6.28 f_c 20C)) \tag{3.6}$$

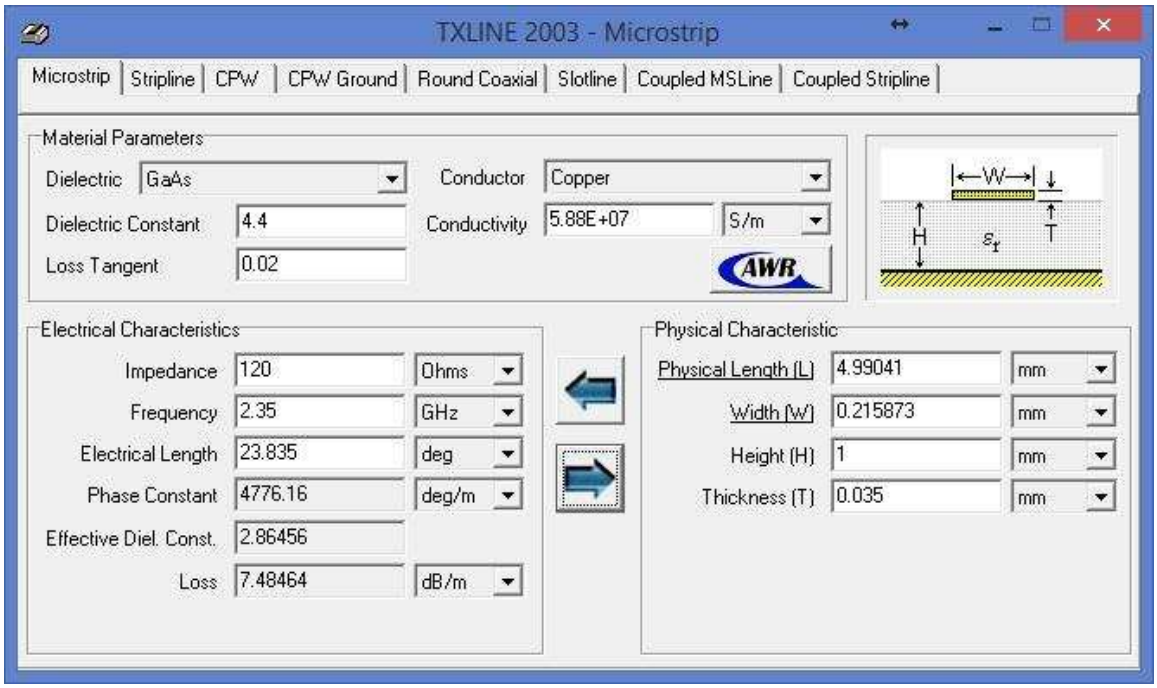
$$L_L = \lambda(sin^{-1}(\frac{6.28 f_c L}{120})) \tag{3.7}$$

$$\beta l_C = \frac{C' Z_0}{R_0} \tag{3.8}$$

$$\beta l_L = \frac{L' R_0}{Z_0} \tag{3.9}$$

To reduce the calculations, the use of the Txline software to estimate the widths and lengths for each component was considered. To obtain the electrical length, Eq. (3.8) for capacitors and (3.9) for inductors were used. The parameters L' and C' are normalized values and Z_0 is the impedance of each component. The width and length for each section can be obtained calculating the electrical length and using the Txline software. Fig. 51 shows an example using the Txline for FR4 material in order to obtain the required parameters for the design.

Figure 51 – Width and length estimation using Txline at 2.35 GHz.



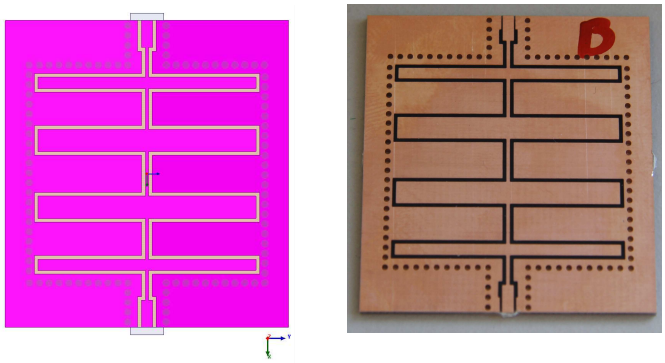
Source: The author.

3.1.3.4 Simulation of LPF using HFSS software

As the structure and the sizes of each lines were defined, the LPF can be designed using the FR4 substrate. For this design, the initial parameters are the obtained values with Txline. After that, some optimizations were performed. Fig. 52 presents the designed structure using HFSS and the prototype.

Figure 52 – Designed LPF using FR4 material.

(a) HFSS layout. (b) Protoype.



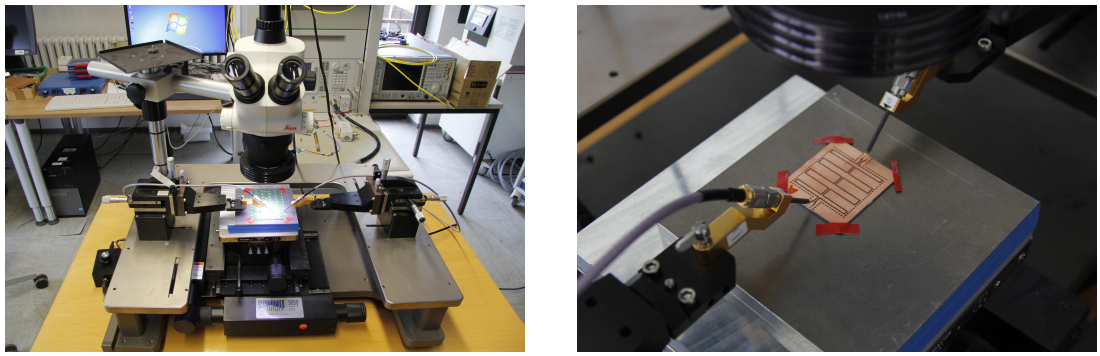
Source: The author.

3.1.3.5 Measurement and simulation results

The measurements of the filters were performed employing a probe station measurement facility, available at DLR, as shown in the Fig. 53. This equipment allows measuring the filter without the influence of connectors. The resulting S-parameters are shown in Fig. 54. The measurement is very similar to the simulations reaching the expected performance. The final dimensions are shown in Table 7. The total length (L) is 41.3 mm.

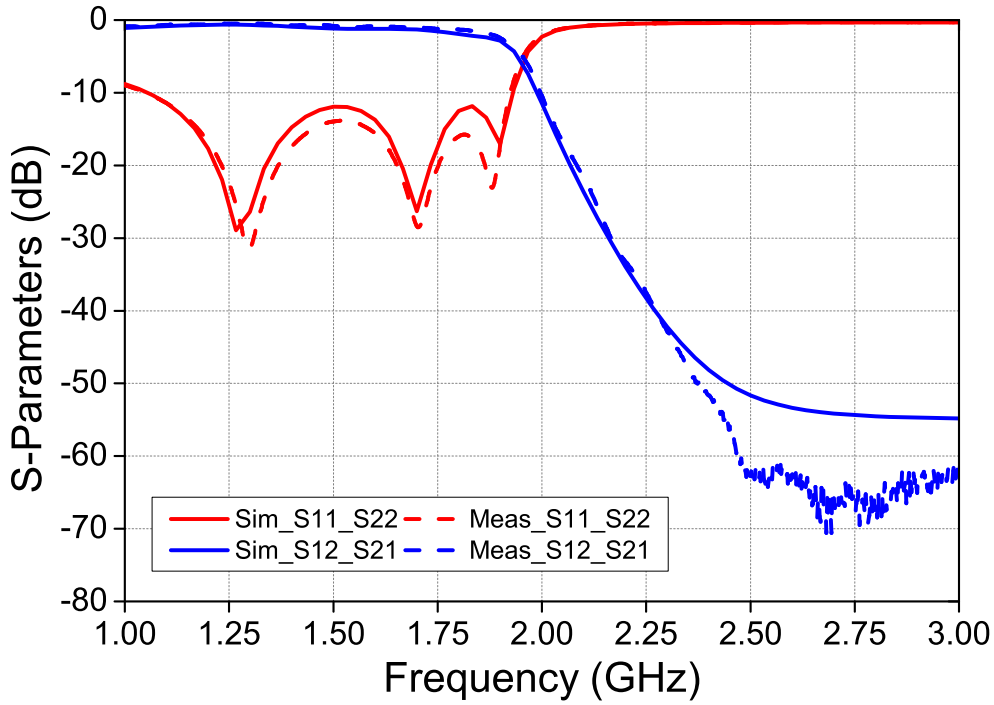
Figure 53 – Probe station to measurements of PCBs.

(a) Probe station. (b) Filter measurement.



Source: The author.

Figure 54 – S-parameters for the LPF operating at 1.9 GHz.



Source: The author.

Table 7 – Final dimensions for the LPF design in CPW technology at 1.9 GHz.

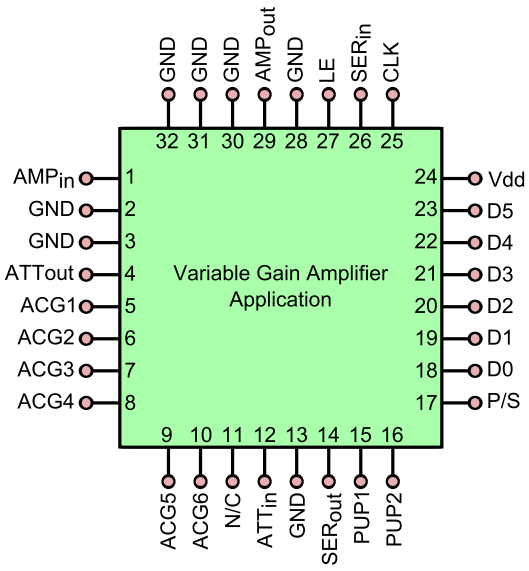
Parameter	Dimension (mm)
L	41.3
W	38.1
$W_{L1,2,3,4,5}$	0.5
$W_{C1,2,3,4}$	29.3
$W_{R1,2}$	1.5
$L_{L1,5}$	4.0
$L_{L2,4}$	5.5
L_{L3}	6.0
$L_{C1,4}$	1.5
$L_{C2,3}$	3.0
$L_{R1,2}$	3.6

Source: The author.

3.1.4 Variable gain amplifier

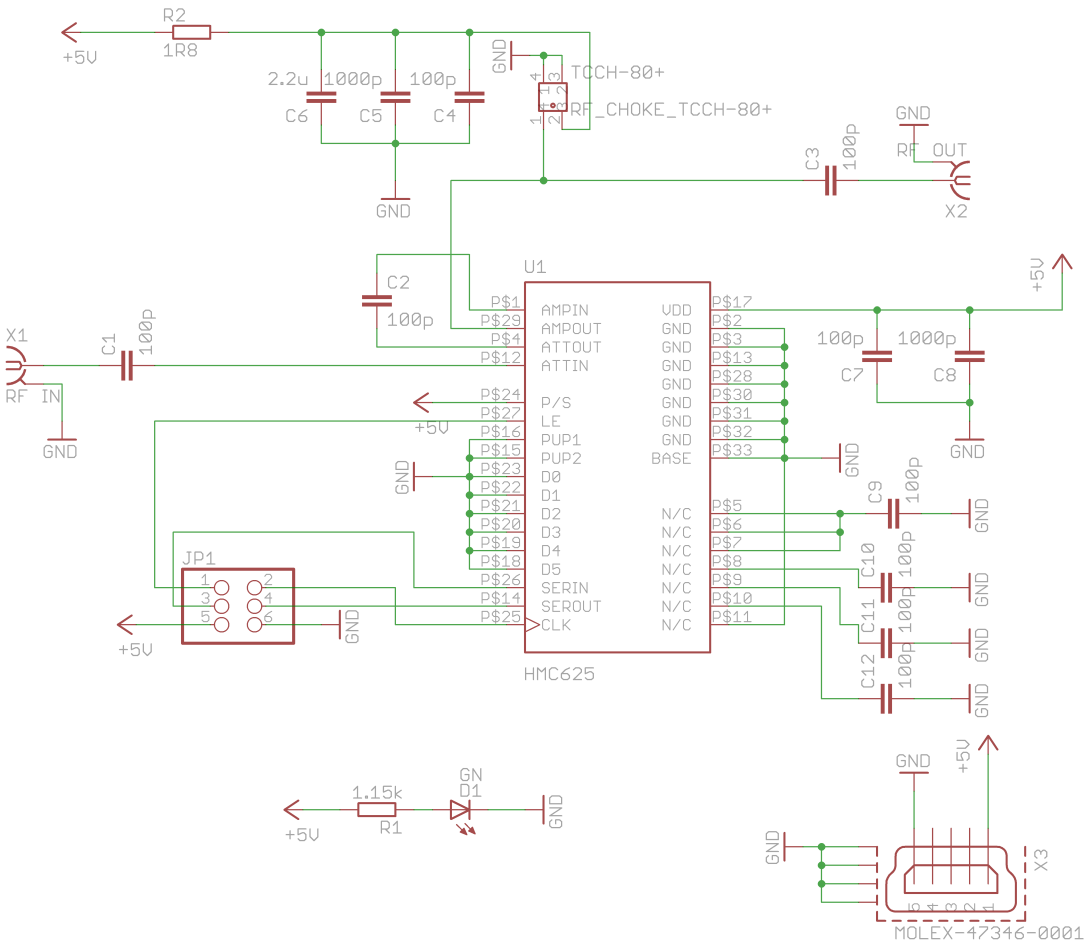
The 6-bit variable gain amplifier (VGA) HMC625ALP5 was chosen in order to deliver the current (amplitude) for each antenna; thus, becoming possible to perform the beamforming. This component operates at a frequency of 1.9 GHz. Fig. 55 shows the recommended application circuit for the VGA. The schematic is shown in Fig. 56. Fig. 57 shows the final layout designed and the prototype.

Figure 55 – Recommended application circuit for the variable gain amplifier.



Source: The author.

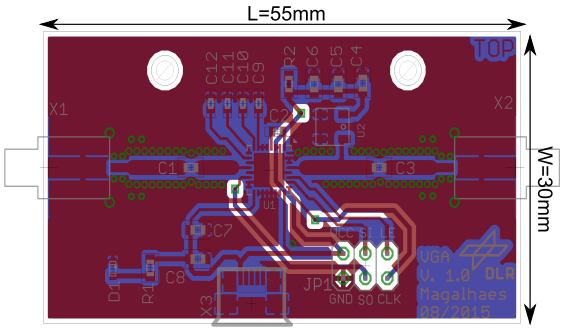
Figure 56 – Schematic designed for the VGA.



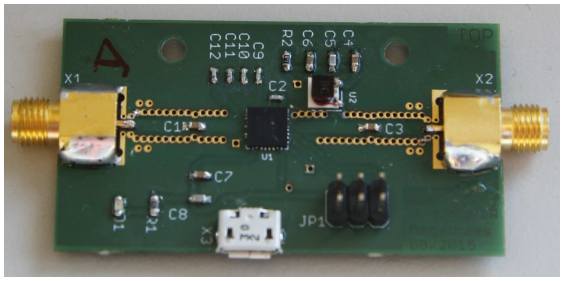
Source: The author.

Figure 57 – Layout designed for the VGA, top view.

(a) EAGLE layout.



(b) Prototype.



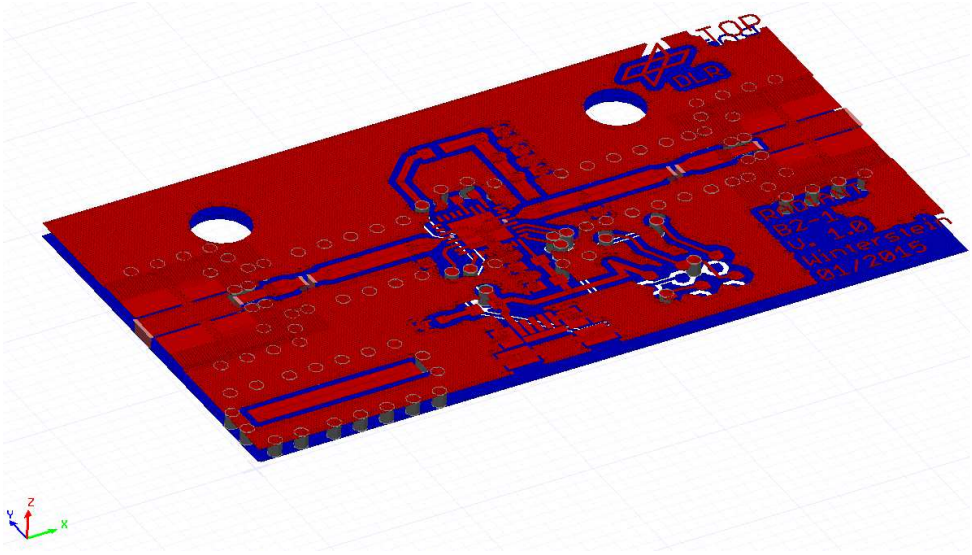
Source: The author.

For the RF_{in}, the use of an external DC blocking capacitor is required and must be chosen for the frequency of operation. For the RF_{out}, the use of DC bias (Vcc) for the amplifier output stage is needed. The necessary DC voltage is 5 V and capacitors for bypass were used. There are two ways to perform the gain control: in serial or in parallel mode. For the desired application, the serial mode is more interesting for interconnection with the control unit (FPGA).

3.1.4.1 Measurement and simulation results

As the device is a broadband amplifier, it can operate at 5.8 GHz (Rx) and in the intermediate frequency of the Tx-circuitry (1.9 GHz). The simulation was done in HFSS and the model is shown in Fig. 58.

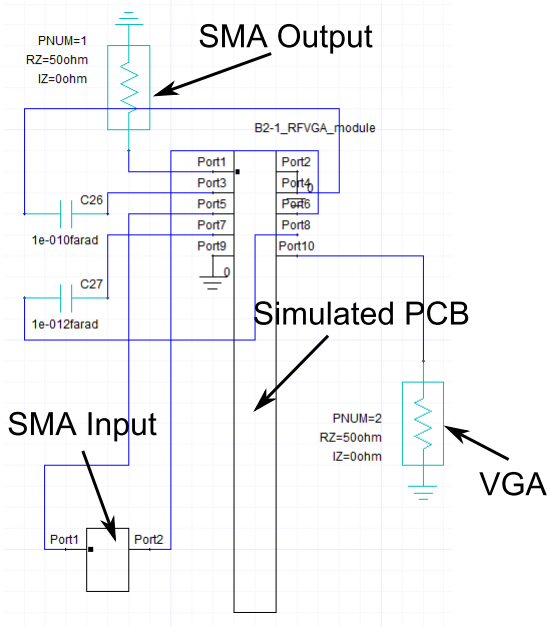
Figure 58 – Simulated PCB for the variable gain amplifier.



Source: The author.

As the PCB simulation has been done, the components may be connected to the N-port model as commented before. The designed circuit is shown in Fig. 59.

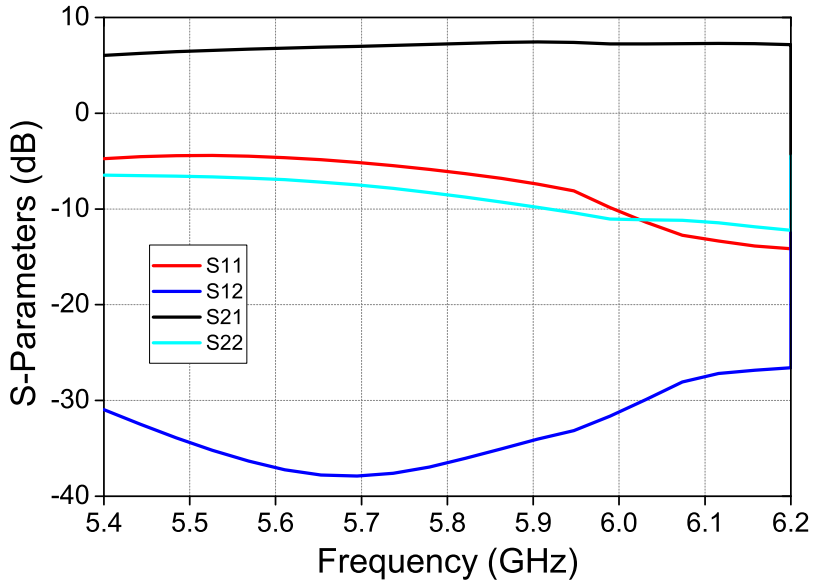
Figure 59 – Designed circuit for the VGA.



Source: The author.

To validate the model, the S-parameters considering the highest gain at 5.8 GHz were obtained and are shown in Fig. 60. The maximum gain obtained at 5.8 GHz was approximately 9 dB.

Figure 60 – Simulated results for the variable gain amplifier.

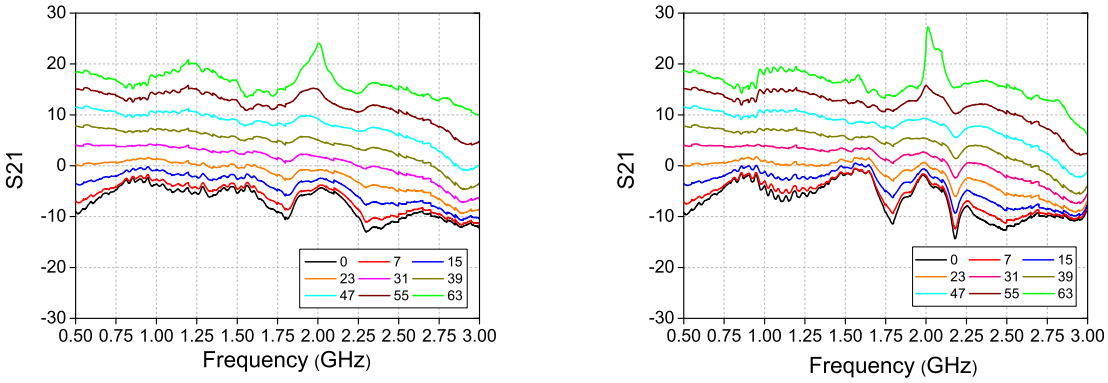


Source: The author

The measurement results for the VGA operating at 1.9 GHz are shown in Fig. 61. As the VGA has 6-bit for control, 64 gain values are possible. For better visualization, only 8 cases were plotted (control bits corresponding to 0, 7, 15, 23, 31, 39, 47, 55 and 63).

Figure 61 – Measured results for two prototypes of the VGA using serial control.

(a) PCB-A. (b) PCB-B.



Source: The author.

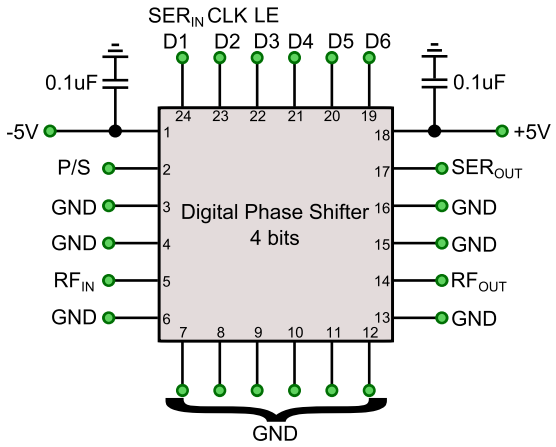
The VGA manufacturer specification provide a range of gain from −13.5 dB to 18 dB. Therefore, a total gain variation of 31.5 dB with 64 possible values results in a gain step of 0.5 dB. As it can be observed at the obtained S-parameters, the reproducibility of the PCBs was validated. Also, the constant variation of 0.5 dB between each state and the maximum gain around 18 dB were achieved. To obtain these results, a serial control through a SPI code was used.

3.1.5 Phase shifter

The phase shifter (PS) MAPS-010143 shall provide each antenna with the required phase. Thus, performing the beamsteering in the desired direction. Fig. 62 shows the recommended application circuit for the phase shifter.

As it can be observed in Fig. 62, the device has 24 ports: 12 ports are used to connect the ground plane (GND), 2 for the RF input and output with external DC blocking capacitor, 2 for the DC voltages of −5 V and 5 V with bypass capacitor. There are two modes of phase control: serial mode and direct parallel mode. The serial mode is activated when the P/S signal is kept high and pins 22, 23, and 24 have the LE, CLK, and SER IN function. While LE is high, CLK is masked to protect the data while the change is implemented, and SEROUT is SERIN delayed by 6 clock cycles. The control is made through an SPI program and FTDI USB cable. The SPI code sets the required pins using a compiler software (C++).

Figure 62 – Recommended application circuit for the phase shifter.



Source: The author.

In serial mode operation, the outputs are constant while LE is kept low. When P/S is set low, the parallel mode is activated. The parallel control depends on setting the pins D3, D4, D5 and D6 to provide the required phase. This setting can be performed manually through a DIP-switch to set up the control bits. In this application, a 5 ports DIP-switch was used for testing, where 1 switch is used to choose between the serial or parallel control and the other 4 switches were used for the control bits. Resistors of 1 MΩ were used to avoid short-circuits in the low level of switching. Table 8 shows the possible phases for the 4-bit phase shifter chosen.

Table 8 – Truth table for 4-bit digital phase shifter.

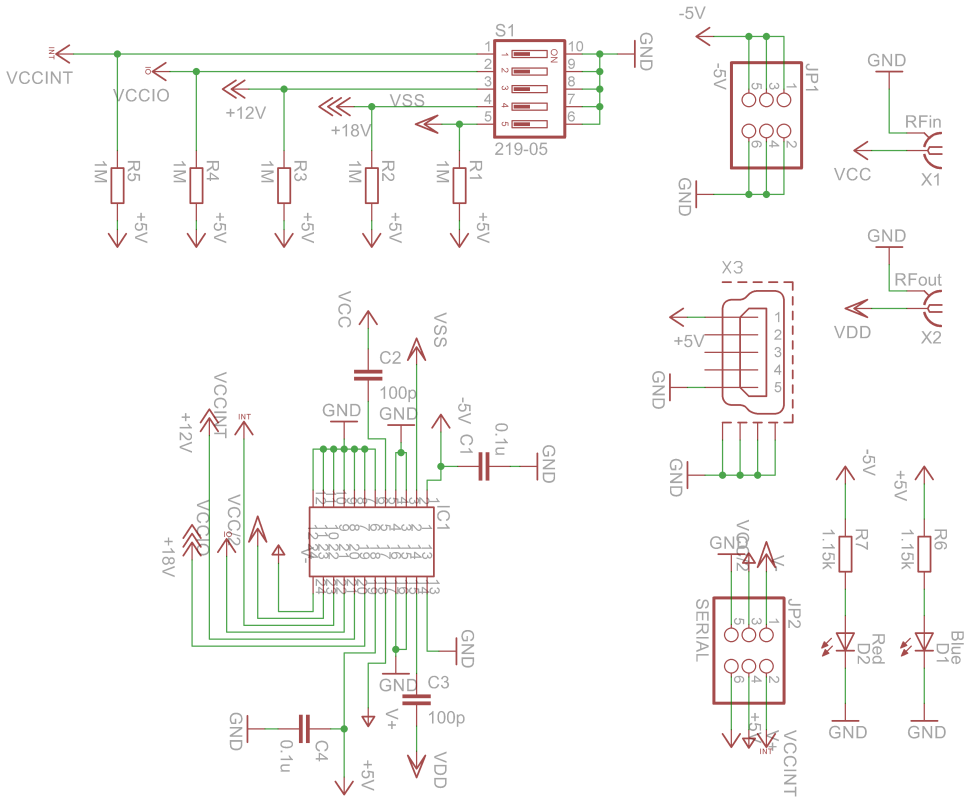
D6	D5	D4	D3	Phase Shift (°)
0	0	0	0	0.0
0	0	0	1	22.5
0	0	1	0	45.0
0	0	1	1	67.5
0	1	0	0	90.0
0	1	0	1	112.5
0	1	1	0	135.0
0	1	1	1	157.5
1	0	0	0	180.0
1	0	0	1	202.5
1	0	1	0	225.0
1	0	1	1	247.5
1	1	0	0	270.0
1	1	0	1	292.5
1	1	1	0	315.0
1	1	1	1	337.5

Source: The author.

3.1.5.1 First prototype

Following the defined specifications, the schematic was created and is shown in Fig. 63. The phase shifter layout was designed using the initial schematic connections. Fig. 64 shows the final layout designed and the prototype for the PS with all soldered components.

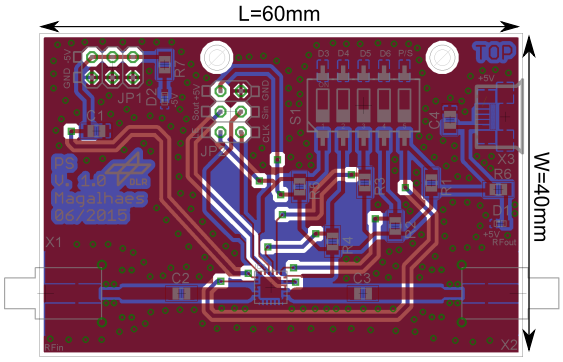
Figure 63 – Schematic designed for the phase shifter, first prototype.



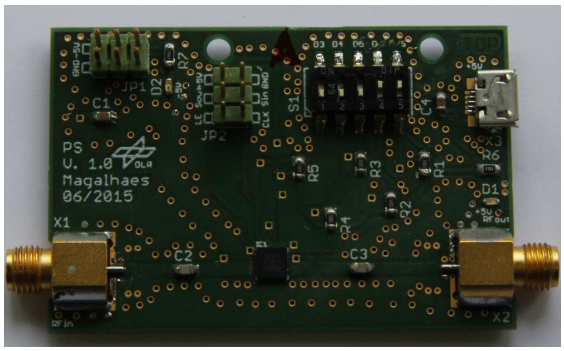
Source: The author.

Figure 64 – Layout designed for the phase shifter, first prototype.

(a) EAGLE layout.



(b) Prototype.

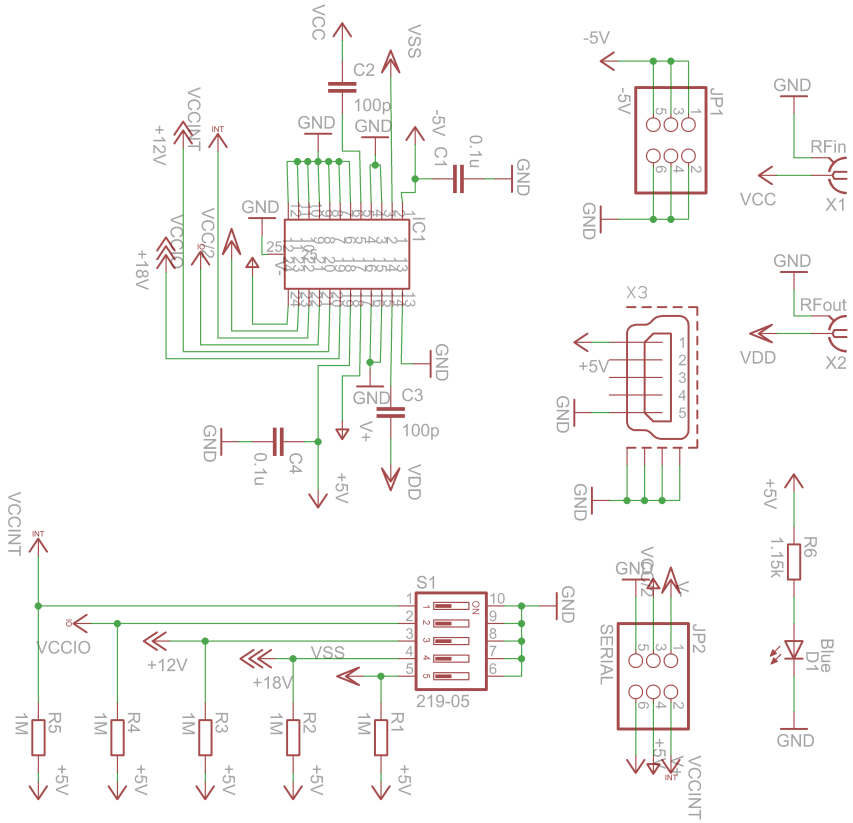


Source: The author.

3.1.5.2 Second prototype

As commented before, small adjustments to improve the performance in the signal propagation were necessary, such as new positioning of some vias and DC lines connection. For the new phase shifter design, the schematic is shown in Fig. 65. The phase shifter layout and prototype can be seen in Fig. 66.

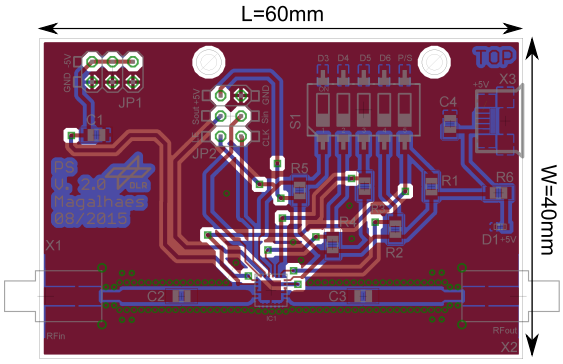
Figure 65 – Schematic designed for the phase shifter, second prototype.



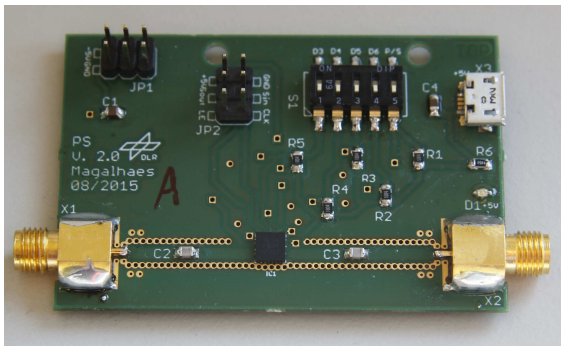
Source: The author.

Figure 66 – Layout designed for the phase shifter, second prototype.

(a) EAGLE layout.



(b) Prototype.

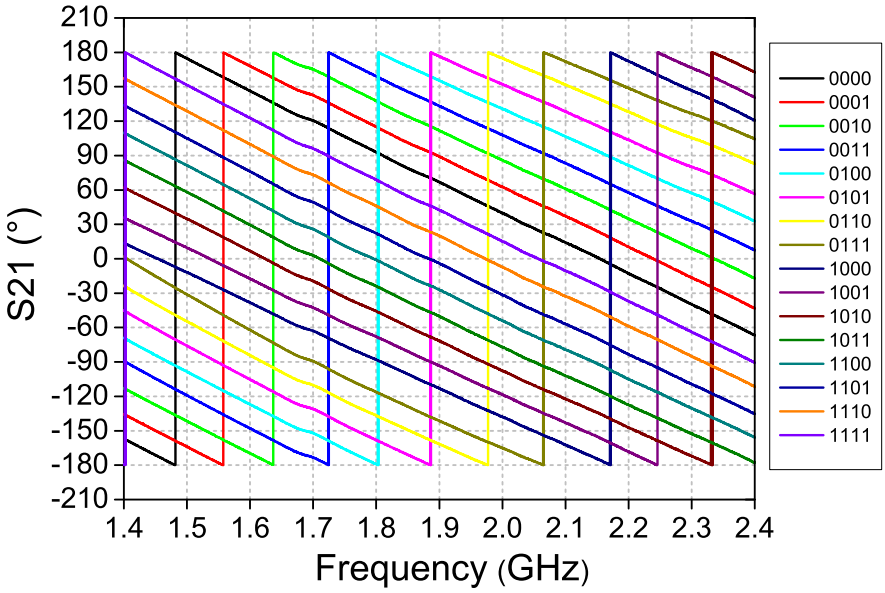


Source: The author.

3.1.5.3 Measurement results

The results for the first prototype were obtained using parallel control and for the second prototype with serial control. These results are shown in Fig. 67, showing the 16 possible phase values that the 4-bit digital phase shifter can provide. The variation of 22.5 ° for each bit state was achieved. Both prototypes worked well based on the component specifications. Because the serial control is more suitable and the SPI control can be implemented in the control unit this was the chosen mode to control the phase shifter. Good results in terms of constant variation of the transmission coefficient for each step were observed.

Figure 67 – Measured phase of the S21-parameter for the digitally controlled phase shifter.



Source: The author.

3.1.6 Mixer - second stage

The second stage of mixing (MIXER2) was implemented using the HMC220AMS8 device for converting the signal from 1.9 GHz to 7.0 GHz. The same schematic and connections used in Fig. 41 were used in this stage, but the local oscilator (LO) is different due to the required output RF frequency at 7.0 GHz. Thus, the LO frequency calculated was 5.1 GHz. The two components of the output signal are given by

$$RF_{out1} = LO - RF_{in} = 3.2 \text{ GHz} \tag{3.10}$$

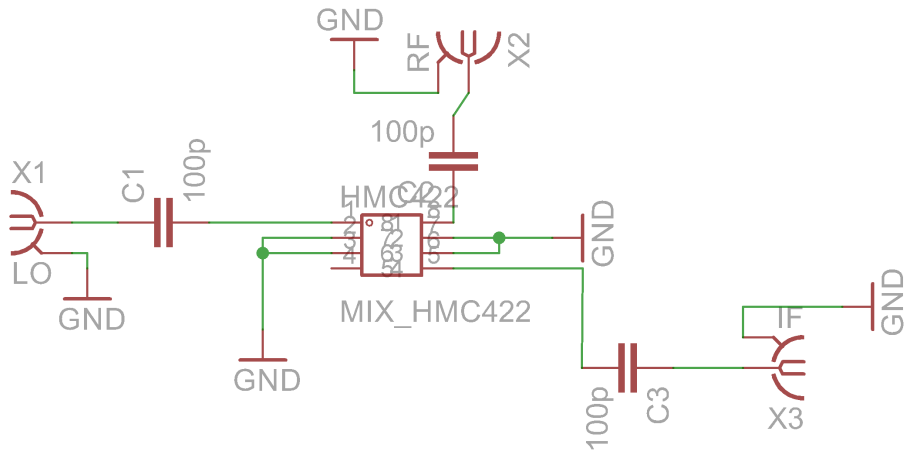
$$RF_{out2} = LO + RF_{in} = 7.0 \text{ GHz} \tag{3.11}$$

In the MIXER2 stage, two prototypes were necessary, which will be described in the following subsections. The manufacturer specifications for the HMC220 device are conversion loss of 7 dB and LO power of 13 dBm.

3.1.6.1 First prototype

The electrical schematic follows the same defined specifications for the MIXER1 stage in passive configuration. The final schematic is shown in Fig. 68. Fig. 69 shows the final layout designed using EAGLE software and the prototype for the MIXER2 stage.

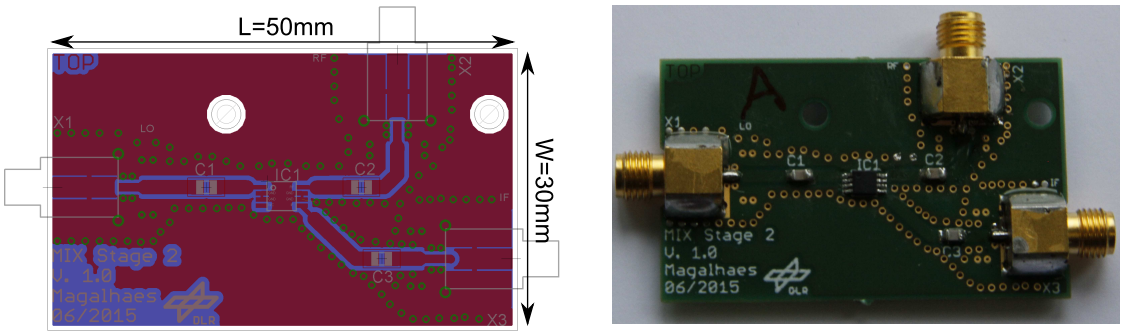
Figure 68 – Schematic designed for the MIXER2 stage.



Source: The author.

Figure 69 – Layout designed for the MIXER2 stage, first prototype.

(a) EAGLE layout. (b) Prototype.



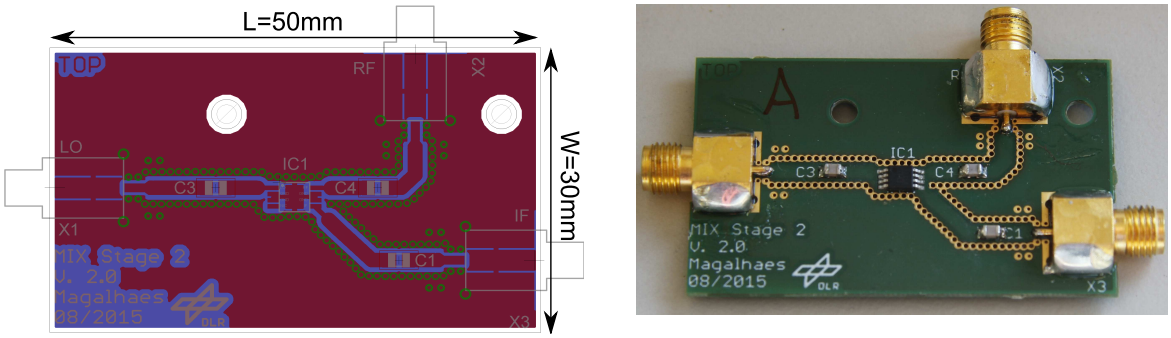
Source: The author.

3.1.6.2 Second prototype

Small adjustments in the design were necessary: the quantity and proximity or positions of the holes were changed. The new layout of the MIXER2 stage can be seen in Fig. 70, along with a photo of the prototype.

Figure 70 – Layout designed for the MIXER2 stage, second prototype.

(a) EAGLE layout. (b) Prototype.

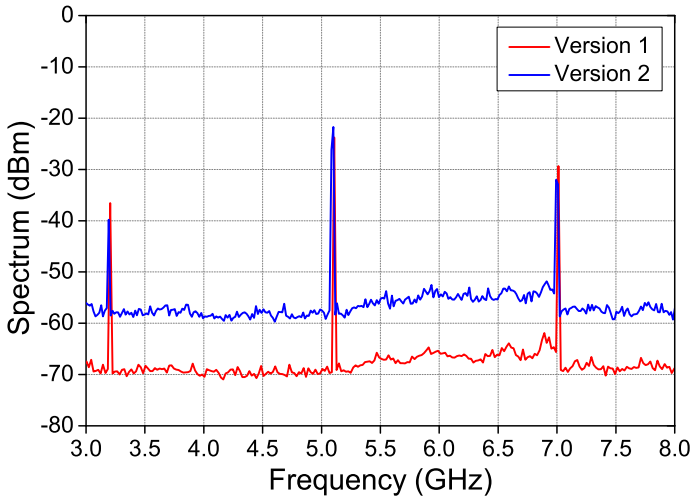


Source: The author.

3.1.6.3 Measurement results

The measurements were performed and are shown in Fig. 71. The results are presented in the form of spectrum as a function of the frequency. As it can be observed, both prototypes presented almost the same performance with good reproducibility in terms of device specifications. The noise level in the graph seems to be different because of the number of points used to measure the different PCBs. As the mixer is passive, the LO level is larger than the output signals, but still meeting the specifications in terms of noise figure, conversion loss and frequency translation.

Figure 71 – Measurement results for the MIXER2 stage.



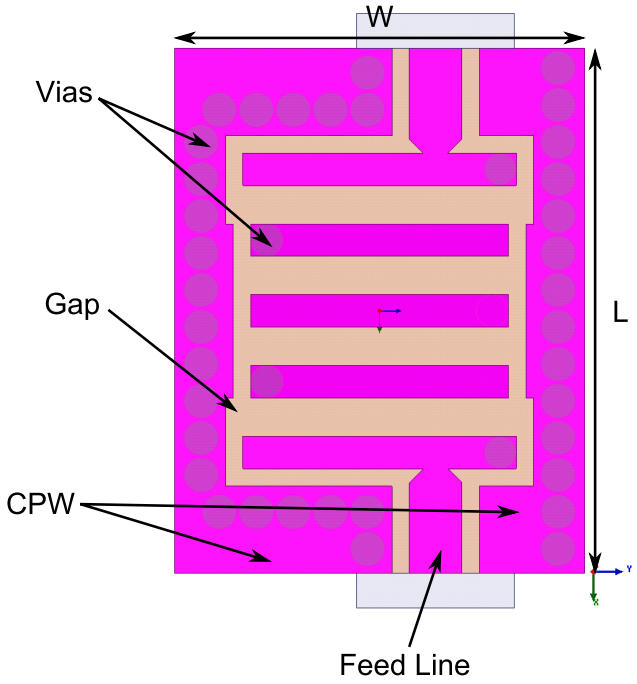
Source: The author.

As expected, there are two signals generated by the combination of the $LO = 5.1$ GHz and the $IF = 1.9$ MHz. The sum resulted in the desired frequency (7.0 GHz) and the difference resulting in 3.2 GHz, which can be cutoff employing a band-pass filter.

3.1.7 Band-pass filter operating at 7.0 GHz

The second filtering stage is composed of a band pass filter (BPF). The design can be performed in several ways, such as: merging a low-pass (LPF) with a high-pass filter (HPF), and then converting the electrical circuit into an equivalent circuit with lumped components; or using an alternative approach with a Butterworth distributed filter also called as an interdigital distribuited band-pass filter. An interdigital filter can be converted from the lumped model directly without knowledge of the electrical circuit with better performance in terms of attenuation, gain and narrowband behaviour compared to the usual case (merging LPF and HPF). For the BPF design, a coplanar waveguide structure was adopted, due to the same advantages described in Section 3.1.3. Fig. 72 shows the defined model.

Figure 72 – Adopted structure for the band-pass filter design.



Source: The author.

An interdigital distributed BPF is formed basically by successive short-circuit stubs connected to the ground by vias and interdigitally connected between the lines. As the filter order increases, the attenuation increases. According to the litarature, a stub is a shunt section of transmission line that is terminated in a short or an open circuit (SAYRE, 2001). This concept is exactly equivalent to lumped series resonant circuits. When a low-impedance load is placed, such as a short, at the end of a 90° long stub, the impedance at the input of a shorted stub will have a very high impedance over a narrow band of frequencies, which can be considered as an open circuit. This is equivalent to a lumped parallel resonant circuit and for every 90° added to this stub (SAYRE, 2001).

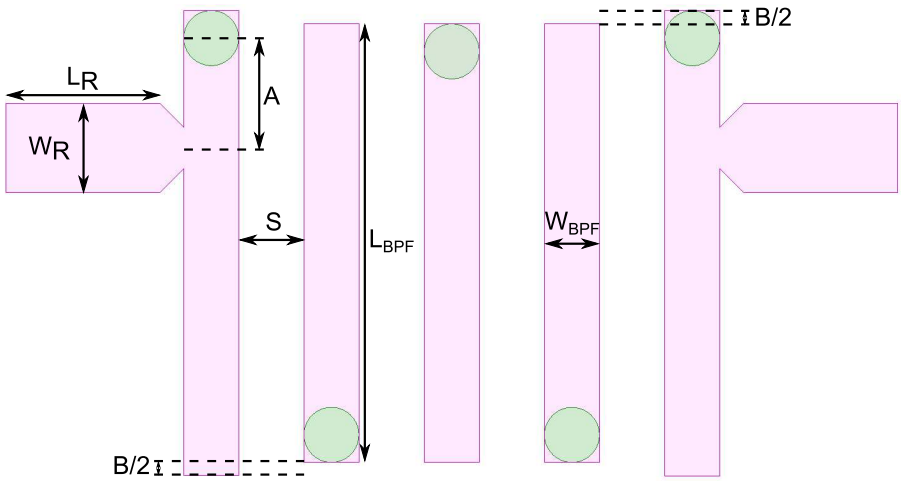
The BPF will operate at a frequency of 7.0 GHz, due to the necessity to cutoff the undesired frequency generated by the MIXER2 stage. The transmission will occur at 7.0 GHz and the defined bandwidth for the proper operation was 100 MHz.

3.1.7.1 Calculation of the initial parameters

Parameters such as operation frequency for the Tx-circuitry of $f = 7.0$ GHz, bandwidth of $BW = 100$ MHz, and input and output impedance of $R_0 = 50\ \Omega$, and characteristic impedance for the feed lines of $Z_0 = 60\ \Omega$ were defined. The FR4 material has dielectric constant of $\varepsilon_r = 4.4$, loss tangent of $\delta = 0.02$ and thickness of $h = 1.6$ mm.

Firstly a third order filter was designed, but due to the low out-of-band attenuation, a higher order filter was necessary. So, a fifth order interdigital distribuited band-pass filter was chosen in order to improve the performance. The dimensions of the filter are shown in Fig. 73: width (W_{stub}) and length (L_{stub}) of the feed lines, the spacing or gap (S) between the adjacent stubs, the length (B) of the first lines regarding to the adjacent lines, the length (A) to the center of the input, and the width W_R of the input/output 50 Ω transmission lines.

Figure 73 – Interdigital distributed BPF model.



Source: The author.

To calculate A, B and S, it is necessary to calculate the stubs width and length. The stub width can be calculated isolating W_{stub} in the following equation (SAYRE, 2001)

$$Z_0 = \frac{377}{(\frac{W_{stub}}{h} + 1)\sqrt{\varepsilon_r + \sqrt{\varepsilon_r}}} \tag{3.12}$$

With the calculated stub width, it is possible to define the effective dielectric constant (ε_r), the propagation velocity V_p, the guided wavelength λ and the length of the

feed line L_{stub} through the following equations (BALANIS, 2012)

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + (\frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + (\frac{12h}{W_{stub}})}}) \tag{3.13}$$

$$V_p = \frac{1}{\sqrt{\varepsilon_{reff}}} \tag{3.14}$$

$$\lambda = \frac{c}{f_c} \tag{3.15}$$

$$L_{stub} = V_p \frac{\lambda}{4} \tag{3.16}$$

Considering the use of the Txline software to determine the parameters as stub width and length, $W_{stub} = 1.365$ mm and $L_{stub} = 5.897$ mm were obtained. After estimating the width and length, it is possible to obtain the parameters $BW_{3\text{dB}}$, A, B and S. The parameters $BW_{3\text{dB}}$ and A can be calculated using the following equations (SAYRE, 2001).

$$BW_{3dB} = \frac{f_u - f_l}{f_c} 100\ \% = 6.114\ \% \tag{3.17}$$

$$A = CF[L_{stub} - (\frac{f_l}{f_u} L_{stub})] = 0.332\ \text{mm} \tag{3.18}$$

Where $BW_{3\text{dB}}$ is the percentage of the bandwidth at the 3 dB points, $f_u = 7.15$ GHz is the frequency of the upper 3 dB point, $f_l = 6.95$ GHz is the frequency of the lower 3 dB point, and CF is the correction factor. If the calculated $BW_{3\text{dB}}$ is above 30%, then $CF = 1.30$; for 20%, $CF = 1.35$; for 10%, $CF = 1.70$; and for 5%, $CF = 2.0$.

With A, it is possible to obtain the parameters B and S according to the following equations (SAYRE, 2001)

$$B = A \cdot CF_B = 0.00332\ \text{mm} \tag{3.19}$$

$$S = A \cdot CF_S = 0.4648\ \text{mm} \tag{3.20}$$

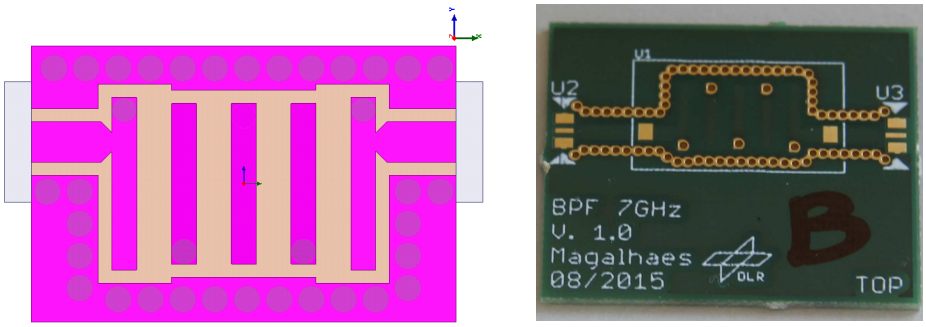
Where CF_B is the correction factor required for various different 3 dB filter bandwidth percentages ($BW_{3\text{dB}}$): for 30%, $CF = 0.20$; for 20%, $CF = 0.14$; for 10%, $CF = 0.05$; and for 5%, $CF = 0.01$. For the parameter S: CF is the correction factor for various bandwidth percentages ($BW_{3\text{dB}}$): for 30%, $CF = 0.09$; for 20%, $CF = 0.2$; for 10%, $CF = 0.55$; and for 5%, $CF = 1.4$.

3.1.7.2 Simulation of BPF using HFSS software

After calculating the initial dimensions, the BPF can be optimized using HFSS software. Fig. 74 presents the designed structure in the software and the prototype.

Figure 74 – Designed BPF operating at 7.0 GHz.

(a) HFSS layout. (b) Prototype.

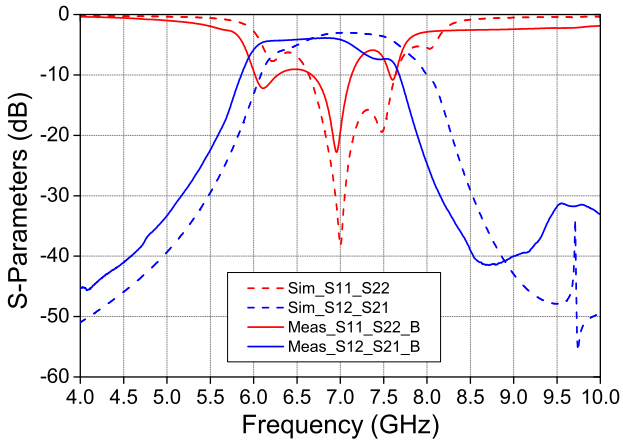


Source: The author.

3.1.7.3 Measurement and simulation results

Some optimizations were needed to obtain a better performance in terms of reflection and transmission coefficients (S-parameters). For comparison, the simulated and measured S-parameters are plotted in Fig. 75. The measurement and simulation results are similar, with a small displacement in frequency. This effect can occur due to the dielectric constant variation of the substrate used and also due to small errors in the prototype dimensions. The reproducibility was checked and the expected insertion loss and out-of-band attenuation were obtained. The final dimensions for this filter are shown in Table 9. The total length (L) is equal to 15.8 mm.

Figure 75 – Obtained S-parameters for the BPF operating at 7 GHz.



Source: The author.

Table 9 – Final dimensions for the BPF designed in CPW technology at 7.0 GHz.

Parameter	Dimension (mm)
L	15.8
W	10.3
L_{stub}	5.5
W_{stub}	0.9
S	1.3
A	1.2
B	0.4
$W_{R1,2}$	1.5
$L_{R1,2}$	3.0

Source: The author.

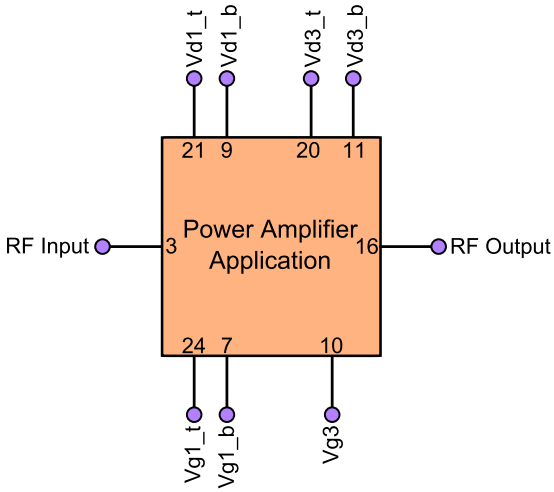
3.1.8 Medium power amplifier - second stage

The tests for the second stage of amplification (MPA2) consisted in two prototypes. In the first, a power amplifier (PA) was designed. However, the obtained results were not as expected. In the second prototype, two kinds of medium power amplifiers were designed and measured in order to provide the required amplification for the system. Since a very high power level was not necessary, the MPAs became feasible for the project replacing the use of power amplifiers.

3.1.8.1 Design of the power amplifier

The power amplifier (PA) TGA2706 should amplify the signal at 7.0 GHz, in order to reach the desired output power. Fig. 76 shows the recommended application circuit for the power amplifier.

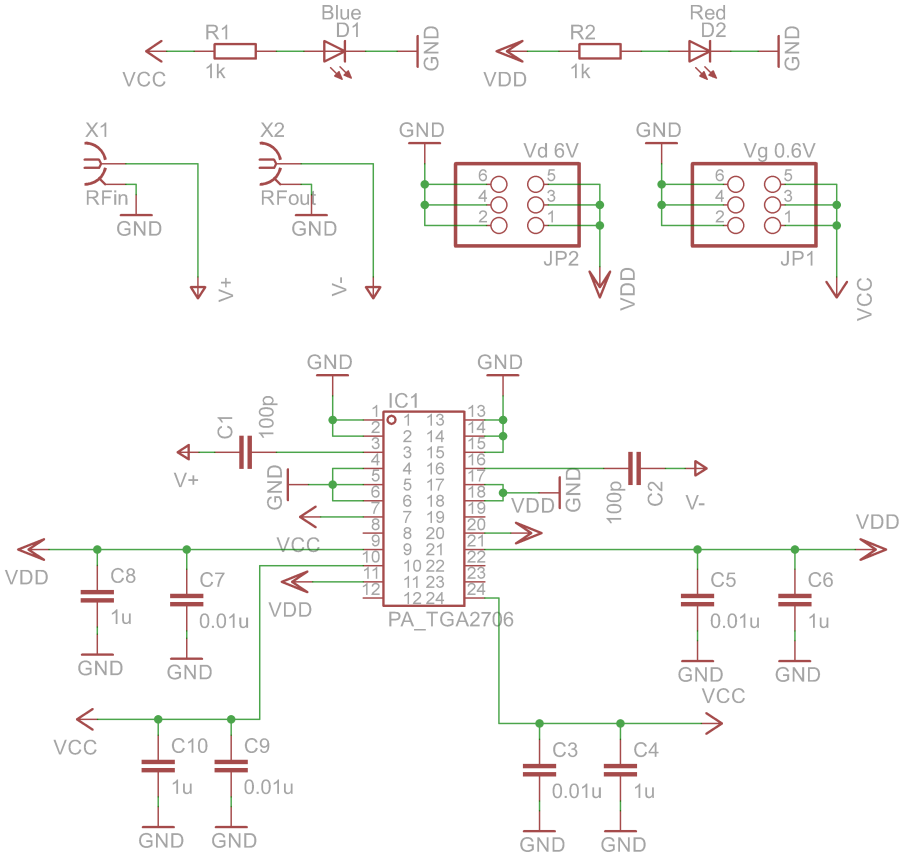
Figure 76 – Recommended application circuit for the power amplifier.



Source: The author.

The connection to RF_{in} requires the use of an external DC blocking capacitor dependent on the frequency of operation. The required DC voltages are 6 V and 0.6 V and capacitors for bypass were used. Fig. 77 shows the final designed schematic. The power amplifier layout was designed with the initial connections provided by the schematic. Fig. 78 shows the designed layout and the prototype for such device.

Figure 77 – Schematic designed for the power amplifier.

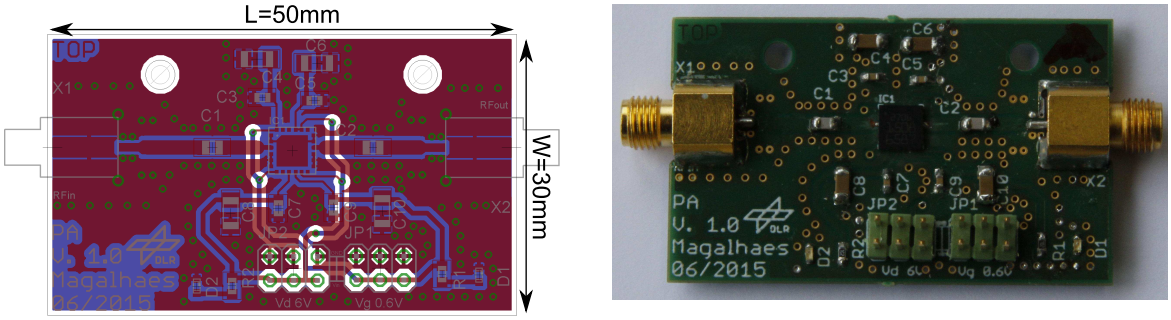


Source: The author.

Figure 78 – Layout designed for the power amplifier.

(a) EAGLE layout.

(b) Prototype.

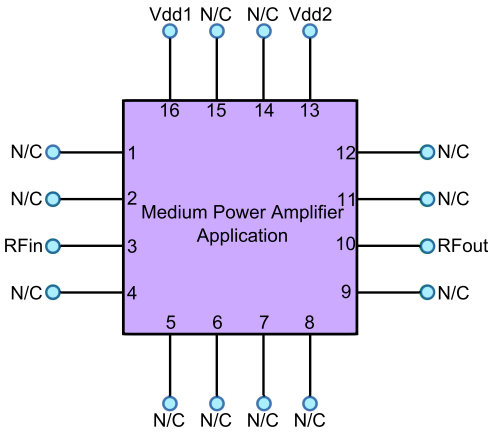


Source: The author.

3.1.8.2 Design of the MPA2 stage

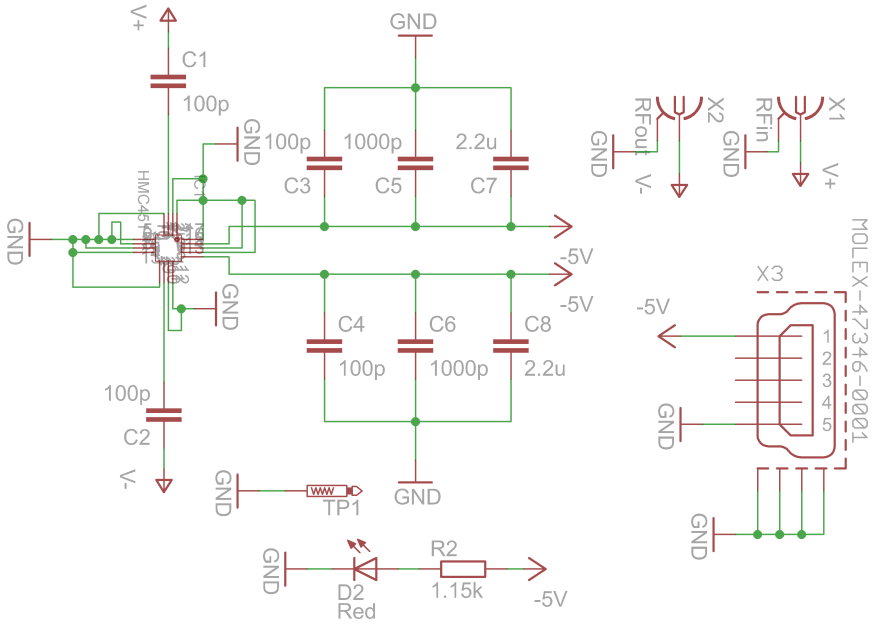
As the designed power amplifier at the first iteration did not work properly, the second iteration consisted on the design of a medium power amplifier. Two MPAs from different manufacturers were tested. Considering the same frequency of operation, the MPAs must amplify the signal at 7.0 GHz. Firstly, the model 1 from Hittite (HMC451LP3) will be described. Fig. 79 shows the recommended application circuit for the model 1 of MPA2 and Fig. 80 shows the final schematic. Fig. 81 shows the designed layout and the prototype.

Figure 79 – Recommended application circuit for the MPA2 from Hittite.



Source: The author

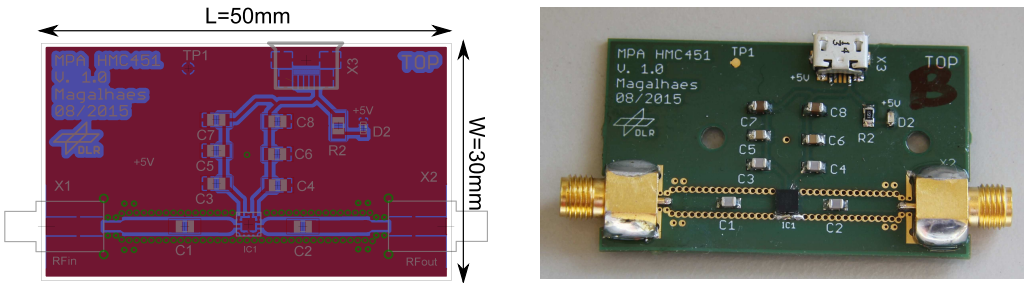
Figure 80 – Schematic designed for the second stage of medium power amplifier from Hittite, second production.



Source: The author.

Figure 81 – Layout designed for the second stage of medium power amplifier model 1.

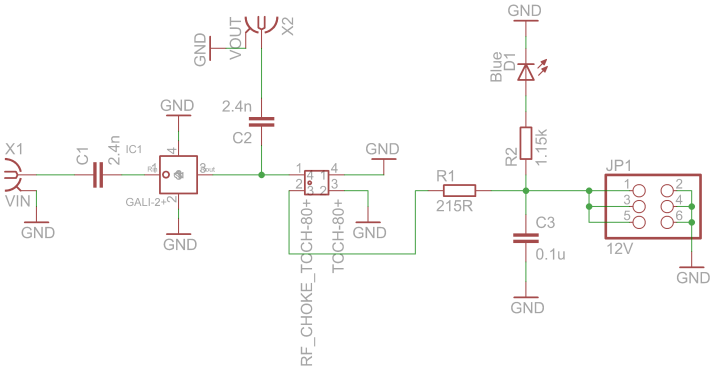
(a) EAGLE layout. (b) Prototype.



Source: The author.

The second model of medium power amplifier chosen is produced by Mini-Circuits (GALI-2+). This amplifier is intersting due the broadband operation: from DC to 8 GHz; hence becoming useful for all the Tx-stages. The manufacturer recommendation is the same used in the first stage of medium power amplifier. The schematic is shown in Fig. 82. Fig. 83 shows the designed layout and the prototype.

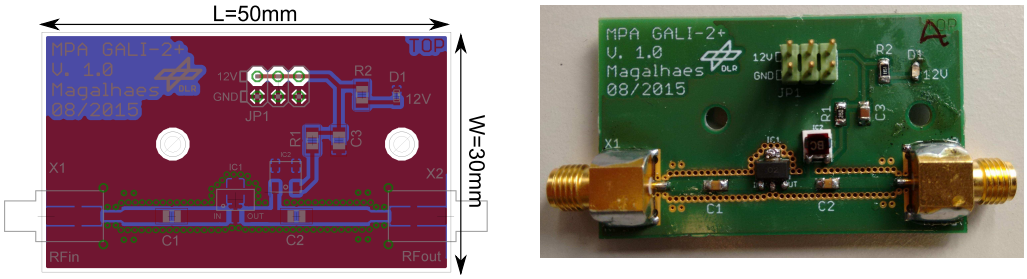
Figure 82 – Schematic designed for the second stage of medium power amplifier from Mini-circuits.



Source: Prepared by the author

Figure 83 – Layout designed for the second stage of medium power amplifier model 2.

(a) EAGLE layout. (b) Prototype.

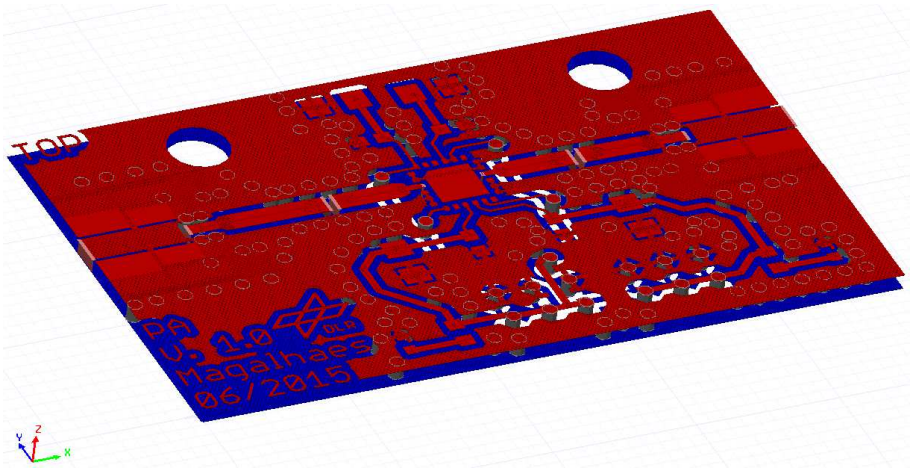


Source: The author.

3.1.8.3 Measurement and simulation results

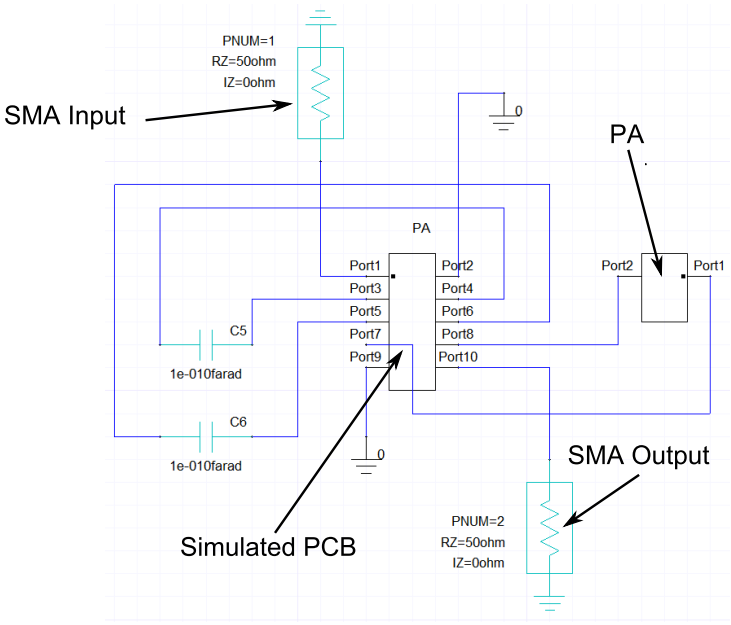
As most of the amplifiers has only one input and one output, the PCB simulation was possible with a touchstone file provided by the manufacturer. The simulation model in HFSS for the power amplifier is shown in Fig 84. Then, performing the standard simulation steps used in previous simulations, the designed circuit is shown in Fig. 85. Simulation results are shown in Fig. 86. The S-parameters present good performance based on the device specifications in terms of reflection and transmission coefficients. The obtained maximum gain at 7.0 GHz was 25 dB.

Figure 84 – Designed PCB for the power amplifier.



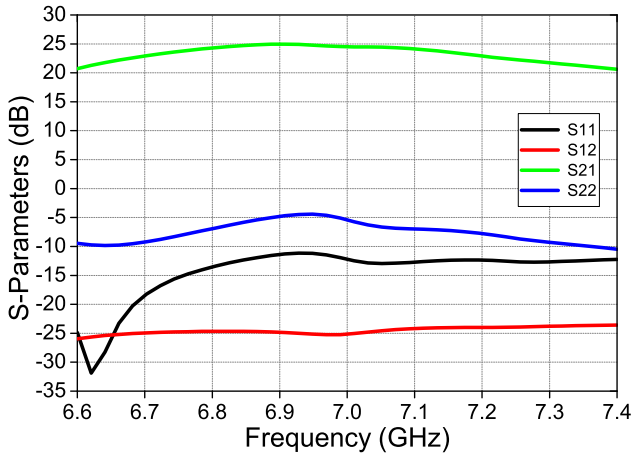
Source: The author.

Figure 85 – Designed circuit for the power amplifier.



Source: The author.

Figure 86 – Simulated S-parameters for the power amplifier.



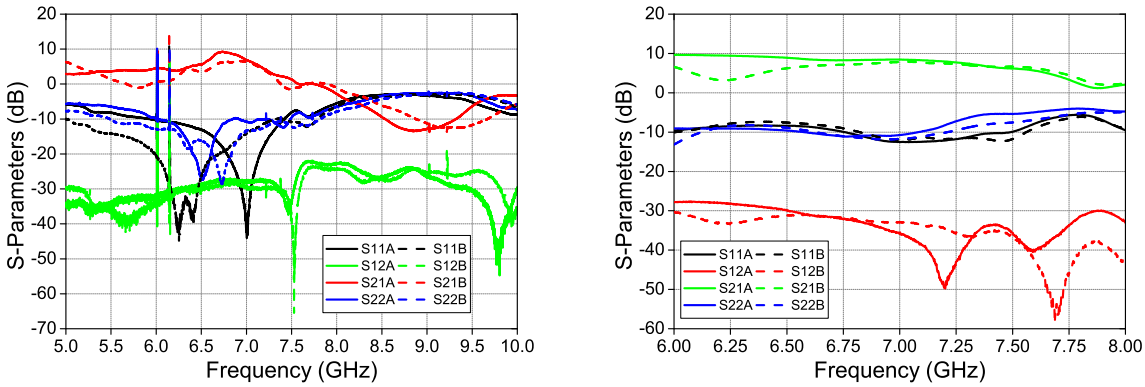
Source: The author.

As commented before, the power amplifier simulation was good for the expected performance from the datasheet. However the measurement behaviour of such device was not as expected.

The measured S-parameters for both models of medium power amplifier are shown in Fig 87. The medium power amplifier GALI-2+ presented better performance than the Hittite device in terms of gain and return loss.

Figure 87 – Measured S-parameters for the second stage of medium power amplifiers.

(a) Model 1 - HMC451. (b) Model 2 - GALI-2+.

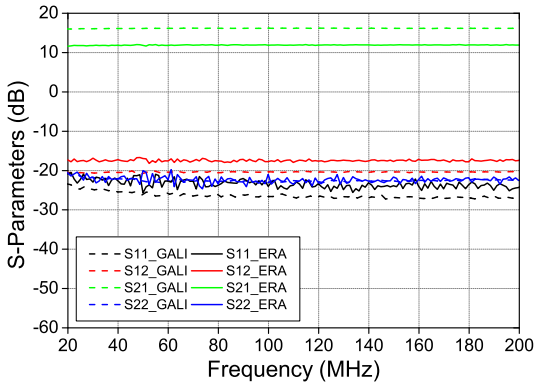


Source: The author.

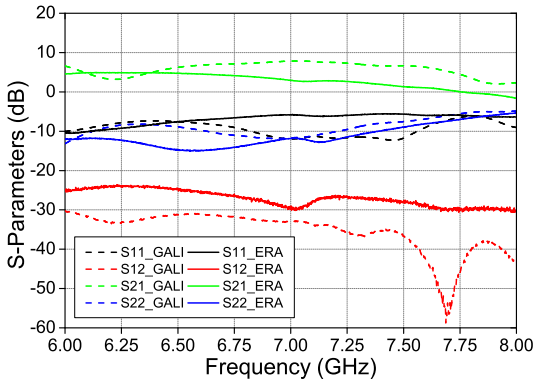
The two stages of MPAs from Mini-circuits worked fine and both are broadband devices operating in both IF or RF frequencies. To compare both models, Fig. 88 shows the measured results in the two frequency ranges in which the MPAs should be employed (100 MHz and 7.0 GHz). The MPA GALI-2+ presented better performance in both frequency ranges, resulting in maximum gain of 16 dB at 100 MHz and of 9 dB at 7.0 GHz, whilst the ERA-1SM+ presented gain of 12 dB at 100 MHz and of 4 dB at 7.0 GHz.

Figure 88 – Comparison between the medium power amplifiers from Mini-circuits.

(a) Comparison at 100 MHz.



(b) Comparison at 7.0 GHz.

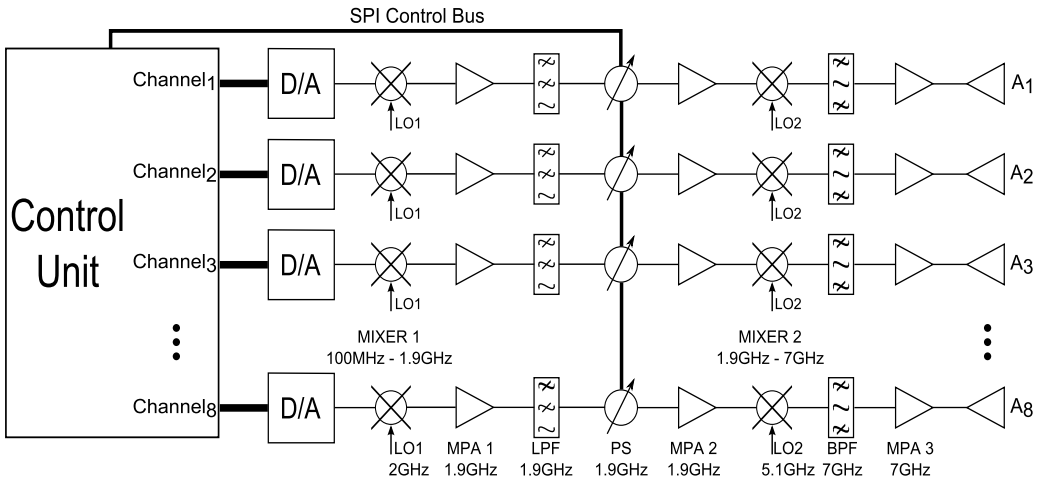


Source: The author.

3.2 Integration of the Individual Components

The design and validation of the individual components were carried out in order to make the RF analysis easier. Some changes regarding the initial architecture were made: the amplitude controlling with the variable gain amplifier has been removed. The reason for this change was commented previously due to the design restrictions at UNIPAMPA and costs. The main reasons were the high price of each component and the difficulty of soldering the VGA on the board. Thus, the amplitude should be now controlled by the FPGA directly. To replace the VGA gain, one more MPA stage has been included after the phase shifter. Also, the calibration system was removed because of the complexity to integrate the whole system. The calibration should be made in offline mode prior to the Tx-circuitry operation. The defined new architecture can be seen in Fig. 89.

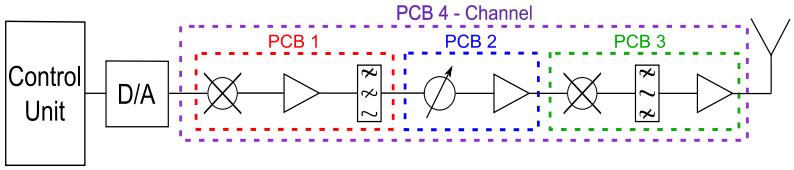
Figure 89 – New architecture for the Tx-circuitry without VGA.



Source: The author.

The second step consisted on merging some of the components prior to design of an entire channel. For that, three PCBs were designed separately as shown in Fig. 90. The first PCB is composed of the first mixing stage, an amplifier and the low-pass filter. The second one is based on phase shifter and amplifier. And finally, the third one is composed of the second mixing stage, the band-pass filter and another amplifier. The PCBs are shown in Fig. 91.

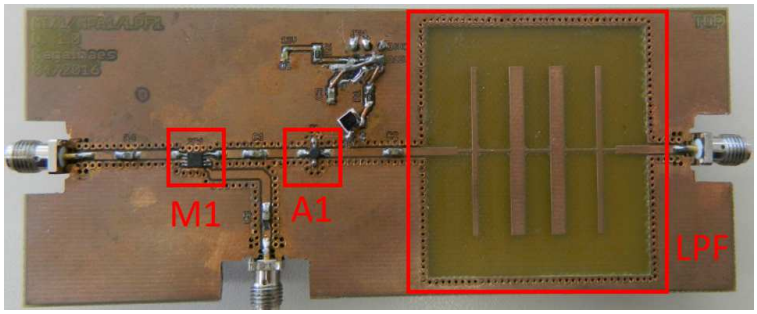
Figure 90 – Design boards for integration of the Tx-channel.



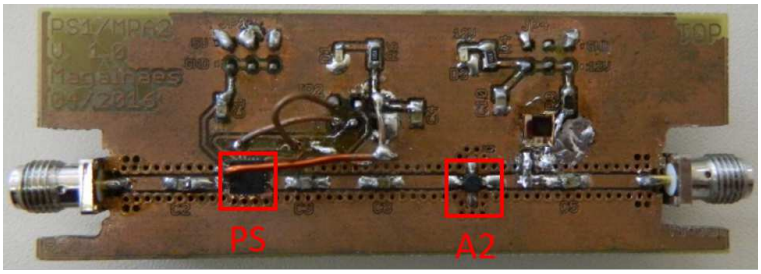
Source: The author.

Figure 91 – Assembled PCBs for the Tx-circuitry.

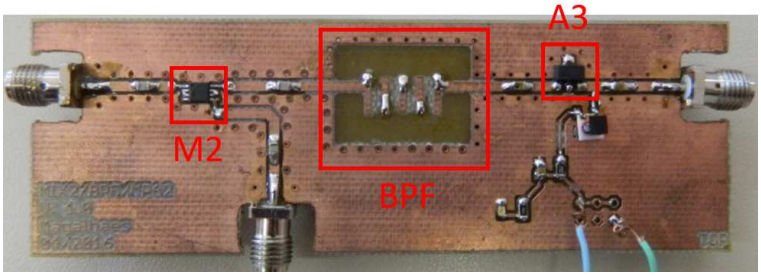
(a) PCB 1.



(b) PCB 2.



(c) PCB 3.



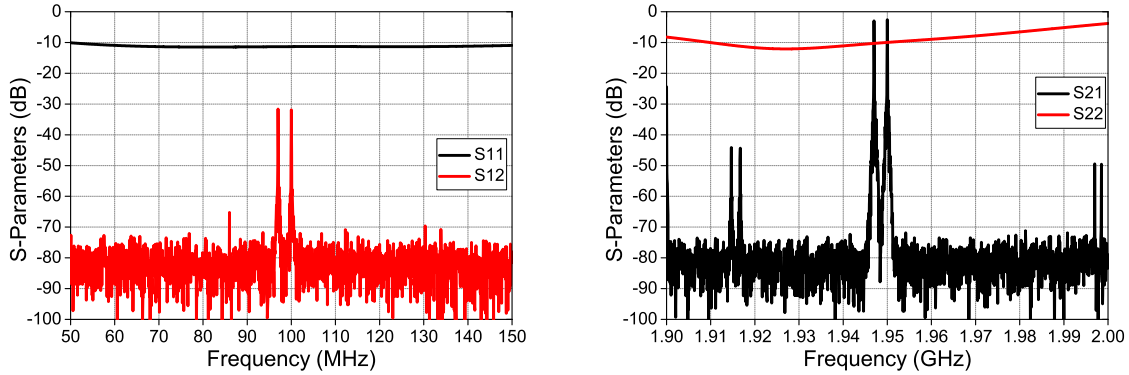
Source: The author.

The measurements were carried out with a network analyzer and a spectrum analyzer. The obtained results for each PCB are shown in Figs. 92 and 93. For PCB1, as there is a mixer stage, there are two ways to obtain the results. Using the network analyzer or spectrum analyzer. In this case, both measurements have been carried out. Fig. 92 shows that best performance of filtering comes when the LO is set at 2.05 GHz. Therefore, for the final operation of the Tx-channel, the LO frequency should be displaced to this value. Also, the expected gain was achieved, considering an input power of −20 dBm. The S-parameters show the same results in another way, the reflection coefficient is lower than −10 dB and the gain was the expected (approximately 0 dB).

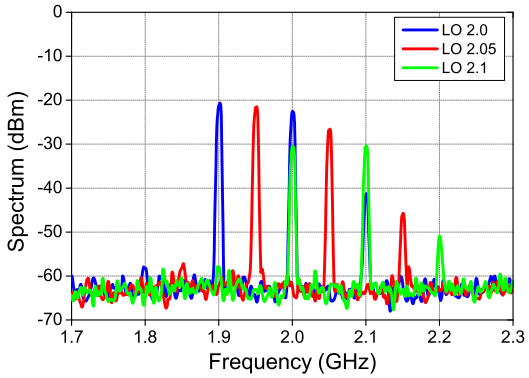
Figure 92 – Measured results for the PCB1.

(a) Measured S-parameters at 100 MHz.

(b) Measured S-parameters at 1.95 GHz.



(c) Measured spectrum.

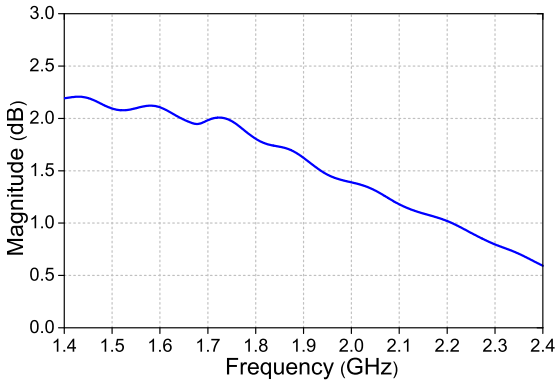


Source: The author.

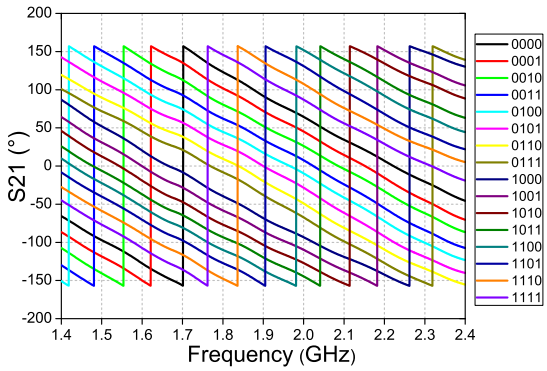
The second PCB was measured using only the network analyzer. For this PCB, it is intersting to observe the amplitude and phase. In Figs. 93a and 93b, the expected gain was achieved and the phase shift is working properly. The phase difference between adjacent curves is around 22.5 degrees. The obtained gain is around 2.0 dB. For the third PCB, the same evaluation made for the first one was carried out, because of the mixer stage. As shown in Figs. 93c and 93d, good results for the expected performance considering the components prototyped individually in terms of S-parameters were obtained.

Figure 93 – Measured results for the PCB2 and PCB3.

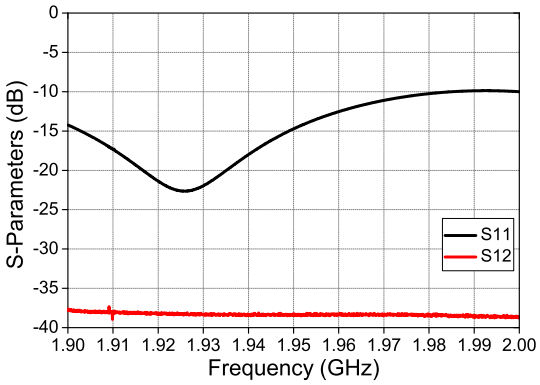
(a) Measured amplitude for the PCB2.



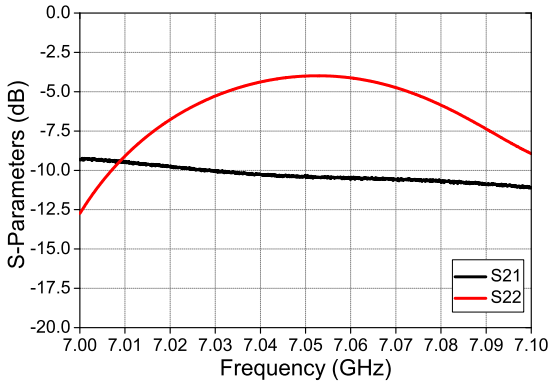
(b) Measured phase for the PCB2.



(c) Measured S-parameters at 1.95 GHz for the PCB3.



(d) Measured S-parameters at 7.0 GHz for the PCB3.

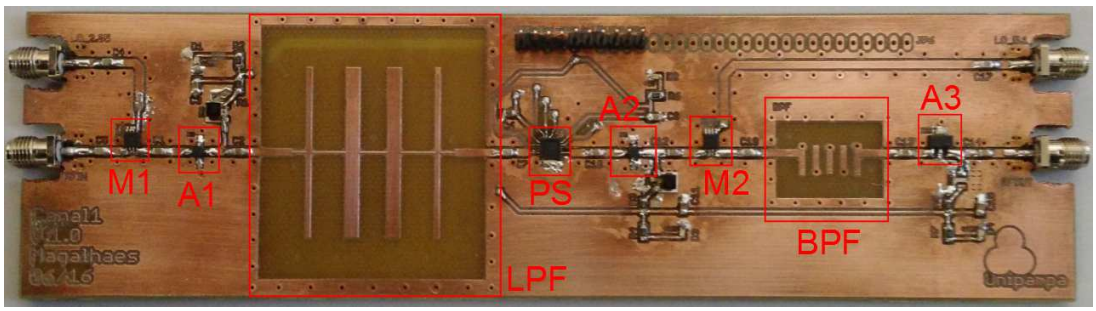


Source: The author.

3.3 Integration of the Complete Channel

The next step consisted in assembling a complete channel with the same architecture shown in Fig. 90. The channel was assembled at UNIPAMPA and can be seen in Fig. 94.

Figure 94 – Complete Tx-channel.

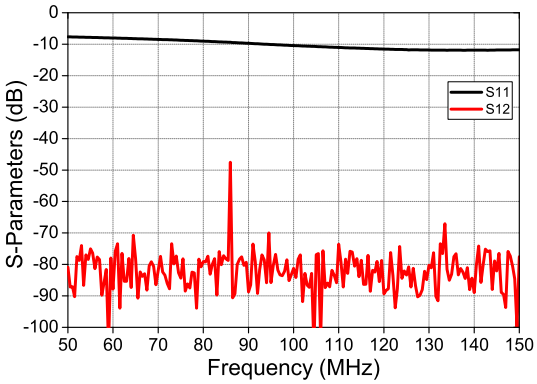


Source: The author.

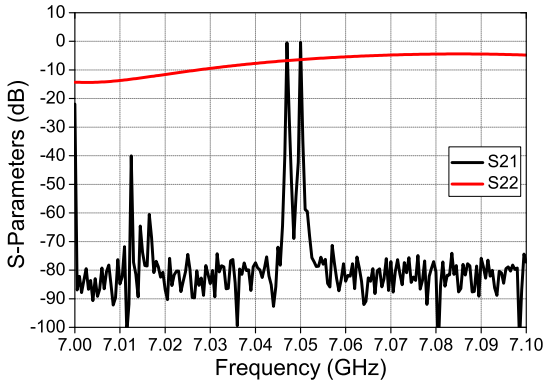
Fig. 95 shows the measured S-parameters. Good results were achieved. The measured gain is around 0 dB at 7.0 GHz and the reflection coefficient is slightly below −10 dB. The phase could not be measured with the equipment available at UNIPAMPA.

Figure 95 – Measured results for the complete channel.

(a) Measured S-parameters at 100 MHz.



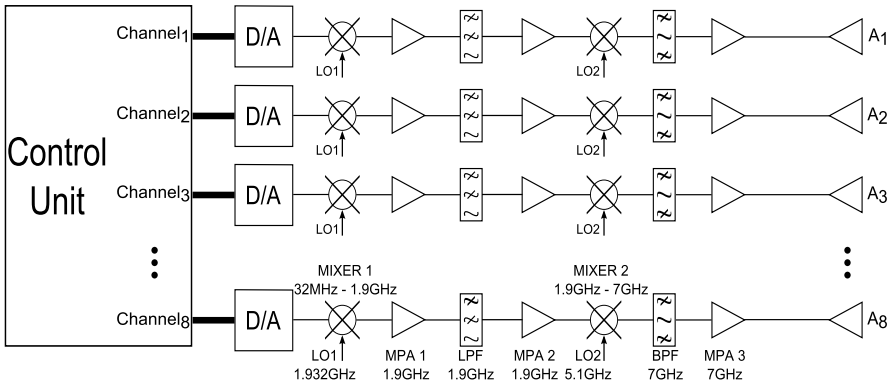
(b) Measured S-parameters at 7.0 GHz.



Source: The author.

Since the measurement of phase for the complete channel was not possible and soldering of the phase shifters was not easy to be done, some changes in the architecture were necessary. The phase shifter was removed and the phase should be controlled also by the control unit. For that, the final architecture is shown in Fig. 96. Also, the input frequency was changed, since the FPGA can only work at 32 MHz to perform the phase shifting properly. The LO frequency for the MIXER1 stage has been also redefined to result in $IF = 1.9$ GHz. One additional MPA stage has been included. In comparison to the previous version, as expected the gain of the channel without the phase shifter increased. The new channel was measured in terms of S-parameters and the results are shown in Fig. 97. As it can be observed, good results based on the expected gain for each component were obtained in terms of amplitude. The gain was increased around 10 dB.

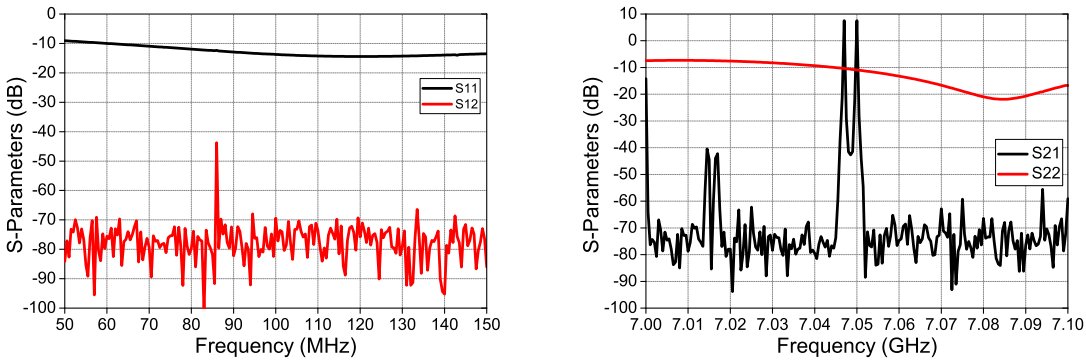
Figure 96 – Final architecture without phase shifters.



Source: The author.

Figure 97 – Measured S-parameters for the complete channel without phase shifter.

(a) 100 MHz. (b) 7.0 GHz.



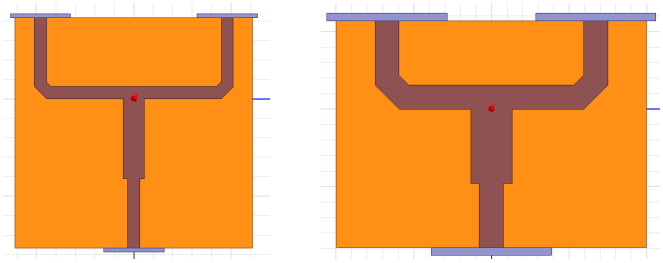
Source: The author.

3.4 Integration of the Eight Channels

In order to feed the antenna array designed in Chapter 2, the final goal is to design 8 Tx-channels. Due to the limitations of the prototyping machine, this has been achieved by designing two boards, each with four channels. For the previous measurements, the mixer operates using an external LO signal directly from the signal generator. For the final boards, the design of power dividers (PD) was necessary. Thus, the PD can be allocated under the channels at the bottom layer and can be connected through vias to the top layer. The PDs were designed with one input and two outputs that should deliver the same output power. The designed PDs operating at 1.932 GHz and 5.1 GHz are shown in Fig. 98. The substrate used is the same FR4 board as employed to the Tx-channels.

Figure 98 – Electromagnetic models of the power dividers for both LO frequencies.

(a) 1.9 GHz. (b) 5.1 GHz.

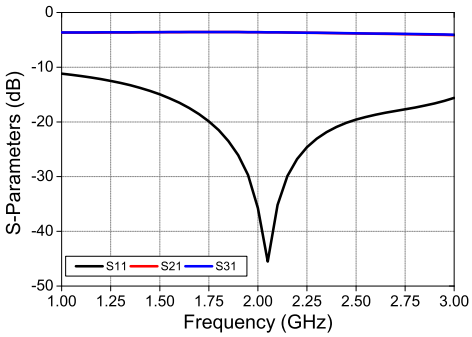


Source: The author.

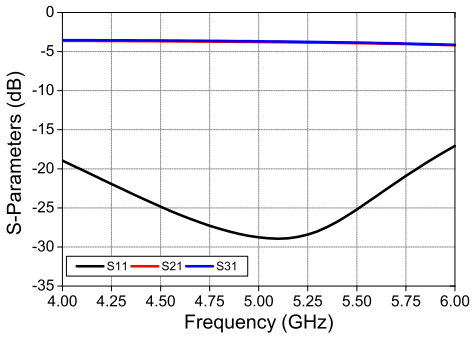
After some simulations, good results for the expected 1:1 power delivered in the outputs have been achieved. The simulation and measurement results can be seen in Fig. 99. Good agreement between simulations and measurements were observed, with a small displacement in frequency, which is expected due to the prototyping accuracy. The 1x4 PD was designed and is shown in Fig. 100.

Figure 99 – Results for the designed power dividers in both frequencies.

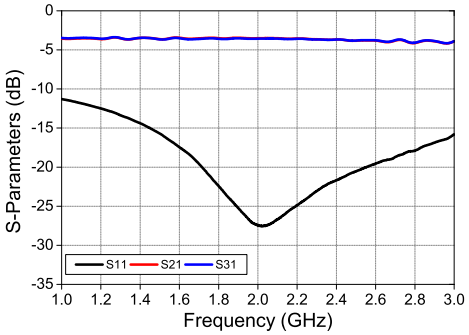
(a) Simulation at 1.932 GHz.



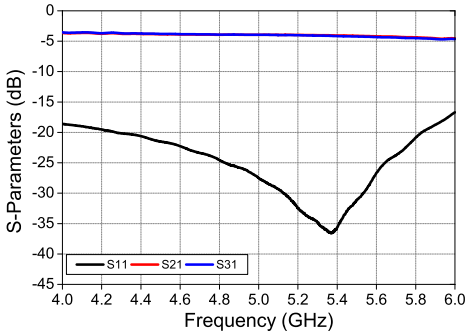
(b) Simulation at 5.1 GHz.



(c) Measurement at 1.932 GHz.

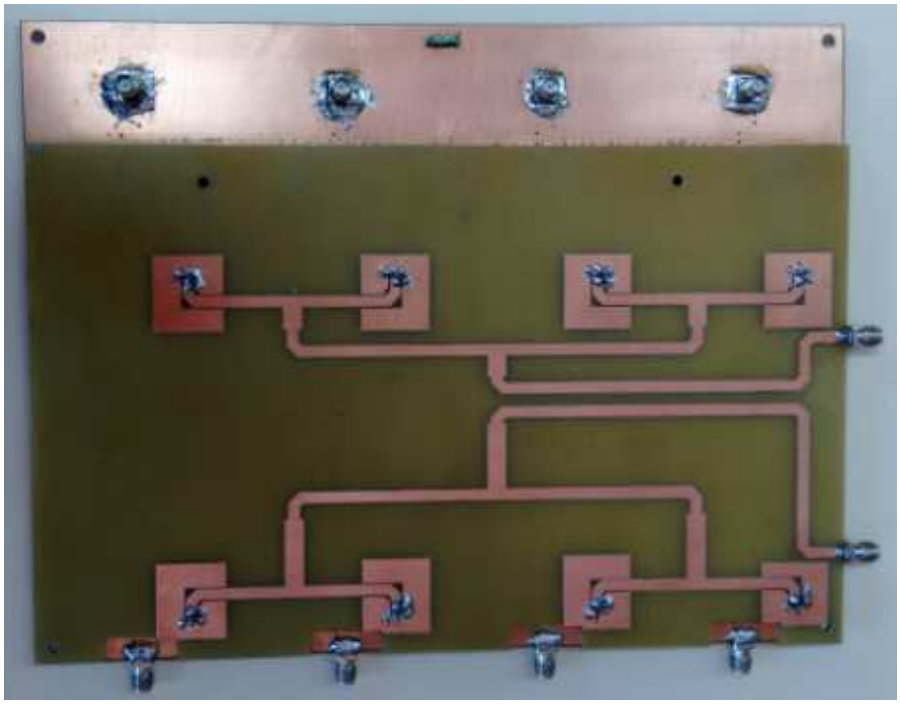


(d) Measurement at 5.1 GHz.



Source: The author.

Figure 100 – Prototyped 1x4 power divider.

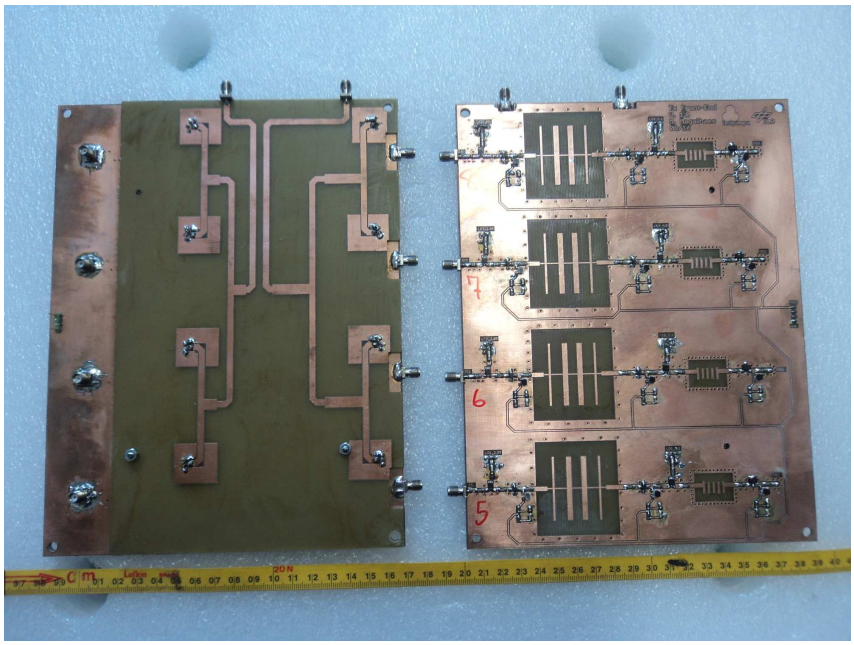


Source: The author.

The next step consisted in merging the 4 channels with the 1x4 power dividers in each board. In this case, two protoypes of 4 channels were built, in order to obtain the needed 8 channels. Fig. 101 shows the final protoype with the channels and the power dividers. For good connection, the two boards were separated from each other by 10 cm.

Figure 101 – Prototyped boards with power dividers.

(a) Top and bottom views.

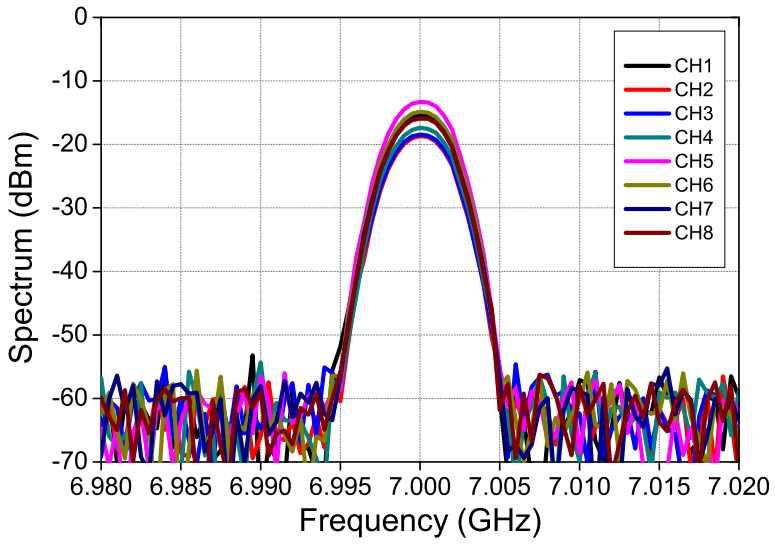


(b) Isometric view of the boards with the supporting structure.

Source: The author.

The final measured results for the eight channels are shown in Fig. 102. The differencies of power level between the channels are due to the tolerances of the fabrication process, especially in terms of soldering the components that operate at 7.0 GHz. By using an input power of −20 dBm, one can see from Fig. 102 that the boards did not perform with the expected gain of 8.0 dB. The main reason for that is the maximum LO power available from the signal generators. The phase shift introduced by each channel has been measured in a two-step approach in the laboratories of DLR. First, the phase shift between the channel input and the output of the low-pass-filter has been measured. Then, the phase shift between the MPA2 stage and the channel output was measured. By combining both measurements, the total phase shift was estimated. For the purpose of calibration, the amplitude and phase unbalances need to be taken in account. The measured values for each channel are listed in Table 10.

Figure 102 – Measured spectrum for the 1x8 channels.



Source: The author.

Table 10 – Measured values for each complete channel.

Channel	Gain (dB)	Phase-shift (degrees)
1	6.7292	−203.3
2	3.3253	−24.4
3	3.5275	−19.4
4	4.6325	−23.6
5	8.6888	−179.4
6	7.1597	−169.9
7	6.1558	−213.1
8	6.0551	−254.2

Source: The author.

4 PCB Simulations

The simulations of Printed Circuit Boards (PCBs) are very important to analyze the boards performance before the production. By doing so, if there are some adjustments to be performed, they can be done without the knowledge of the real measurements. These simulations can be helpful in order to reduce the costs and time (MAGALHÃES et al., 2016).

The simulation process consists basically on three steps. Firstly, the PCB layout design (EAGLE) is done, then the evaluation of the PCB simulation (Ansys HFSS) analyzing the PCB behaviour without components is carried out, and, after that, an analysis using the circuit design is performed. To develop the last step, a co-simulation between the simulated PCB and the components is used (Ansys Designer).

Therefore, in this chapter, a tutorial explaining how to convert and simulate PCBs from a design tool (EAGLE) to an eletromagnetic simulation software is described. Then, the simulation of two cascaded LNAs is presented. The stages of mixer, phase shifter and variable gain amplifier are not possible to simulate due to the provided touchstone files by the manufacturer, which consider just one input and one output (.s2p). This means that the S-parameters are not the same as the measured ones (MAGALHÃES et al., 2016).

4.1 Procedure for Accurate Simulation of PCBs Working at High Frequencies

The PCB simulations using HFSS and Designer packages (both from ANSYS) can be used in order to improve the process and optimize the PCB designs. The simulation of a PCB from the gerber files can be performed through the following steps:

- Importing the DXF file
- Verification of the most relevant layers
- Setting up PCB stackup
- Recreating the vias from the original PCB
- Setting up the ports and HFSS extents
- Setting up an HFSS setup
- Creating the Circuit Design

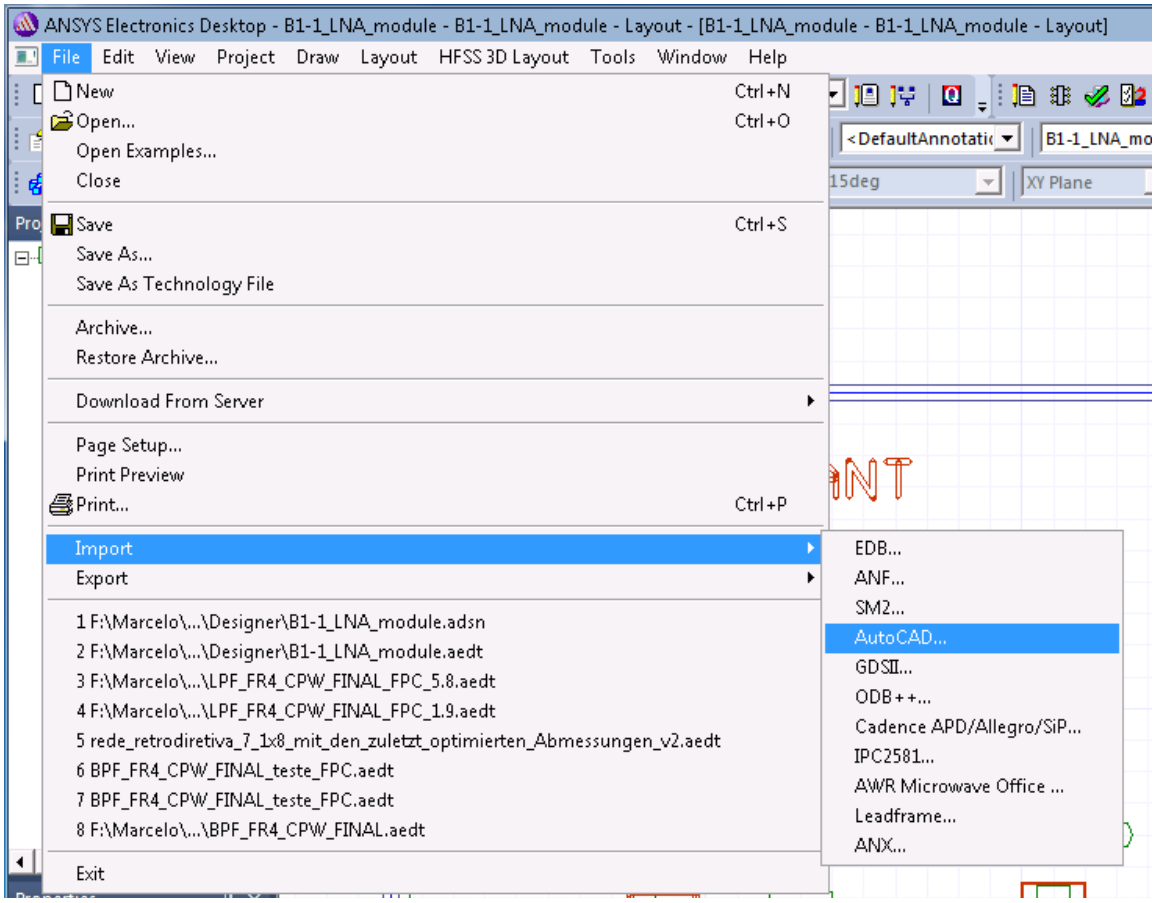
- Simulation of the electromagnetic model

In the following subsections, the step-by-step procedure to simulate the PCB design of two cascaded low-noise amplifiers (LNA) operating at 5.8 GHz will be presented.

4.1.1 Importing the DXF file

The first step consists in importing the DXF file including all the PCB layers. When the layout of a PCB has been done in EAGLE, the file must be saved in a DXF extension. Then, the DXF file can be imported into Ansys Designer going to File->Import->AutoCAD, as shown in Fig. 103.

Figure 103 – Importing DXF files.

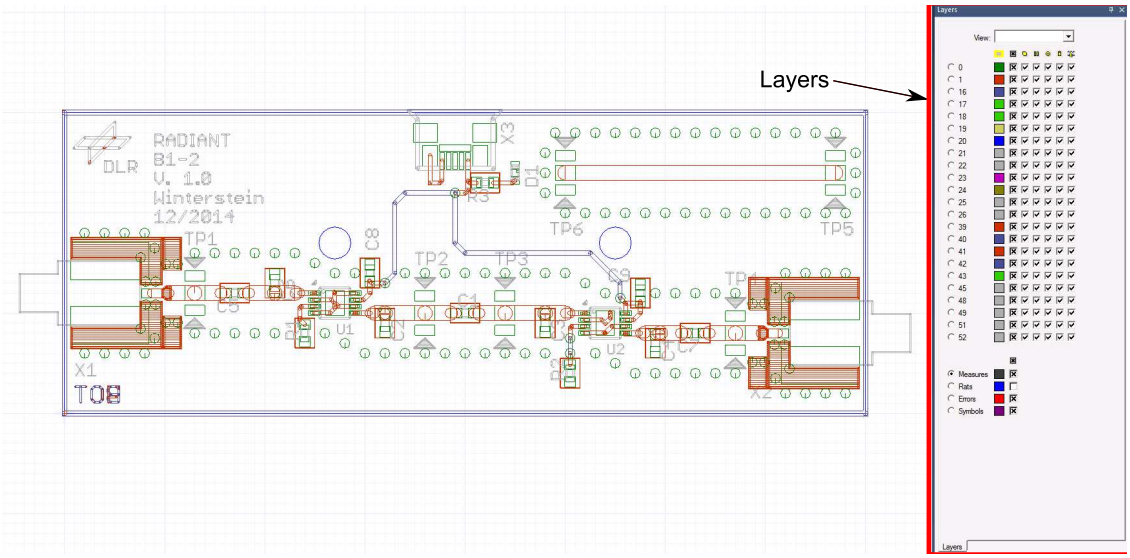


Source: The author.

4.1.2 Verification of the most relevant layers

The second step is based on the verification of which layers have relevant information about the desgined PCB and shall be used in the simulations. Fig. 104 shows the imported file with all LNA layers. In this case, the PCB has 23 layers, but only few layers are relevant for the electromagnetic simulation.

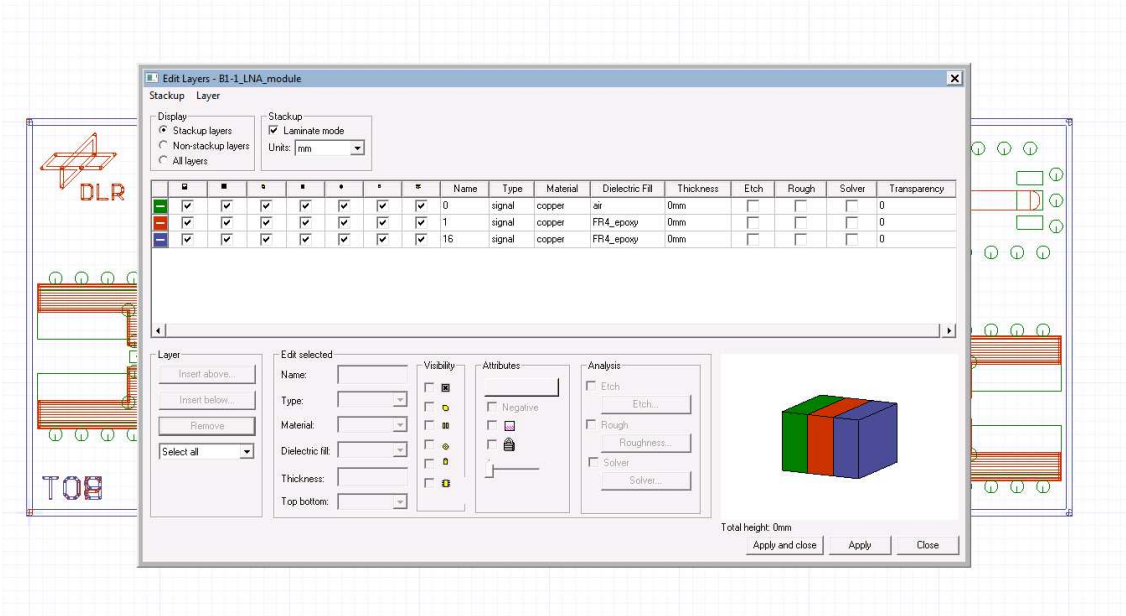
Figure 104 – Verification of the PCB layers.



Source: The author.

Then, just the layers that have relevant information (components, lines and vias) may be kept and the others can be deleted. In this case, top, bottom and vias (temporary) layers are relevant and were kept. Fig. 105 presents the final stack-up.

Figure 105 – Selection of the relevant layers.



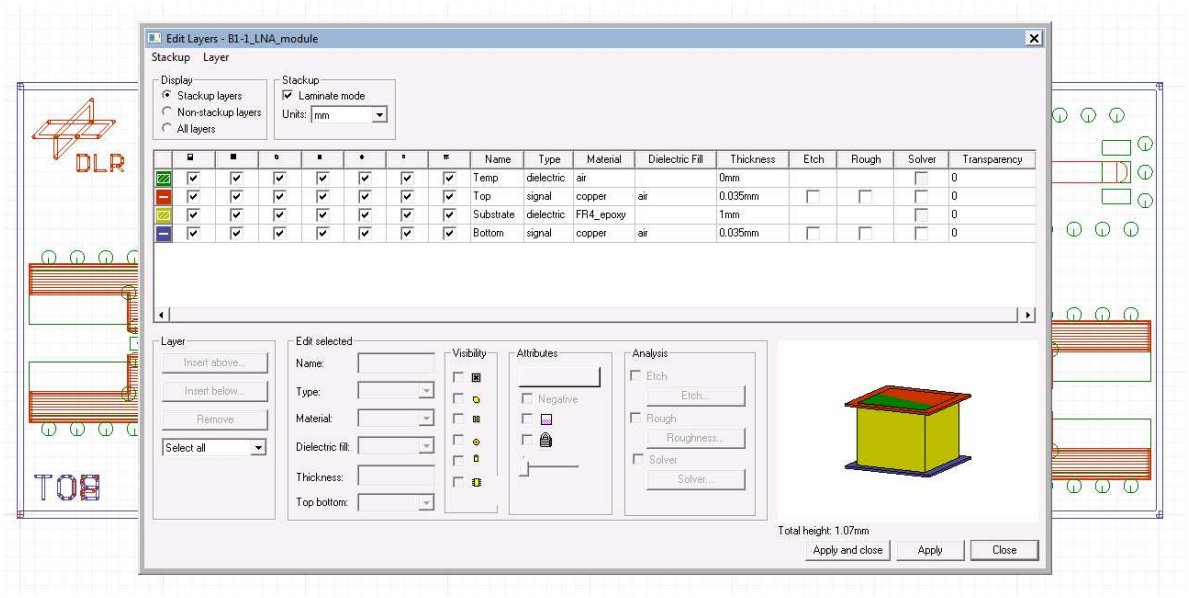
Source: The author.

The vias layer consists on the places that the vias will be created. The details about this process will be described in subsection 4.1.4.

4.1.3 Setting up the PCB stack-up

The third step consists on setting the PCB stackup and adjusting the physical position of the PCB layers, including the layer thicknesses and the choice of the materials to be used. For the present case, the dielectric substrate chosen was FR4, the thickness between top and bottom layer was defined as 1 mm and the thickness of the copper cladding as 0.035 mm. Fig. 106 shows the details of final stackup.

Figure 106 – Details of the PCB stack-up.



Source: The author.

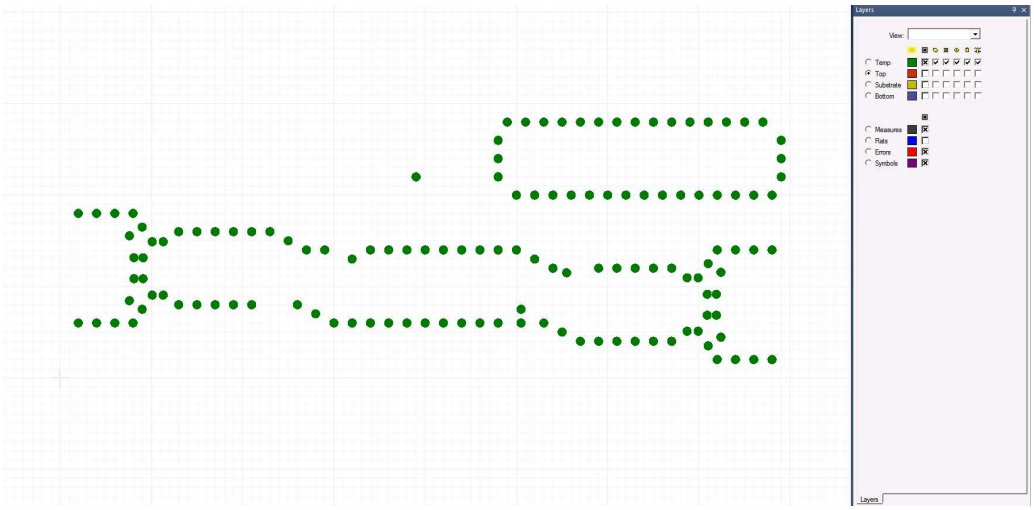
The vias layer is necessary to execute step 4. After that, this layer can be deleted and a new layer must be created, in this case the substrate layer.

4.1.4 Recreating the vias from the original PCB

In the fourth step, the vias from the original PCB can be included in the model in two ways: using a manual process, choosing one layer as reference, or creating a script considering a template that can be accepted by the Designer software. In this subsection, the manual case will be presented, while the process to include the vias using a script will be presented in the Section 4.2.

The manual procedure means that each via may be alocated one-by-one considering the vias positions (temporary layer) through the via dialog box. Considering that just the holes are kept in the temporary layer, the other signals should be changed to the top layer. Fig. 107 shows the vias allocated on the right places.

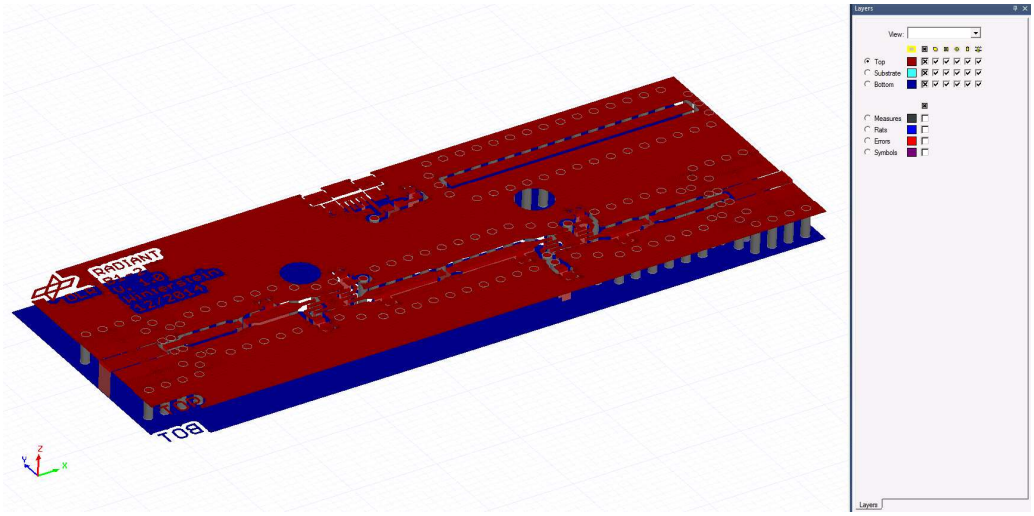
Figure 107 – Allocation of the vias in the PCB.



Source: The author.

After that, the temporary layer can be deleted, hence keeping just the top, bottom and substrate layers. Fig. 108 presents an isometric view of the model after these changes.

Figure 108 – PCB with the final layers, isometric view.

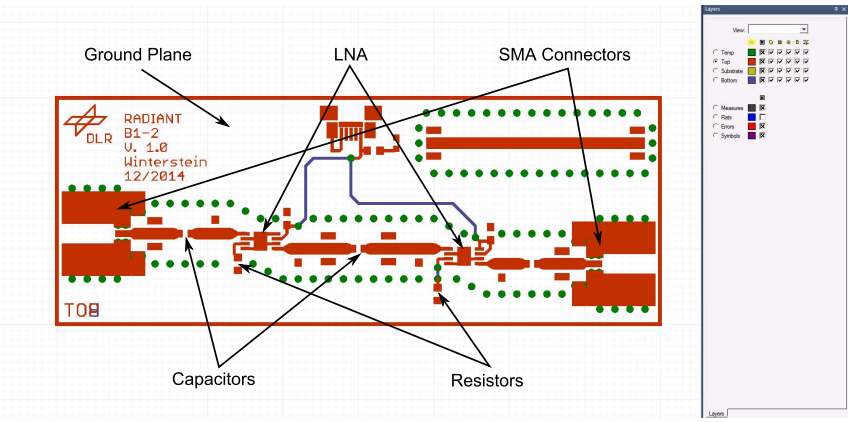


Source: The author.

4.1.5 Setting up the ports and HFSS extents

The fifth step consists on setting the ports and HFSS extents, including the airbox size on the HFSS solver. The ports must be allocated selecting the correct face and then creating the port through Assign excitation->Wave port. In the LNA design, 20 ports were created for the SMA input and output, capacitors, resistors, LNAs and ground planes, as shown in Fig. 109.

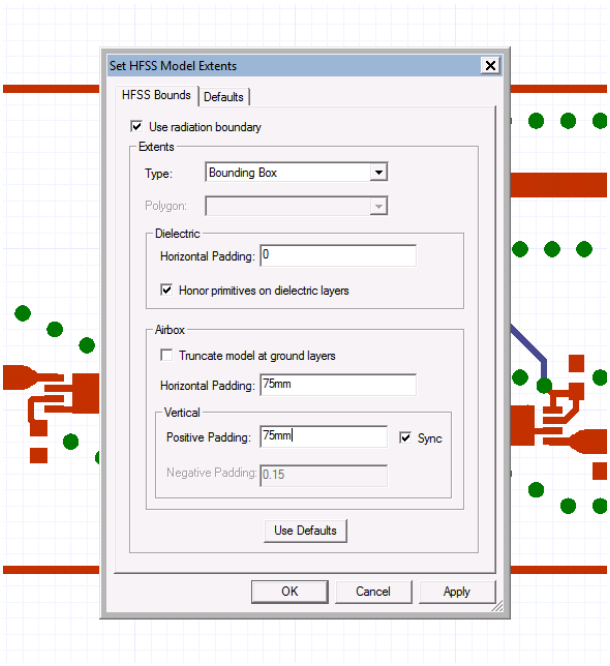
Figure 109 – Creating ports in the PCB, top view.



Source: The author.

The HFSS extents must be set up to be used in the HFSS solver, using the tool following EM Design->HFSS Extents and changing the padding setup as shown in Fig. 110.

Figure 110 – Setting up the HFSS extents.

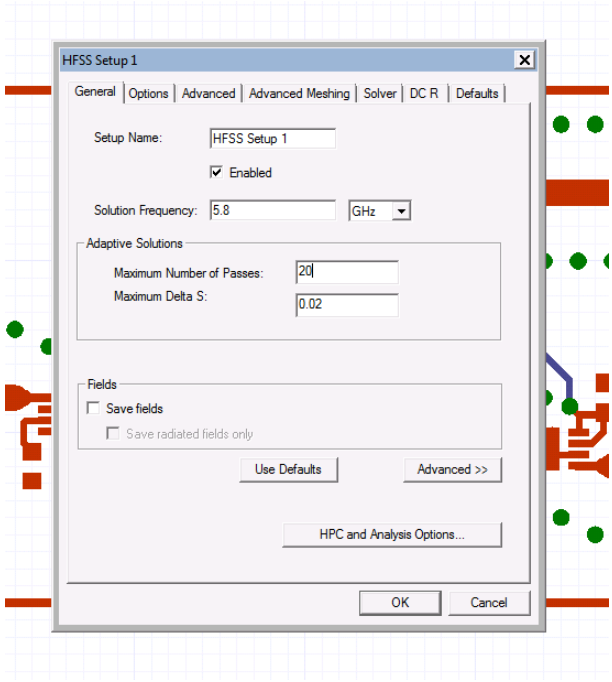


Source: The author.

4.1.6 HFSS setup

In the sixth step, the inclusion of an HFSS setup in order to start an electromagnetic simulation from the Designer layout interface is carried out. This can be done in Analysis->Add HFSS Solution Setup, where parameters as frequency solution, number of passes and maximum delta S are specified. This process is shown in Fig. 111.

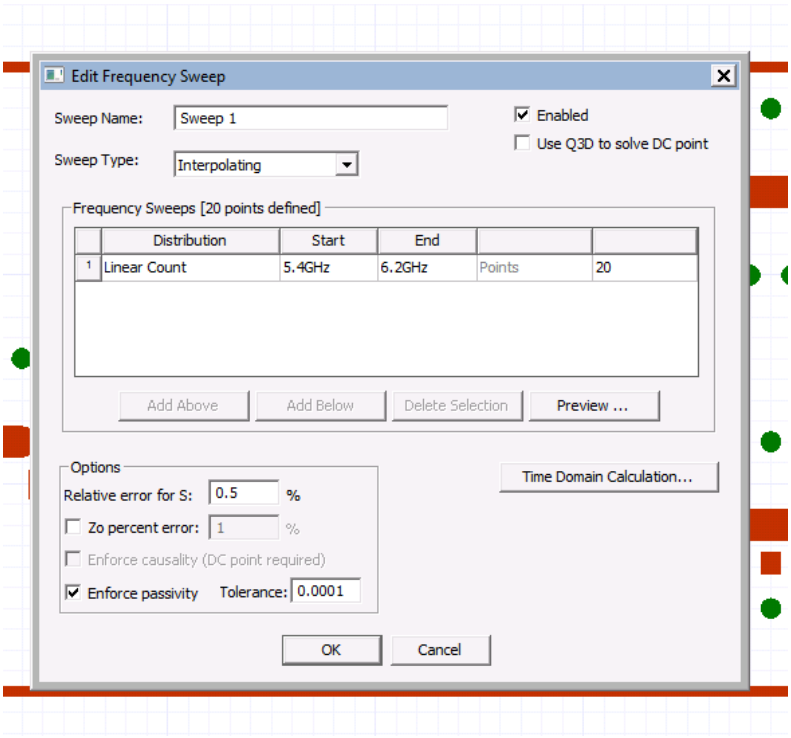
Figure 111 – Dialog box to set up an HFSS solution.



Source: The author.

Then, the frequency sweep must be chosen. In this case, a sweep from 5.4 GHz to 6.2 GHz considering 20 steps was used. This setup is presented in Fig. 112.

Figure 112 – Including an HFSS frequency sweep.



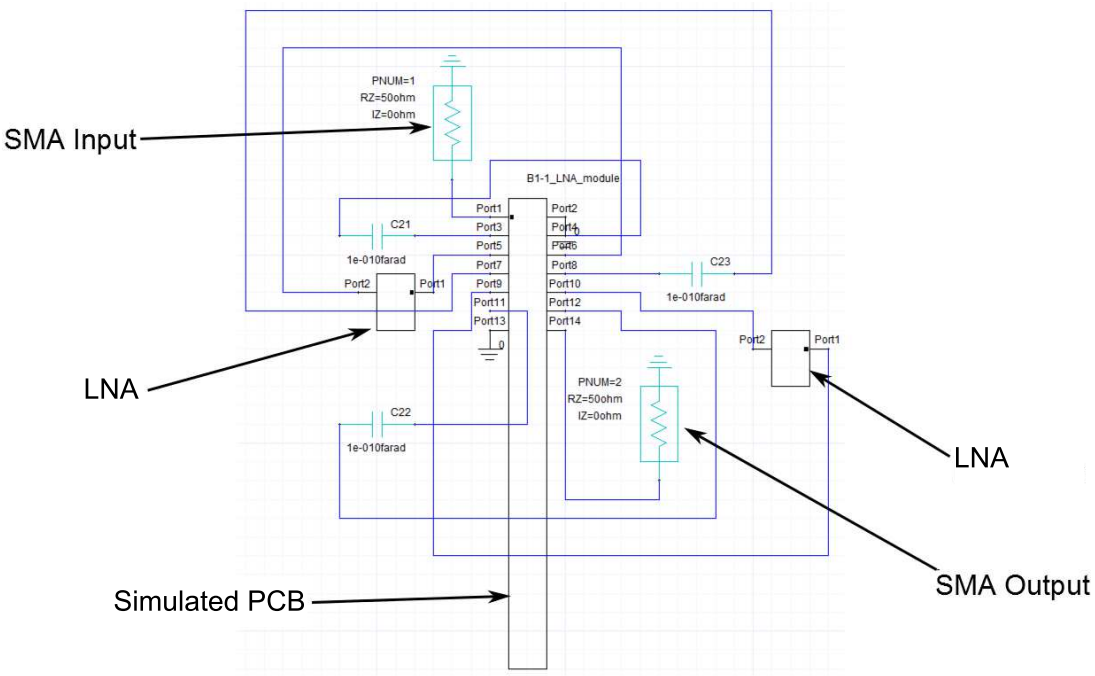
Source: The author.

After specifying the setups, the simulation can be started through the right click in Analysis->Choose Analyze. After the simulation is done, the results can be plotted in terms of reflection and transmission coefficients (S-parameters) for each port and the process to simulate the PCB is finished.

4.1.7 Creating a Circuit Design

Finally, when the PCB simulation is finished, a Circuit Design must be created using the ANSYS Designer in order to perform a linear simulation using the designed board merged with the components. The simulated PCB can be used as an N-port model, thus the components can be connected to the respective ports set in the PCB model. After that, the simulation can be performed. In this case, two LNAs model HMC320, capacitors of 100 pF and 10 nF, resistors of 22 Ω and 174 Ω were used. The LNA behaviour was modeled through the touchstone files provided by the manufacturer and the other components are found in the Designer library. Fig. 113 shows the connections between the PCB N-port model and the respective components.

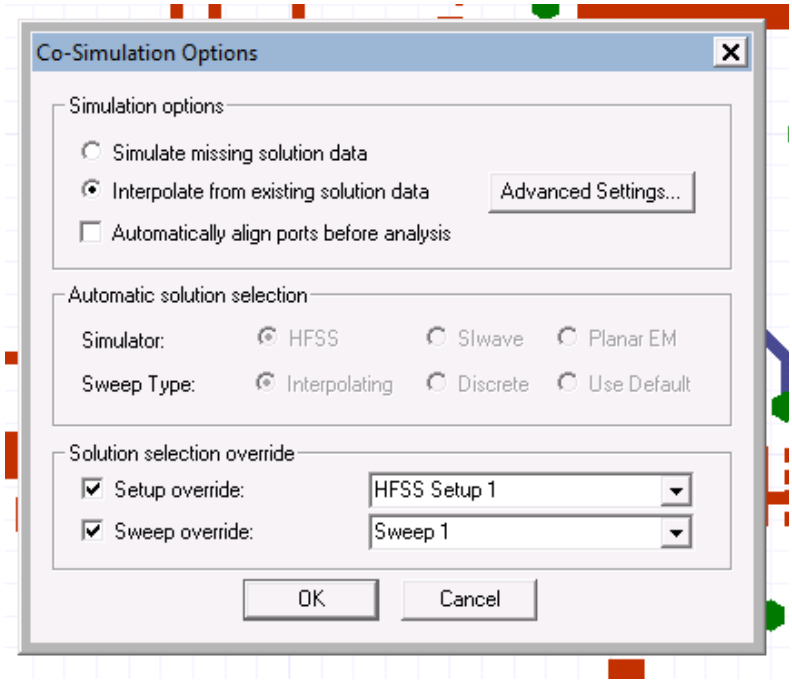
Figure 113 – Circuit design using the PCB as an N-port model.



Source: The author.

The co-simulation options shall be specified using an EM Model in Analysis->Co-simulation Options, as can be observed in Fig. 114. The co-simulation is an environment using both HFSS and Designer tools simultaneously. The simulated PCB through HFSS and the designed circuit through Designer are linked.

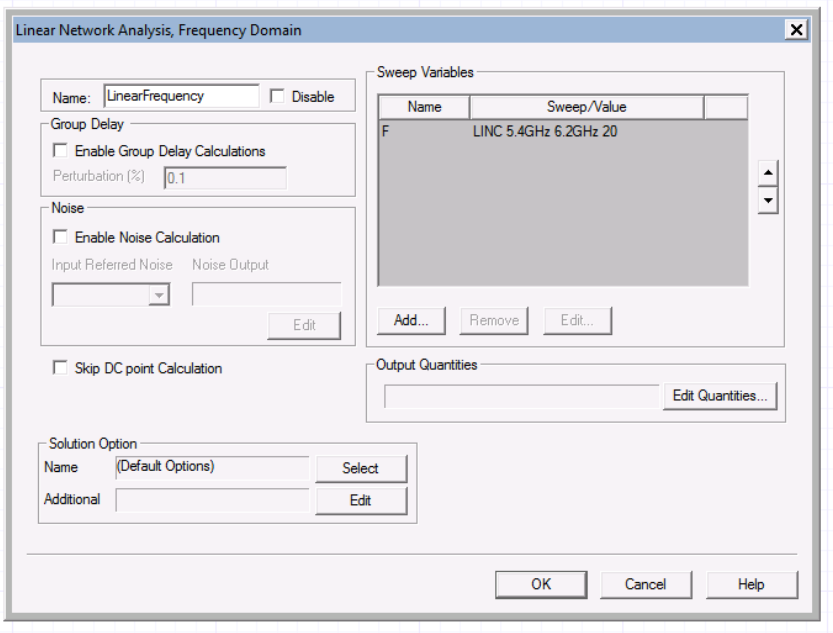
Figure 114 – Setting up a co-simulation.



Source: The author.

Finally, the solution model can be simulated using a Linear Network Analysis in the Frequency Domain, conidering the same frequency range and number of steps used in the PCB simulation. In Circuit->Analysis->Create Linear Network Analysis, this setup can be created. Fig. 115 presents the process to set up these parameters.

Figure 115 – Setting up the Designer setup.

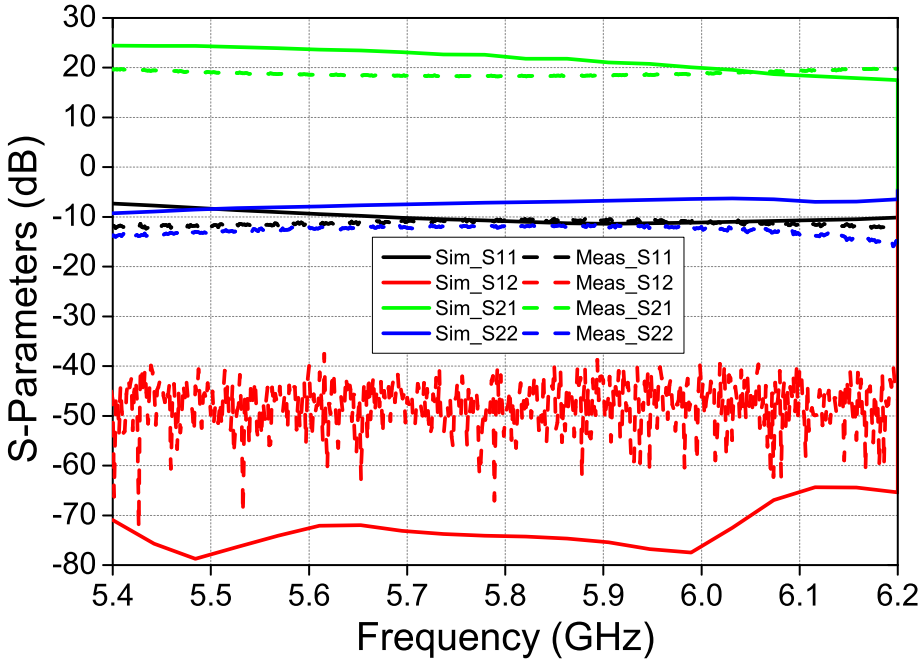


Source: The author.

4.1.8 Simulation of the model

In order to compare and validate the simulated and measured results, the S-parameters were plotted in the same graphic. In Fig. 116, the obtained S-parameters from the simulations presented good performance and similarity with the measurements. The obtained gain at 5.8 GHz with two cascaded LNAs was around 20 dB.

Figure 116 – Reflection and transmission coefficients as a function of the frequency for the PCB simulation, in dB.



Source: The author.

4.2 Script to Include Vias Automatically on PCBs

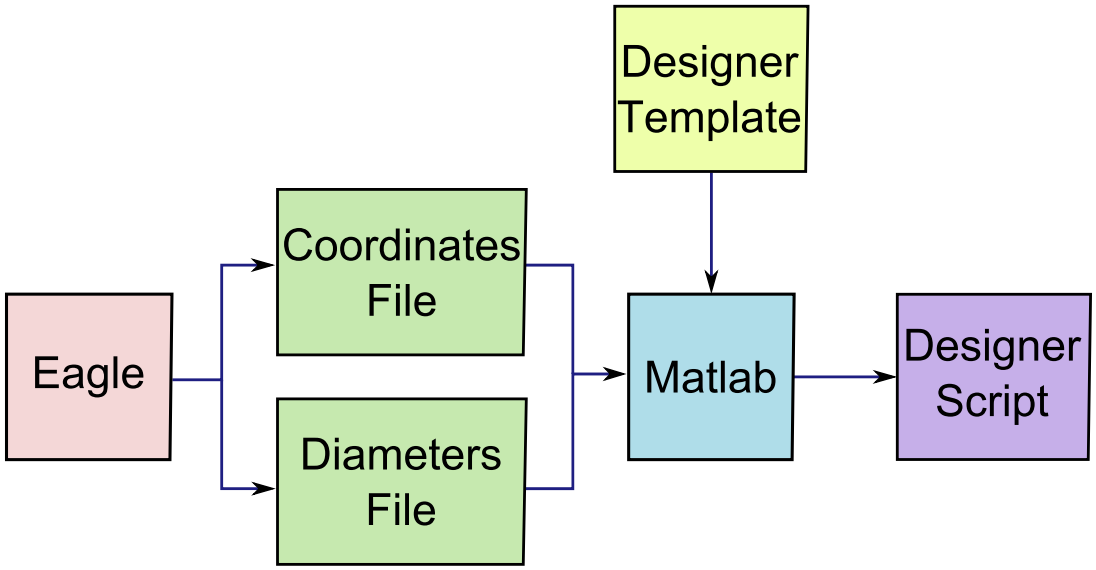
In many projects that demand the insertion of several vias, the manual insertion is cumbersome. Therefore, the creation of a script to do it automatically is necessary. In order to improve the conversion process from PCBs layouts (EAGLE) to PCBs simulations (Ansys Designer), a converter script using MATLAB was proposed. However, this script must be created in a format that can be accepted by the Designer software from the generated gerber files from the layout software. This script was written considering the following steps:

- Designer script template
- Setup of the input parameters
- Import and setup via diameters

- Import and setup via coordinates
- Create an Ansys Designer script output
- Validation of the script

The script basically works following the fluxogram shown in Fig 117. Firstly, two gerber files (drill and diameter files) in text extension containing information about the vias, such as diameters and coordinates may be exported from EAGLE. Then, these two files are imported and used in MATLAB. After that, knowing the Designer script model, the MATLAB interprets and merges the created text files from EAGLE with the Designer template, thus creating the output file as a Designer script (MAGALHÃES et al., 2016).

Figure 117 – Flow chart of the script steps.



Source: The author.

In the following subsections, the step-by-step procedure to convert vias of a PCB layout to a PCB simulation format using the script developed in MATLAB will be presented.

4.2.1 Designer script template

The first step consists of knowing the structure of the script template accepted by the Designer software. Therefore, creating an example with two vias using Tools->Record Script to File in the Designer software, a Designer script template can be generated. The script language is the Visual Basic Scripting Edition (VBScript - .vbs Extension). An example of the created model is shown in Appendix A.

4.2.2 Setup of the input parameters

Some input parameters such project name, design name, height of the vias must be set in MATLAB to avoid errors in the Designer script. As it can be observed in Appendix A, the script template is composed of two parts: the information about the Designer file and then of the vias. For the Designer information, it is necessary only to insert the project name and the design name as shown in Appendix B -> Lines 4-5 to Appendix A -> Lines 14-15. After that, the height of each via from the layers should be inserted. For example, from top layer (t) to bottom layer (b) as done in Appendix B -> Lines 9-10 to Appendix A -> Line 22 and 28.

4.2.3 Import and setup of via diameters

In the third step, the insertion and setting up of all via diameters are carried out. The import of a generated .dlr file by the layout tool should be converted to a .txt file, which contains the information about the via diameters. Then, the positions of each different diameter can be found in the imported text file (diameters.txt). After that, the values should be defined and converted from string to number. Finally, a vector with the size of each different diameter containing the respective name is created. This process can be seen in Appendix B -> Lines 12-31.

4.2.4 Import and setup of via coordinates

In the fourth step, the importing and setting up of the coordinates are performed. Firstly, a .drd file generated by the layout tool (EAGLE - Cam Processor) must be imported and converted to a .txt file. This file contains the information about the coordinates for each different diameter. Then, the coordinates (x,y) for all the vias and each different diameter should be found in the imported text file (drill.txt); thus creating a relation between the diameters and the coordinates. After that, the values must be defined and converted from string to number and also from inch to millimeters. Finally, a matrix containing the via coordinates regarding to the respective diameter is created. Appendix B -> Lines 33-96 show the developed code for the described process.

4.2.5 Creation of a Ansys Designer script output

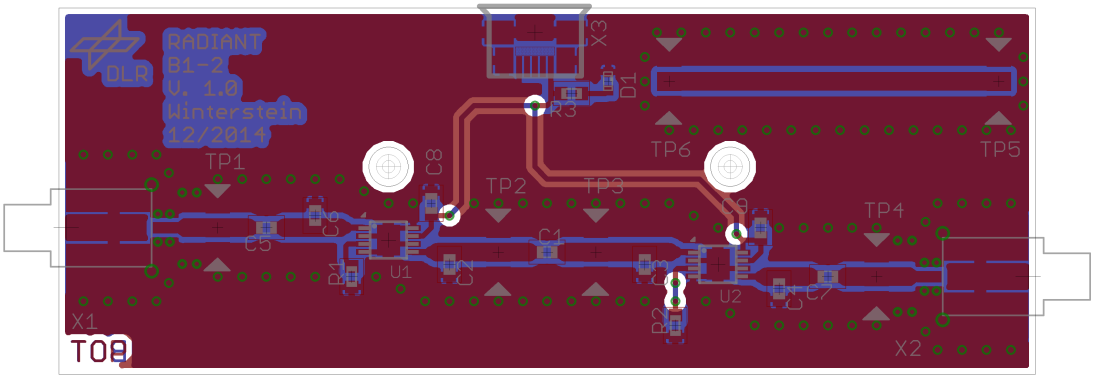
Finally, the designer template with the obtained coordinates and diameters must be merged by the text files. It is possible to create a script that can be read by Ansys Designer software using the same input information and structure as in Appendix A, and creating a relation with the obtained values from EAGLE files. This process can be seen in Appendix B - Lines 98-153.

4.2.6 Validation of the script

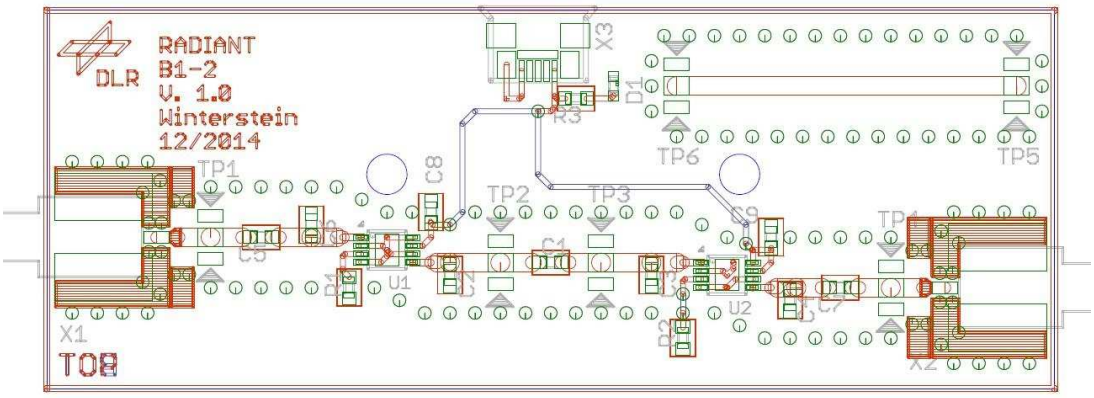
In order to compare the produced PCB layout using the Designer software with the EAGLE layout, Fig. 118 shows both layouts. As it can be observed, the vias are placed in the correct positions. Therefore, the validation showed that the script used is a good option to decrease the conversion time of PCB layouts into the simulation models. Also, comparing the developed script with the manual procedure (one-by-one), larger accuracy in the coordinates and number of vias could be observed. Possible errors for the manual procedure include: missing of vias, vias allocated in the wrong place and vias with incorrect diameter.

Figure 118 – Comparison and validation of the Designer script.

(a) EAGLE layout.



(b) Designer layout.



Source: The author.

5 Conclusion

The main contributions of this work are the design of a dual-band and dual-polarized antenna array suitable for retrodirective systems, the development of the necessary hardware to control the transmitting part of this array, and the development of a procedure to simulate printed circuit boards (PCBs) operating at microwave frequencies.

The scenario for the retrodirective system was described and the antenna array was optimized with ANSYS HFSS. Good results in terms of axial ratio, impedance matching and gain were achieved in the simulations. The experimental results show some deviation from the simulations. However, due to the complexity of the structure, the measured performance was considered acceptable.

The second contribution was the development of a procedure to simulate the electromagnetic behaviour of PCBs operating at microwave frequencies. A MATLAB code was developed to make the insertion of vias into the model in an automatic way. Experimental results were used to validate the proposed approach, which has provided good predictions of the experimental results.

The third goal was the development of the complete architecture for the transmitting channels to be connected to the array developed in this work. Prior to the selection of the final architecture, all the components were tested individually. After this procedure, the eight channels have been integrated and measured. The calibration coefficients needed for the correct operation of the array have been experimentally determined. Since there are two mixing stages, these coefficients have been determined in a two-step approach whereby the total phase shift has been estimated from the measured values.

Future activities of this work include the measurement of the developed antenna array connected to the Tx-channels, as well as to the controlling FPGA unit. A simpler version of the antenna array, with an easier fabrication procedure, would also be desirable. These tests are important to verify whether the beamforming algorithm works correctly and the calibration coefficients are accurate enough.

APPENDIX A – Designer Template

```
' ----------------------------------------------
' Script Recorded by Ansoft Designer Version 2014.0.0
' 8:31:02  Jun 16, 2015
' ----------------------------------------------
Dim oAnsoftApp
Dim oDesktop
Dim oProject
Dim oDesign
Dim oEditor
Dim oModule
Set oAnsoftApp = CreateObject("AnsoftDesigner.DesignerScript")
Set oDesktop = oAnsoftApp.GetAppDesktop()
oDesktop.RestoreWindow
Set oProject = oDesktop.SetActiveProject("Project1")
Set oDesign = oProject.SetActiveDesign("EMDesign1")
Set oEditor = oDesign.SetActiveEditor("Layout")

oEditor.CreateVia Array("NAME:Contents", "name:=", "via_1",
  "ReferencedPadstack:=",  _ "PlanarEMVia", "vposition:=", Array("x:=",
  "10.020046mm", "y:=",  _ "4.035044mm"), "vrotation:=", Array("0deg"),
  "overrides hole:=", true, "hole diameter:=", Array(  _ "0.40mm"),
  "Pin:=", false, "highest_layer:=", "t", "lowest_layer:=", "b")

oEditor.CreateVia Array("NAME:Contents", "name:=", "via_2",
  "ReferencedPadstack:=",  _ "PlanarEMVia", "vposition:=", Array("x:=",
  "11.219942mm", "y:=",  _ "4.035044mm"), "vrotation:=", Array("0deg"),
  "overrides hole:=", true, "hole diameter:=", Array(  _ "0.40mm"),
  "Pin:=", false, "highest_layer:=", "t", "lowest_layer:=", "b")
```

APPENDIX B – MATLAB Code for Automatic Import of Vias

```
%% Input Parameters

% Setting the project names
project_name='Project1';
design_name='EMDesign1';
hora_data=datestr(now,'HH:MM:SS mmm dd, yyyy');

% Setting the vias height from the layers
layer_begin='t';  %(From Top Layer)
layer_finish='b'; %(To Bottom Layer)

%% Setting the vias diameters
diameters_name='diameters.txt';            %Name of text file
diameters_file=importdata(diameters_name); %Importing .txt file
diameters_char=char(diameters_file);
diameter_size=size(diameters_char);
diameter_lines=diameter_size(1,1);

% Setting the number of different diameters
for i=1:diameter_lines

    %Finding the position of the diameters in the text file
    posicao_dia=find(diameters_char(i,:)=='.');
    %Obtaining the diameters value
    valor=diameters_char(i,posicao_dia-1:end-2);
    %Converting from string to number
    valor=str2num(valor);
    %Creating a vector with the diameters
    diameters(i,1)=valor;

end

%% Setting the vias coordinates (x,y) and name
drill_name='drill.txt';              %Name of text file
drill_file=importdata(drill_name);  %Importing .txt file
drill_char=char(drill_file);
drill_size=size(drill_char);
drill_lines=drill_size(1,1);        %Setting the number of vias
cont=1;
```

```
string_T='T';
string_X='X';

% Finding the position of each diameter
for i=1:drill_lines
    if drill_char(i)==string_T && drill_char(i+1)==string_X

        save_pos_dia(cont)=i;
        cont=cont+1;

    else

    end

end

% Calculating the number of vias for each diameter
for i=1:diameter_lines-1

numero_drills(i)=save_pos_dia(i+1)-save_pos_dia(i)-1;
numero_drills(diameter_lines)=drill_lines-save_pos_dia(diameter_lines)-1;

end

soma_diameters_passo=zeros(1,diameter_lines);
for i=1:diameter_lines-1
    soma_diameters_passo(i+1)=soma_diameters_passo(i)+numero_drills(i);
end

soma_drills=0;
for i=1:diameter_lines
    soma_drills=soma_drills+numero_drills(i);
end

% Finding the drill coordinates
cont_pos=1;
cont_drill=1;
for i=1:drill_lines
            if i==save_pos_dia(1)+cont_pos
                if drill_char(i)==string_X

                posicao_x=find(drill_char(i,:)=='X');
                posicao_y=find(drill_char(i,:)=='Y');
                valor_x=drill_char(i,posicao_x+1:posicao_y-1);
                valor_y=drill_char(i,posicao_y+1:end);
                valor_x=str2num(valor_x);
                valor_y=str2num(valor_y);
```

```
                drill(cont_drill,1)=(valor_x/10000)*2.54;
                drill(cont_drill,2)=(valor_y/10000)*2.54;
                cont_drill=cont_drill+1;

                else
                end
                cont_pos=cont_pos+1;
            else
            end
end

%% Output Designer Script Model .vbs

% Generating the strings to be alocated in the text file
fprintf(''' ----------------------------------------------\n');
fprintf(''' Script Recorded by Ansoft Designer Version 2014.0.0\n');
fprintf(''' %s\n',hora_data);
fprintf(''' ----------------------------------------------\n');
fprintf('Dim oAnsoftApp\n');
fprintf('Dim oDesktop\n');
fprintf('Dim oProject\n');
fprintf('Dim oDesign\n');
fprintf('Dim oEditor\n');
fprintf('Dim oModule\n');
fprintf('Set oAnsoftApp = CreateObject("AnsoftDesigner.DesignerScript")
\n');
fprintf('Set oDesktop = oAnsoftApp.GetAppDesktop()\n');
fprintf('oDesktop.RestoreWindow\n');
fprintf('Set oProject = oDesktop.SetActiveProject("%s")\n',project_name);
fprintf('Set oDesign = oProject.SetActiveDesign("%s")\n',design_name);
fprintf('Set oEditor = oDesign.SetActiveEditor("Layout")\n\n\n');

contador_vias=1;
for j=1:diameter_lines
    if soma_diameters_passo(j)~=0
        for i=1:numero_drills(j)

        fprintf('oEditor.CreateVia Array("NAME:Contents", "name:=",
         "via_%d", "ReferencedPadstack:=",  _\n  "PlanarEMVia",
         "vposition:=", Array("x:=", "%.6fmm", "y:=",  _\n  "%.6fmm"),
         "vrotation:=", Array("0deg"), "overrides hole:=", true,
         "hole diameter:=", Array(  _\n  "%.2fmm"), "Pin:=", false,
         "highest_layer:=", "%s", "lowest_layer:=", "%s")\n\n',
         contador_vias, drill(i+soma_diameters_passo(j),1),
         drill(i+soma_diameters_passo(j),2), diameters(j),
         layer_begin, layer_finish);
         contador_vias=contador_vias+1;
```

```
134
135         end
136
137     elseif soma_diameters_passo(j)==0
138
139         for i=1:numero_drills(j)
140
141         fprintf('oEditor.CreateVia Array("NAME:Contents", "name:=",
142          "via_%d", "ReferencedPadstack:=",  _\n  "PlanarEMVia",
143          "vposition:=", Array("x:=", "%.6fmm", "y:=",  _\n  "%.6fmm"),
144          "vrotation:=", Array("0deg"), "overrides hole:=", true,
145          "hole diameter:=", Array(  _\n  "%.2fmm"), "Pin:=", false,
146          "highest_layer:=", "%s", "lowest_layer:=", "%s")\n\n',
147          contador_vias, drill(i,1), drill(i,2), diameters(j),
148          layer_begin, layer_finish);
149          contador_vias=contador_vias+1;
150
151         end
152     end
153 end
```

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