FEDERAL UNIVERSITY OF PAMPA

Diego Maran de Mattos

INTEGRATED DC-DC CONVERTER DESIGN FOR PHOTOVOLTAIC ENERGY HARVESTING IN INDOOR ULTRA-LOW VOLTAGE AND LOW-POWER ENVIRONMENTS

Alegrete/RS
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Master's Thesis submitted to the Graduate Program in Electrical Engineering of Federal University of Pampa in partial fulfillment of the requirements for the degree of Master in Electrical Engineering.

Supervisor: Alessandro Gonçalves Girardi
Co-supervisor: Lucas Compassi Severo

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ABSTRACT

Energy Harvesting stands out as an emerging technology in the 21st century, finding diverse applications, especially in the realm of batteryless systems, where the goal is to eliminate dependence on conventional batteries. A range of energy sources, including light, thermal, vibration, and electromagnetic energies, are potential candidates for harvesting. Although thermal and vibration prove less reliable for indoor use, indoor light energy, emanating from artificial sources such as fluorescent light bulbs or light-emitting diodes (LEDs), emerges as a promising avenue for sustained energy harvesting.

In the domain of ultra-low power systems, particularly those associated with the Internet of Things (IoT), the role of DC-DC converters is paramount. Switched-capacitor DC-DC converters demonstrate superiority in integrated-form applications, boasting higher power density and ease of implementation in CMOS technologies. However, the efficiency of these converters is influenced by the non-ideal nature of transducers like photovoltaic cells, which introduce finite series resistance. Consequently, analytical models are imperative to incorporate and address the effects of series resistance in switched-capacitor converters.

Given that a significant proportion of electronic devices is predominantly utilized indoors, the appeal of energy harvesting as a solution becomes evident. This is especially relevant for powering electronic devices and IoT sensor nodes, contributing to a sustainable and efficient energy ecosystem. The focus on harnessing indoor light energy showcases the potential for continuous power generation, offering a promising avenue for reducing our reliance on traditional power sources and batteries in indoor environments.

This work specifically characterizes a 20 x 40 mm photovoltaic (PV) cells under various indoor ambient lighting conditions (50 to 500 lux), using a detailed 1D2R model electrical model including a diode, series, and shunt resistances to capture PV cell behavior and non-linearities. Small-signal AC models account for dynamic resistances and equivalent capacitances critical for visible light communication (VLC) and energy harvesting co-design. Measurement and parameter extraction results demonstrate the trade-off between maximum power point operation for energy harvesting and bias points favoring communication bandwidth, guiding optimal PV cell biasing strategies. The PV cell delivers approximately 28.09 μW of power, with a stable voltage output ranging from 0.18 V to 0.28 V under indoor lighting conditions.

An integrated switched-capacitor DC-DC converter topology employing a series-parallel configuration is proposed, designed and simulated in 65 nm CMOS technology. To overcome startup challenges at ultra-low input voltages typical of indoor harvesting (127 mV to 297 mV), a low-voltage cold-start circuit using a current-starved ring oscillator (CSRO) operating at 16.02 MHz, clock boosting, and a multi-stage Dickson charge pump is developed. Post-startup, the control circuit regulates output voltage ($\approx$0.5 V) through a finely controlled Current-Starved Ring Oscillator frequency, modulated by a error amplifier

and current mirror system. Transmission gates with minimal on-resistance and Bootstrap circuit enhance converter efficiency by reducing conduction losses.
Transient simulations validate the stable operation of the energy harvesting system under indoor lighting, illustrating effective voltage multiplication with low ripple and noise, suitable for ultra-low-power IoT devices. The efficiency of the switched-capacitor circuit varies with illuminance, peaking at approximately 65.8% around 420 lux and decreasing to about 65.1% at 500 lux. While both input and output power increase with illuminance, power losses also grow, explaining the modest efficiency decline at higher light levels. These insights highlight the system's sensitivity to ambient lighting and the trade-offs between power availability and conversion efficiency, underscoring the importance of optimizing switched-capacitor designs for varying indoor environments.
The systematic design approach and parameter extraction methodology advance the state-of-the-art for integrated indoor photovoltaic energy harvesting, enabling battery-less, sustainable, and efficient power management for future ubiquitous sensing and IoT applications.

Keywords: Switched Capacitor. DC-DC converter. Indoor Energy Harvesting. Photovoltaic Cell Modeling. Electronic Devices. Ultra-Low Power Circuits.

RESUMO

A colheita de energia desponta como uma tecnologia emergente no século XXI, encontrando diversas aplicações, especialmente no campo de sistemas sem bateria, onde o objetivo é eliminar a dependência de baterias convencionais. Uma variedade de fontes de energia, incluindo luz, térmica, vibração e energias eletromagnéticas, são candidatas potenciais para colheita. Embora a energia térmica e de vibração se mostrem menos confiáveis para uso em ambientes internos, a energia luminosa interna, proveniente de fontes artificiais como lâmpadas fluorescentes ou diodos emissores de luz (LEDs), emerge como uma promissora alternativa para colheita contínua de energia.

No domínio de sistemas de ultra baixa potência, especialmente aqueles associados à Internet das Coisas (IoT), o papel dos conversores DC-DC é fundamental. Os conversores DC-DC de capacitor chaveado demonstram superioridade em aplicações de forma integrada, apresentando maior densidade de potência e facilidade de implementação em tecnologias CMOS. No entanto, a eficiência desses conversores é influenciada pela natureza não ideal de transdutores como células fotovoltaicas, que introduzem uma resistência em série finita. Consequentemente, modelos analíticos são imperativos para incorporar e abordar os efeitos da resistência em série nos conversores de capacitor chaveado.

Considerando que uma parcela significativa dos dispositivos eletrônicos é predominantemente utilizada em ambientes internos, o apelo da colheita de energia como solução torna-se evidente. Isto é especialmente relevante para alimentar dispositivos eletrônicos e nós sensores de IoT, contribuindo para um ecossistema de energia sustentável e eficiente. O foco na captação da energia luminosa interna evidencia o potencial para geração contínua de energia, oferecendo uma alternativa promissora para reduzir a dependência de fontes tradicionais de energia e baterias em ambientes internos.

Este trabalho caracteriza especificamente células fotovoltaicas (PV) de 20 x 40 mm, sob diversas condições de iluminação ambiente interna (50 a 500 lux), utilizando um modelo elétrico detalhado 1D2R que inclui diodo, resistências série e shunt para capturar o comportamento e as não linearidades da célula PV. Modelos AC de pequeno sinal consideram resistências dinâmicas e capacitâncias equivalentes, essenciais para o co-design de comunicação por luz visível (VLC) e colheita de energia. Resultados de medição e extração de parâmetros demonstram o trade-off entre operação no ponto de máxima potência para colheita e pontos de polarização favoráveis à largura de banda da comunicação, guiando estratégias ótimas de polarização da célula PV. A célula PV fornece aproximadamente 28,09 μW e potência, com saída de tensão estável variando de 0,18 V a 0,28 V sob condições de iluminação interna.

Propõe-se um topologia integrada de conversor DC-DC de capacitor chaveado empregando configuração série-paralelo, projetada e simulada em tecnologia CMOS de 65 nm. Para superar desafios de partida em tensões de entrada ultrabaixas típicas da colheita interna (127 mV a 297 mV), desenvolve-se um circuito de cold-start de baixa tensão utilizando

oscilador de anel com corrente limitada, Current-Starved Ring Oscillator, CSRO) operando a 16,02 MHz, amplificação de clock e um Dickson charge pump de multiestágio. Após a partida, o circuito de controle regula a tensão de saída (≈0.5 V) por meio da frequência do oscilador de anel com corrente limitada, modulada por um amplificador de erro e sistema de espelho de corrente. Portas de transmissão com resistência em condução mínima e circuito Bootstrap aumentam a eficiência do conversor ao reduzir perdas por condução. Simulações transientes validam a operação estável do sistema completo de colheita de energia sob condições de iluminação interna, ilustrando uma multiplicação eficaz da tensão com baixo ripple e ruído, adequado para dispositivos IoT de ultra-baixo consumo. A eficiência do circuito de capacitores comutados varia com a iluminância, atingindo um pico de aproximadamente 65,8% em torno de 420 lux e diminuindo para cerca de 65,1% em 500 lux. Enquanto a potência de entrada e saída aumenta com a iluminância, as perdas também crescem, explicando o modesto declínio de eficiência em níveis de luz mais altos. Essas observações destacam a sensibilidade do sistema à iluminação ambiente e os trade-offs entre disponibilidade de potência e eficiência de conversão, ressaltando a importância de otimizar designs capacitores comutados para diferentes ambientes internos. A abordagem sistemática de projeto e a metodologia de extração de parâmetros avançam o estado da arte para a colheita integrada de energia fotovoltaica interna, viabilizando gerenciamento de potência sustentável, eficiente e sem bateria para futuras aplicações ubíquas de sensoriamento e IoT.

Palavras-chave: Capacitor Chaveado. Conversor CC-CC. Colheita de Energia Interna. Modelagem de Células Fotovoltaicas. Dispositivos Eletrônicos. Circuitos de Ultra-Baixa Potência.

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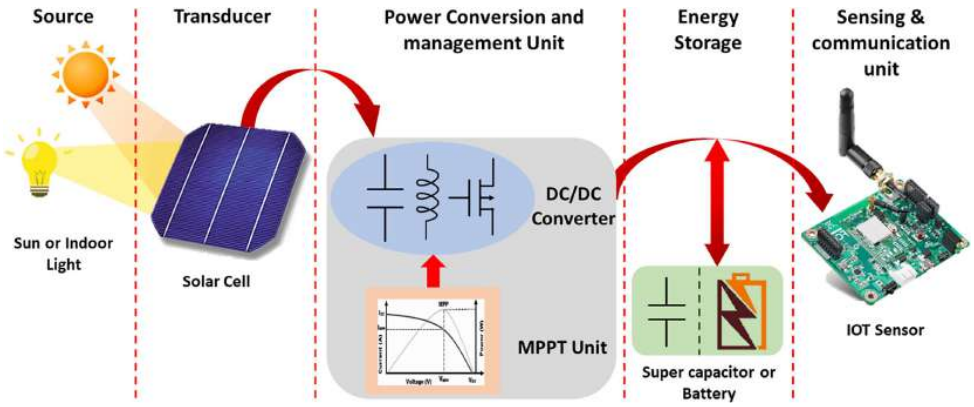
1 INTRODUCTION

The energy harvesting using the environment as energy source has recently attracting attention, that is due to the necessity of powering remote electronics devices and implanted or embedded electronics (CHEN; WANG; WONG, 2015). Energy harvesting offer a solution to eliminate the necessity of wiring or batteries, enhancing the portability and autonomy of devices while diminishing the need for maintenance and minimizing the chemical waste generation (RADIN et al., 2022).

The most know and abundant environment energy source is the luminous energy, having it source either solar light for outdoor applications or artificial light for indoor applications. To harvest the luminous energy source it necessary a photovoltaic (PV) cell to act as a transducer, a DC-DC converter that act as an unit for power conversion and management (PCMU), the energy storage device using a battery or a super-capacitor is optional in case of a power hungry devices and a sensor or node (AHMAD; GHENAI; BETTAYEB, 2021). A MPPT algorithm is employed in the converter to maximize the extracted power, the algorithm is necessary due to the nonlinear voltage-current relationship of the PV cell (RADIN et al., 2022). In Figure 1 is a block diagram of a PV energy harvesting system.

Figure 1 – Block Diagram of PV Energy Harvesting System.

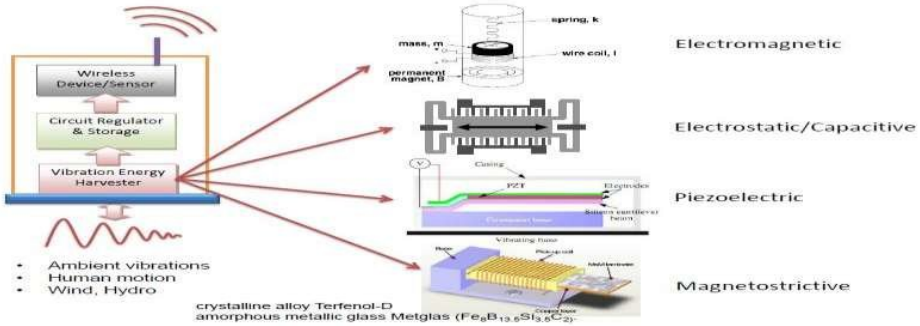


Source: From (AHMAD; GHENAI; BETTAYEB, 2021).

Vibrational energy harvesting have it source from vibration turning mechanical energy into electrical energy (WEI; JING, 2017). The vibration source can come from the environment i.e. the ocean waves or from human body by means of motion (RADIN et al., 2022; WEI; JING, 2017). The most common energy conversion mechanism employed are the electrostatic, electromagnetic, and piezoelectric transducer (RADIN et al., 2022; DEEPAK; GEORGE, 2021). The piezoelectric effect was first discovered in 1880 by the brothers Pierre and Jacques Curie, in which was observed that when a crystal is compressed it generate a positive and a negative charge on several part of the crystal, this phenomenon was named in 1881 by Hankel where piezo means pressure in Greek (ARNAU et al., 2004). Piezoelectric transducers function by utilizing the piezoelectric effect to transform surrounding vibrations

into electrical energy (ERTURK; INMAN, 2011). The electromagnetic energy harvester use the relative motion between a permanent magnet and a coil, inducing current in the coil (ROY; MALLICK; PAUL, 2019). The electromagnetic transducers are distinguished by their low internal (coil) resistance, output voltage moderately low and current output high (ROY; MALLICK; PAUL, 2019). Electrostatic harvester requires an external voltage source as well a precise conversion circuit to extract electrical energy from mechanical vibrations during operation (KHAN; QADIR, 2016). In figure 2 is a block diagram of a vibrational energy harvesting system.

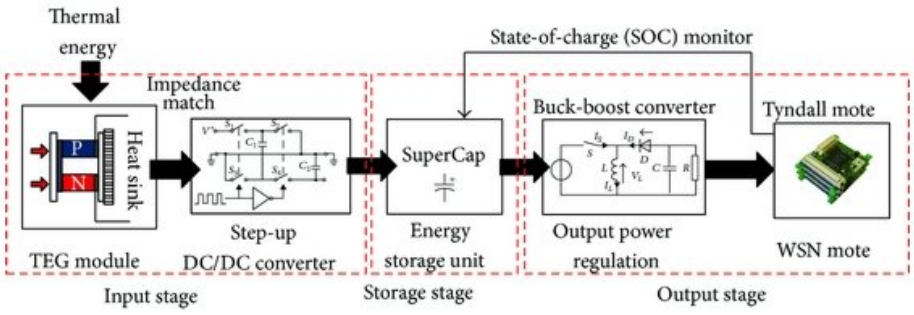
Figure 2 – Block Diagram of Vibrational Energy Harvesting System.



Source:From (KUMAR,)

Thermal energy harvesters (TEHs) usually belong to the static type category, featuring a stationary hot source at one end and a cold source at the opposite end (BAKYTBEKOV et al., 2022). TEH is a practical approach to energize on-body devices, tapping into the inherent heat produced by the human body (RADIN et al., 2022). A thermoelectric generator (TEG) converts the difference in temperature into electricity by means of the Seebeck effect, this process is present in the semiconductor and in the conductors (RADIN et al., 2022). In Figure 3 is a block diagram of a thermal energy harvesting system.

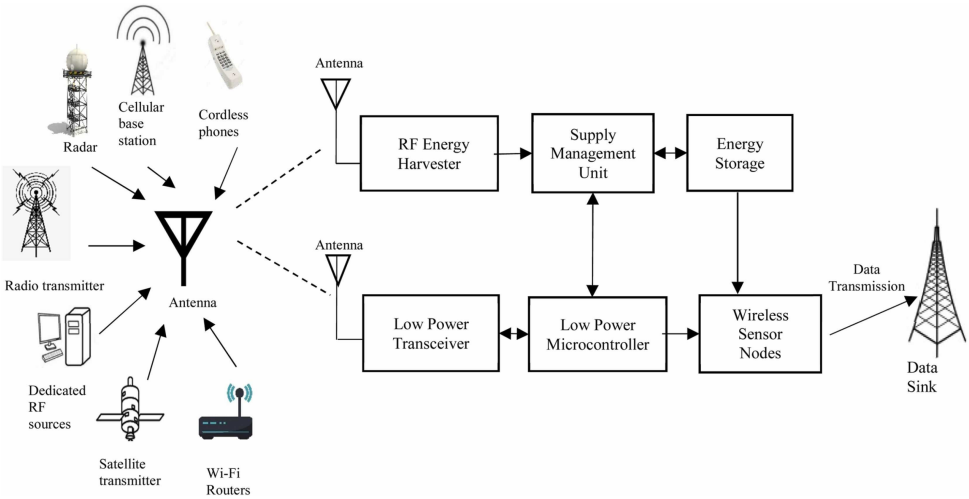
Figure 3 – Block Diagram of Thermal Energy Harvesting System.



Source: From (WANG et al., 2013).

Radio frequency (RF) energy has the lowest power density when compared with other ambient energy sources, however it can be harvested from electromagnetic waves spanning a wide and populated areas were the RF sources are widely available making this a very attractive option (CANSIZ; ALTINEL; KURT, 2019; Van Breussegem; STEYAERT, 2013). Electromagnetic waves from RF energy sources propagate across diverse frequency bands, making them widespread and accessible, even in remote locations, it can be used in combination with wireless powered communication (WPC) and simultaneous wireless information and power transfer (SWIPT) systems (CANSIZ; ALTINEL; KURT, 2019). This energy harvester system has the capability to be a energy source for a wireless sensor networks (WSNs) and internet of things (IoT) (CANSIZ; ALTINEL; KURT, 2019). Figure 4 illustrates the block diagram of the RF energy harvesting system.

Figure 4 – Block Diagram of RF Energy Harvesting System.



Source: From (SHARMA; SINGH, 2023).

In table 1 a comparison of the power density of the energy sources mentioned above is shown.

Table 1 presents a comparison of the power density values for the energy sources discussed above.

The energy harvesting system necessitates dedicated transducers tailored for harvest distinct energy sources. Furthermore, it requires specialized converters to serve as interfaces between the diverse power sources and the voltage rails essential for powering electronic systems. These transducers and converters play pivotal roles in efficiently capturing and transforming energy from different sources, ensuring seamless integration with electronic components

Table 1 – Power density comparison of alternative energy sources.

Source	Power Density	Harvesting technology
Light	Indoor: 10 $\mu W/cm^2$ Outdoor: 10 mW/cm^2	Photovoltaic
Vibration	Human: 4 $\mu W/cm^2$ Industrial: 100 $\mu W/cm^2$	Piezoelectric Electrostatic Electromagnetic
Thermal	Human: 30 $\mu W/cm^2$ Industrial: 1-10 mW/cm^2	Thermoelectric Pyroelectric
RF	GSM: 0.1 $\mu W/cm^2$ Wi-Fi: 1 mW/cm^2	Patch antenna

Source: From (TRAN; CHA; PARK, 2017).

1.1 OBJECTIVES

The primary objective of this work is to introduce and validate an integrated switched-capacitor DC-DC converter designed for a batteryless energy harvesting system. This system is powered by a photovoltaic cell and incorporates an energy-storing capacitor, eliminating the need for conventional battery usage in ultra-low power devices. The focus is on creating an energy harvesting solution suitable for ultra-low power applications in indoor ambient lighting conditions.

For achieving the objective, we propose the design and validation of an integrated DC-DC switched capacitor converter for a batteryless energy harvesting system powered by a photovoltaic cell, specifically designed for ultra-low power devices intended for indoor ambient lighting levels. This system focuses on utilizing a DC-DC series-parallel switched capacitor converter circuit for low power, low voltage, and batteryless applications. The integrated energy-harvesting system includes a switched-capacitor DC-DC converter to achieve an output voltage of 400 mV using a 20x40 mm photovoltaic cell. The circuit will be implemented in 65-nm CMOS technology.

The specific objectives of this work are the following:

- Characterization of photovoltaic cells under various indoor ambient lighting conditions to gain insights into their limitations and electrical characteristics.
- To propose a DC-DC switched capacitor converter topology with multiple voltage conversion ratios for energy harvesting systems powered by photovoltaic cells.
- To simulate the electrical behavior of the proposed topology to validate its effectiveness.
- To design and optimize the circuit for maximum efficiency, focusing on post-layout simulation and validation of the conversion system.
- To design and implement a test chip for physical evaluation of the proposed system.

These objectives aim to advance the development of energy harvesting systems for ultra-low power devices in indoor ambient lighting environments by leveraging innovative switched-capacitor converter designs and simulation techniques.

1.2 ORGANIZATION OF THE WORK

This work is organized as follows: Chapter 2 presents an overview of the DC-DC converter. Chapter 3 presents a comprehensive literature review of diverse type and application of DC-DC converters. Chapter 4 presents a small signal modeling and parameter extraction for PV cell integration in indoor VLC systems. Chapter 5 proposes an Energy Harvesting system, consisting of cold-star system, control circuit, and a switched capacitor DC-DC converter. Chapter 6 presents the conclusions and Chapter 7 presents the final dissertation schedule of activities.

2 DC-DC CONVERTER

A DC-DC Converter, also referred to as a voltage converter or voltage regulator, is defined as an electronic circuit that converts the DC voltage supplied to the input terminals into a different DC voltage at the output terminals (ERICKSON; MAKSIMOVIC, 2020). The DC Converter acts as a link between the power source and the various voltage rails required in a electronic system (Van Breussegem; STEYAERT, 2013),(MOHAN; UNDELAND; ROBBINS, 2003).

The design of DC-DC converters relies on various conversion techniques, each with specific advantages and trade-offs that dictate their selection based on application requirements. these techniques encompass the choice of circuit topology (e.g., Buck, Boost, Switched-Capacitor), the control strategies (e.g., PWM, PFM), and the specific components utilized to achieve the desired voltage conversion (ERICKSON; MAKSIMOVIC, 2020). To evaluate the performance of different converter prototypes and facilitate objective comparisons, a set of characteristics is employed. This evaluation step is critical for selecting the most suitable converter for a given application, as each design presents distinct requirements. These performance characteristics are conventionally classified into two main groups: dynamic characteristics (such as transient response and settling time) and static characteristics (including efficiency, output ripple, and quiescent current) (Van Breussegem; STEYAERT, 2013), (RASHID, 2018).

2.1 DYNAMIC CHARACTERISTICS

The dynamic characteristics of a DC-DC converter refer to its behavior during transient events or past transients events. These characteristics are influenced by both the converter stage and the control method or circuit used in the DC-DC converter (ERICKSON; MAKSIMOVIC, 2020). The key dynamic characteristics include Line Regulation, Load Regulation, Bandwidth, and Overshoot, a block diagram with all this key dynamic characteristics can be seen in Figure 5 (Van Breussegem; STEYAERT, 2013).

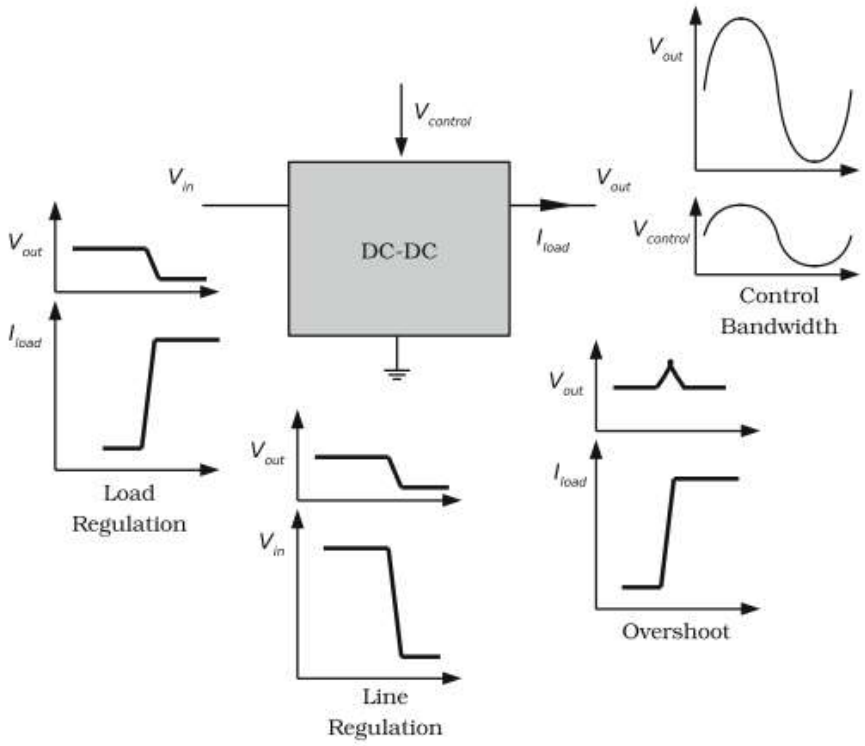
2.1.1 LINE REGULATION

Line regulation indicate the potential of the DC-DC converter to handle the variation in the input voltage (V_{IN2}-V_{IN1}). The percentage representing the line regulation in equation (2.1), is determined by measuring the difference in the output voltage ($V_{OUT,IN2}$-$V_{OUT,IN1}$) at two distinct input voltage levels and then normalizing this difference relative to the variation in the input voltage (MOHAN; UNDELAND; ROBBINS, 2003).

$$R_{line} = \frac{V_{OUT,IN2} - V_{OUT,IN1}}{V_{IN2} - V_{IN1}} \cdot 100\% \tag{2.1}$$

Line regulation may exhibit non-linearity across the whole input range, hence, the output variation is calculated for the maximum and minimum input voltage (Van

Figure 5 – Key Dynamic Characteristics.



Source: From (Van Breussegem; STEYAERT, 2013).

Breussegem; STEYAERT, 2013).

2.1.2 LOAD REGULATION

The load regulation rather then deals with voltage variation as the line regulation, deals with load current variation. It is determined by measuring the variation between the two specific load currents, denoted as $I_{1/2}$ and normalizing this variation with respect to the load variation, such as in equation (2.2) (ERICKSON; MAKSIMOVIC, 2020).

$$R_{load} = \frac{V_{OUT,I2} - V_{OUT,I1}}{I_2 - I_1}\Omega \tag{2.2}$$

Such as the line regulation the load regulation may exhibit non-linearity, however since it deals with loads, this non-linearity will occur over the whole load range. The output variation is calculated for the maximum and minimum load current (Van Breussegem; STEYAERT, 2013).

2.1.3 BANDWIDTH

The bandwidth refers to the capability of the converter to effectively handle changes in load, input voltage (line voltage), and control signals (ERICKSON; MAKSIMOVIC, 2020). Load-regulation bandwidth represents the highest frequency of load fluctuations

that the converter can handle without impacting other operational requirements. This feature is assessed by subjecting the converter to a load step, in which the load will transition from minimum to full load with predefined rise/fall-time.

Line-regulation bandwidth is defined as the maximum input frequency variation tolerated by the converter. It is a essential characteristic for converter with multiple inputs (Van Breussegem; STEYAERT, 2013).

2.1.4 OVERSHOOT AND UNDERSHOOT

A deviation in the nominal voltage is referred to as an overshoot (positive deviation) or undershoot (negative deviation). This deviation occurs due to a transient in the load-line or in the control loop (MOHAN; UNDELAND; ROBBINS, 2003). it is immportant to specify exactly in which circumstances and operating conditions the overshoot/undershoot occurs (Van Breussegem; STEYAERT, 2013).

2.2 STATIC CHARACTERISTICS

The static characteristics are strongly tied to the inherent properties of the converter stage, being independent of the control method utilized in the DC-DC converter (Van Breussegem; STEYAERT, 2013).

2.2.1 VOLTAGE-CONVERSION RATIO

The Voltage-Conversion Ratio (VCR) is defined as the relationship between the output voltage (V_{OUT}) and the input voltage (V_{IN}), as shown in equation 2.3 (MOHAN; UNDELAND; ROBBINS, 2003).

$$VCR = \frac{V_{OUT}}{V_{IN}} \tag{2.3}$$

A DC-DC converter is classified based on its VCR value. If the VCR is greater than one, the converter is referred to as an up converter, as described in equation 2.4.

$$VCR > 1 => V_{OUT} > V_{IN} \tag{2.4}$$

Conversely, when the VCR is less than one, it is known as a down converter (or buck type), as indicated in equation 2.5.

$$VCR < 1 => V_{OUT} < V_{IN} \tag{2.5}$$

In the case of a negative VCR, the converter falls into the category of inverter types, as shown in equation 2.6 and 2.7, where the output voltage is of opposite bias compared to the input voltage.

$$VCR(negative) = V_{OUT}(negative) => V_{IN}(positive) \tag{2.6}$$

$$VCR(negative) = V_{OUT}(positive) => V_{IN}(negative) \tag{2.7}$$

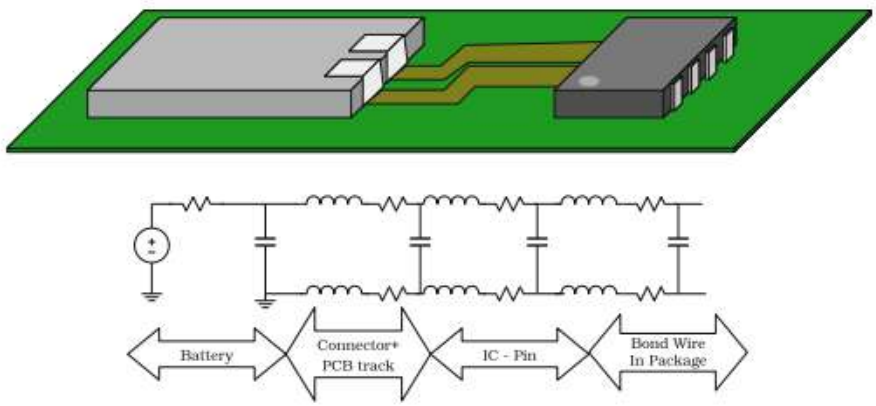
While many DC-DC converters offer a wide range of VCR values simpler types are typically limited to either up or down conversion (Van Breussegem; STEYAERT, 2013).

2.2.2 NOISE

In a DC-DC converter, noise (ripple) is generated due to the combined effect of a non-zero impedance and a varying (switched) current (ERICKSON; MAKSIMOVIC, 2020). To reduce the output impedance, a large output capacitor is connected, resulting in a decrease in noise levels. However, while it's true that the capacitors can help reduce the noise, they also impact the control bandwidth and increase the bill of materials.

In an ideal scenario, a well-regulated power supply should deliver a clean DC voltage without any interference, regardless of the load current. In a realistic scenario, most voltage sources come with their own inherent, sometimes variable, output impedance. Moreover every physical component introduced into the connection between the voltage source and the load, as show in Figure 6, introduces an additional parasitic component to the final output impedance (Van Breussegem; STEYAERT, 2013).

Figure 6 – Physical Connection Model Between the Voltage Source and the Load.



Source: From (Van Breussegem; STEYAERT, 2013).

2.2.3 EFFICIENCY

The efficiency η of a DC-DC converter is its most critical feature. It represents the ratio of the converter's output power (P_{OUT}) to its input power (P_{IN}) (RASHID, 2018). The disparity between input and output power results in power loss (P_{loss}). The efficiency can be calculated using the equation 2.8 which can be also represented as equation 2.9.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{2.8}$$

$$\eta = \frac{P_{OUT}}{P_{loss} + P_{OUT}} \tag{2.9}$$

In an ideal situation, where no power loss occurs, the efficiency would reach 100% under all conditions. However, when real components are used in a DC-DC converter, these components introduce resistive losses, converting electrical power into heat. Various other sources of power loss exist in practical DC-DC converters (Van Breussegem; STEYAERT, 2013), (ERICKSON; MAKSIMOVIC, 2020).

2.2.4 POWER DENSITY

Power density (PD) represents the output power of a standard DC-DC converter concerning the area necessary for the conversion process, as described by equation 2.10.

$$PD = \frac{P_{OUT}}{A} \tag{2.10}$$

Power density is applicable primarily for the calculation of planar implementations of DC-DC converters that are monolithically integrated. For converters implemented with discrete components, it is essential to account for the occupied volume in order to enable accurate assessments (Van Breussegem; STEYAERT, 2013).

2.2.5 EFFICIENCY ENHANCEMENT FACTOR

Not too long ago, the DC-DC converters evaluation was largely based on their power density of efficiency rating as the primary measures of their performance or quality. However, efficiency rating is an insufficient measure especially for step down converter (RASHID, 2018). There is no significant relatioship between the efficiency and the reduction in power loss of the converter. The efficiency should be normalized in accordance to the conversion factor. A down-conversion DC-DC converter can be effectively benchmarked against the most basic down-converter, namely the linear regulator (Van Breussegem; STEYAERT, 2013).

2.2.6 ACCURACY

Ensuring that the DC-DC converter maintains external controllability and closely tracks the control signal under all conditions is highly desirable. This precision can be represented in various manners, with the simplest approach being as equation 2.11.

$$e_{control} = \frac{V_{OUT}}{k_{control} V_{control}} \cdot 100\% \tag{2.11}$$

In the equation 2.11, $e_{control}$ represents the percentage error of the output voltage with respect to the control voltage. It's important to consider that $k_{control}$ is a scaling factor that depends on the method used for sensing the output voltage.

2.3 CAPACITIVE CONVERSION

This type of DC-DC converter operates by means of the capacitive conversion method. This method utilizes only capacitors and switches to perform the voltage conversion (BAKER, 2019).

Capacitive conversion operates based on the energy-storage properties of capacitor, known as capacitance (C). Capacitors are passive electrical components, they store energy in the form of a charge on two conductors separated by an insulating material, by means of an electric field ($\overrightarrow{E}$). According to the equation 2.12, the capacitance occurs when a potential voltage is applied across the plates, a positive charge (Q_+) is placed on one plate and a negative one (Q_-) in the other plate (Van Breussegem; STEYAERT, 2013), (HALLIDAY; RESNICK; WALKER, 2014).

$$C = \frac{Q}{V} \tag{2.12}$$

The capacitance of a capacitor, or any similar arrangement, is influenced by its physical structure and dimensions. In a parallel-plated capacitor as in Figure 7, the capacitance is determined by the permittivity (ϵ) of the insulating material between the plates, the distance (d) separating the plates, and the area (A) of the plates, as indicated by equation 2.13.

$$C_{ParallelPlates} = \frac{\epsilon \cdot A}{d} \tag{2.13}$$

The parallel plate approximation is frequently employed for a wide array of common capacitors and capacitance computations for objects. In instances involving more intricate structures, manual calculations are often overlooked in favor of dedicated tools such as FastCap (Van Breussegem; STEYAERT, 2013).

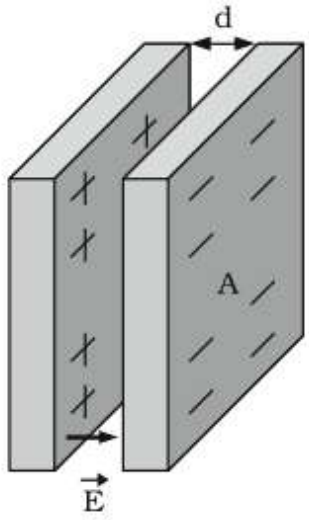
When an electric field is established between the capacitor's plates, and is capable of accelerating charge, the capacitor can perform work, indicating the presence of stored energy. The work (dW) required to transfer an additional charge increment (dq) from one plate to the other is given by equation 2.14.

$$dW = V_{dq} = \frac{q}{C} \cdot dq \tag{2.14}$$

The overall work required to raise the charge from zero to Q can be found in equation 2.15.

$$W = \int_0^Q \frac{q}{C} \cdot dq = \frac{Q^2}{2 \cdot C} = \frac{C \cdot V^2}{2} \tag{2.15}$$

Figure 7 – Representation of a parallel plate capacitor.



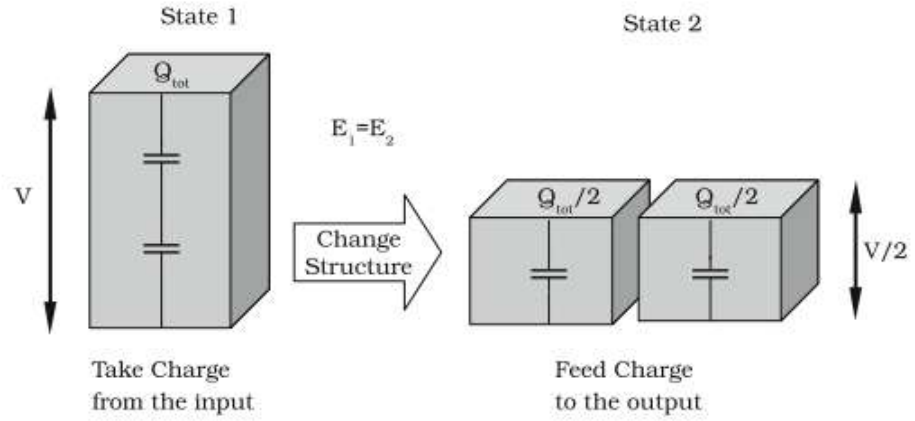
Source: From (Van Breussegem; STEYAERT, 2013).

A capacitor can't only work by storing energy, it must also have the capability to efficiently transfer energy (Van Breussegem; STEYAERT, 2013), (ERICKSON; MAKSIMOVIC, 2020).

2.3.1 ENERGY TRANSFER

A capacitive converter operates by utilizing capacitors to transfer charge from the input to the output of the converter. Although the total charge is conserved, the mechanism of energy storage is altered, as depicted in Figure 8. Despite the principle of energy conservation, an observed shift in voltage across the structure suggests that a capacitor arrangement can effectively achieve voltage conversion (Van Breussegem; STEYAERT, 2013).

Figure 8 – Capacitive conversion from a charge view point.

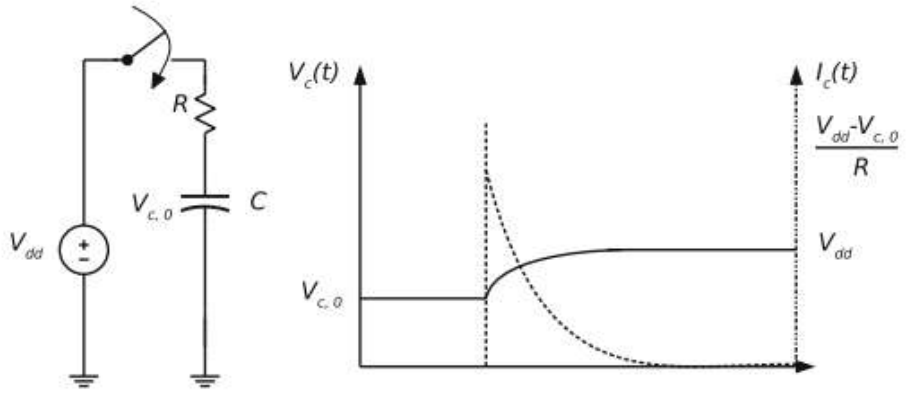


Source: From (Van Breussegem; STEYAERT, 2013).

In a practical capacitive DC–DC converter, energy is efficiently transferred from the input supply to the load through the utilization of capacitors. The charging dynamics of a capacitor can be seen in Figure 9 and are characterized by the following differential equation 2.16 (NILSSON; RIEDEL, 2015).

$$-V_{dd} + RC \cdot \frac{dV_C}{dt} + V_C = 0 \tag{2.16}$$

Figure 9 – Charging of a capacitor.



Source: From (Van Breussegem; STEYAERT, 2013).

Upon solving for $V_C(t)$ and deriving the capacitor current, $I_C(t)$, the equation 2.17 and 2.18 are obtained.

$$V_C(t) = V_{dd} - (V_{dd} - V_{C,0}) \cdot e^{\frac{-t}{RC}} \tag{2.17}$$

$$I_C(t) = \frac{V_{dd} - V_{C,0}}{R} \cdot e^{\frac{-t}{RC}} \tag{2.18}$$

Using the equations 2.17 and 2.18, the power trasferred to the capacitor can be obtained using the equation 2.19 and the energy added to the capacitor can be found using the equation 2.20.

$$P_C(t) = V_C(t) \cdot I_C(t) = \frac{V_{C,0} \cdot V_{dd} - V_{C,0}^2}{R} \cdot e^{\frac{-t}{RC}} \tag{2.19}$$

$$E_C = \int_0^\infty P(t)dt = \frac{V_{dd}^2 - V_{C,0}^2}{2} \cdot C \tag{2.20}$$

The total energy provided by the supply voltage source can be calculated by equation 2.21.

$$E_{tot} = V_{dd}(V_{dd} - V_{C,0}) \cdot C \tag{2.21}$$

The total energy delivered by the power supply is greater because some power is lost as a result of resistive losses in the resistor (denoted as R). Consequently, a

portion of the energy is dissipated as heat (BAKER, 2019). This loss is quantified by the charging efficiency, denoted as $\eta_{C,Charge}$, as can be seen in equation 2.22. Charging efficiency represents the ratio of the actual energy stored in the capacitor to the energy that could ideally be stored if there were no losses. In other words, it measures how effectively the system converts the supplied energy into stored energy in the capacitor, taking into account the losses incurred during the charging process. A higher charging efficiency indicates a more effective energy transfer and storage process.

$$\eta_{C,Charge} = \frac{E_C}{E_{tot}} = \frac{1}{2} \cdot \frac{V_{C,0} + V_{dd}}{V_{dd}} \tag{2.22}$$

The efficiency (η) of charging a capacitor is solely determined by the ratio of the initial voltage to the charging voltage. Even in the absence of resistance, power loss still occurs during the charging process. For capacitive converters to function efficiently, it is crucial to minimize the difference between the charging voltage and the initial voltage across the capacitor during operation (Van Breussegem; STEYAERT, 2013).

2.4 INDUCTIVE CONVERSION

Inductors, as passive components, store energy in a magnetic field (represented as $\overrightarrow{B}$), which is generated by flowing currents (HALLIDAY; RESNICK; WALKER, 2014). Constructed by winding a conductor around a core with optimal permeability, inductors leverage their inductance (L) to store energy in the magnetic field. This inductance enables the calculation using equation 2.23 of the voltage across the inductor (V_L) by considering the instantaneous change in current (I) passing through the inductor.

$$V_L = L \cdot \frac{dI}{dt} \tag{2.23}$$

Enabling a current to flow through an inductor requires external work, with the work performed aligning with the energy stored in the inductor. This power can be expressed using the equation 2.24

$$\frac{dW}{dt} = I \cdot V_L \tag{2.24}$$

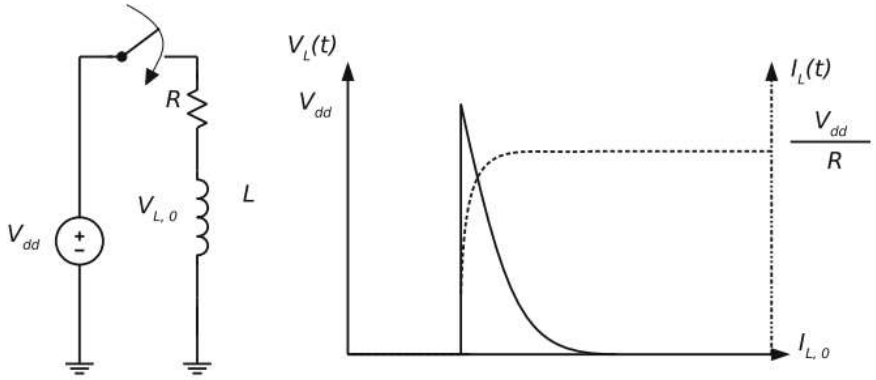
$$W = \frac{L \cdot I^2}{2} \tag{2.25}$$

The equation 2.25 is found by substituting equation 2.23 in equation 2.24 and integrating from the initial time until the current attains a magnitude of I yields the expression for the energy stored within the inductor (Van Breussegem; STEYAERT, 2013)

2.4.1 ENERGY TRANSFER

Inductive converters (such as Buck, Boost, and Cuk converters) utilize an inductor to enable the efficient transfer of energy from the input to the output (ERICKSON; MAKSIMOVIC, 2020). Instead of delving extensively into various topologies and the associated equations, let's center our attention on the fundamental process of storing energy in an inductor. In Figure 10, the illustration captures the current and voltage dynamics within and across the inductor when the switch is closed. This clear depiction promptly unveils the essential characteristics of harnessing an inductor in a switched-mode inductive converter (Van Breussegem; STEYAERT, 2013).

Figure 10 – Charging Current to Energize the Inductor.



Source: From (Van Breussegem; STEYAERT, 2013).

The energy transfer process can be analyzed using a simple R-L circuit model, where R represents the parasitic resistance of the inductor winding and the closed switch. The diferential equation 2.26 describes this circuit dynamics (NILSSON; RIEDEL, 2015).

$$-V_{dd} + R \cdot I_L + L\frac{dI_L}{dt} = 0 \tag{2.26}$$

The equations 2.27 and 2.28 are found by solving V_L and deriving the current through the inductor ($I_L(t)$).

$$V_L(t) = (V_{dd} - R \cdot I_L(0)) \cdot e^{\frac{-t \cdot R}{L}} \tag{2.27}$$

$$I_L(t) = \frac{V_{dd}}{R} + (I_L(0) - \frac{V_{dd}}{R}) \cdot e^{\frac{-t \cdot R}{L}} \tag{2.28}$$

Equation 2.29 shows the power that is stored in the inductor and equation 2.30 the energy inserted into the inductor (NILSSON; RIEDEL, 2015).

$$p_L = V_L(t) \cdot I_L(t) = \frac{V_{dd}^2}{R} \cdot (e^{\frac{-t \cdot R}{L}} - e^{\frac{-2t \cdot R}{L}}) \tag{2.29}$$

$$E_L = \int_0^{\infty} P_L(t)dt = \frac{L \cdot V_{dd}^2}{2 \cdot R^2} \tag{2.30}$$

The charging efficiency calculation is omitted, but it can be demonstrated that η can reach 100% irrespective of the boundary conditions when R equals zero. However, if R is non-zero, refer to equation 2.30; the maximum energy that can be stored is limited by the series resistance of the inductor (Van Breussegem; STEYAERT, 2013).

2.5 ANALYSIS

In exploring energy storage and transfer through capacitors and inductors, this study delves into their distinctive characteristics (ERICKSON; MAKSIMOVIC, 2020). Inductive conversion involves a continuous current flow with permanent resistive losses, and the controlled increase in inductor current is addressed, emphasizing the need to cease the process when nearing maximum energy content, as indicated by equation 2.30. Conversely, capacitive conversion relies on capacitors, with resistors playing a diminished role when the circuit's time constant exceeds the observed time period. Charging efficiency is examined, specifically the impact of the charging voltage-to-initial voltage ratio as shown in equation 2.22 (BAKER, 2019). As seen beforehand to obtain energy transfer as high as possible, is required a large capacitor for a capacitive DC-DC converter or a large inductor with a small series resistance for an inductive DC-DC converter (Van Breussegem; STEYAERT, 2013).

This discussion delves into the fundamental characteristics of various DC–DC conversion techniques, emphasizing a theoretical perspective that does not delve into practical implementation nuances. Nevertheless, this analysis elucidates the foundational bottlenecks inherent in both approaches. Inductive-type DC–DC converters emerge as an attractive option when equipped with low-resistance inductors, characterized by a high-quality factor (Q). In contrast, capacitive-type DC–DC converters become a viable alternative in production technologies featuring capacitors with high capacitance density. While acknowledging the elementary nature of this discussion, it lays the groundwork for understanding the essential considerations influencing the choice between inductive and capacitive DC–DC conversion techniques (Van Breussegem; STEYAERT, 2013).

2.6 STATE-OF-THE-ART INTEGRATED CONVERTERS

The miniaturization of power supplies, is a key requirement for modern portable and Internet of Things (IoT) devices, can be cansidered from two distict perspectives (BAKER, 2019). The PowerSIP that follows a System-in-Package (SIP) strategy where maximum functionality is consolidated onto a single Integrated Circuit (IC), with the passives packaged alongside the IC. This approach often uses standard silicon thecnology

for the IC specialized packaging for the passives, offering a balance between size and efficiency (ERICKSON; MAKSIMOVIC, 2020).

The PowerSoC approach strives for a fully integrated System-on-Chip (SoC) design. This method aims to encompass all elements - control functionality, power switches, and the passive components - onto a single silicon die. While challenges related to integrating high-quality inductors and large capacitors directly into the standard CMOS process, which often limits the overall efficiency and power handling capability (Van Breussegem; STEYAERT, 2013).

2.6.1 INDUCTIVE CONVERTERS

The initial stage of integrating DC-DC converters involves the development from converters built entirely from discrete components to incorporating the control circuit and power switches on the same Integrated Circuit (IC) (ERICKSON; MAKSIMOVIC, 2020). For inductive converters, the primary challenge in full integration (PowerSoC) remains the need for a external, off-chip inductor with a high quality factor (Q) to achieve acceptable efficiency. While some low-power approaches utilize on-chip inductors, these typically result in lower efficiency and power density compared to using a discrete inductor, leading most higi-performance inductive solutions to follow the System-in-Package (SiP) approach (BAKER, 2019).

2.6.2 CAPACITIVE CONVERTERS

Capacitive DC-DC converter traditionally requires higher numbers of components in comparison to the inductive converter (Van Breussegem; STEYAERT, 2013). The capacitive DC-DC converter can be divided in two types. The discrete capacitors where it uses a small number of capacitors, however it is necessary to use external components. Fully-integrated Capacitive Converters don't require external components, but it necessary a great number of capacitors to achieve the desired results (Van Breussegem; STEYAERT, 2013).

2.7 CONVERTER TOPOLOGIES AND FUNDAMENTALS

DC-DC converters that use capacitors are fundamentally different from inductive DC-DC converters. The most significant difference between the capacitive and the inductive converters lies in the conditions requierd for achieving lossless conversion (ERICKSON; MAKSIMOVIC, 2020).

For capacitive converters (Switched-Capacitor Converters), achieving truly lossless conversion is theoretically possible only at infinitely high switching frequencies (to minimize voltage differentce during charge transfer) or by a converter possessing an infinetely large capacitance (to minimize ripple and impedance). however, a well-designed capacitive

DC-DC converter encounters minimal efficiency drawbacks for reasonable deviations from these theoretical stipulations (PALUMBO; PAPPALARDO, 2010).

In contrast, inductive converters have inherent resistive losses due to winding resistance (ESR) of the inductor and the on-resistance ($R_{DS,on}$) of the switches, making 100% efficiency imposible in any real-world operation (RASHID, 2018). These distinct loss mechanisms fundamentally separate the design principles of the two converters types (Van Breussegem; STEYAERT, 2013).

2.8 DC-DC CONVERTER STRUCTURE

The capacitive DC-DC converters are composed of two main parts: the conversion block and the control block. The conversion blcok is the most important part of the converter, as it performs the voltage conversion between the DC input voltage and the DC output voltage. The control block is a signal processing system that manipulates the behavior of the conversion block to maintain alignment with the system requirements (ERICKSON; MAKSIMOVIC, 2020).

The conversion block conversion block constitues the power stage and deals with the low impedance part of the DC-DC converter, handling the high power flow. Conversely, the control part utilizes a high impedance feedback path that senses the output voltage characteristic in relation to a minimum of one control parameter (e.g., switching frequency or duty cycle) of the conversion block (Van Breussegem; STEYAERT, 2013).

2.8.1 PRINCIPLES

The DC-DC converter is also know as a Variable Structure System (VSS). The VSS operation is marked by repetitive change in the circuit's structure which is implemented by the controlled switching action (RASHID, 2018). The DC-DC capacitive converters utilize only switches and capacitors to transfer charge between input and output. The capacitors consists of two types of capacitors being the flying capacitor (C_{fly}) and the output buffer capacitor (C_{OUT}) (Van Breussegem; STEYAERT, 2013).

The flying capacitors work as the charge-transferring capacitors, the buffer capacitor (C_{OUT}), however, doesn't interfere in the charge transfer mechanism but primarily affects the star-up behavior of the converter, it also influences the steady-state noise (ripple) characteristics by filtering the output voltage (Van Breussegem; STEYAERT, 2013).

Every topology of a converter has an ideal VCR (iVCR), which is the maximum ratio between the output voltage and the input voltage of the conversion block. The iVCR is the upper limit for the VCR, theoretically, the converter can operate at 100% of it efficiency when this VCR limit is reached. The VCR is defined by the equation 2.3 show in section (1.1.2.1) (Van Breussegem; STEYAERT, 2013), (PALUMBO; PAPPALARDO,

2010).

2.8.2 SERIES-PARALLEL HALF CONVERTER

This type of converter is built using one flying capacitor (C_{fly}) and one output buffer capacitor (C_{OUT}). Due to a periodic change in the converter structure, the terminals of the flying capacitor suffer a notable change in potential, acting as the charge-transfer element (PALUMBO; PAPPALARDO, 2010). The output buffer capacitor, however, does not take part directly in the charge tranfer but plays a crucial role in reducing the switching noise originated from the switching nature of the converter (BAKER, 2019).

The series-parallel half converter works by alternating between two-state operation, often termed ϕ_1 and ϕ_2. This structure typically achieves a Voltage Conversion Ratio (VCR) of 1/2 or 2, making it a basic fractional converter (Van Breussegem; STEYAERT, 2013). the operation of the switches (S_1 through S_4) during two phases is defined by the logic states as show in equations 2.31, and 2.32.

$$\phi_1 = S_1 = S_2 = 1, S_3 = S_4 = 0 \tag{2.31}$$

$$\phi_2 = S_1 = S_2 = 0, S_3 = S_4 = 1 \tag{2.32}$$

2.9 ANALYSIS TECHNIQUES

In the design and modeling of Switched-Capacitor Converters, the precise calculation of parameters like output impedance and efficiency requires specialized mathematical approches. The Charge Flow Analysis techniques characteristics an in-depth understanding of the Output Impedance Model and the voltage characteristics (ERICKSON; MAKSIMOVIC, 2020). these methods allow designer to accurately predict the steady-state and transient performance of the converters, especially crucial in integrated solutions (Van Breussegem; STEYAERT, 2013).

2.9.1 CHARGE FLOW ANALYSIS

The Charge Flow Analyis is an essential tool for identifying the role of each component in the conversion block. Using this analysis, the charge flow vectors (a_c^i) are extracted. These vectors serve to qualify the performance of the capacitive converter, enabling an objective comparison of diferent converter topologies (PALUMBO; PAPPALARDO, 2010).

The chage that flows through the capacitors during the first phase (ϕ_1) and the sedonf phase (ϕ_2) of the switching period is described by the equations 2.33 and 2.34, where q_{out}, q_{in}, and q_i represent the charge flow elements related to the output, input and n flying capacitors respectively (Van Breussegem; STEYAERT, 2013).

$$a_c^1 = \frac{q_{out}^1 q_1^1 q_n^1 q_{in}^1}{q_{out}} \tag{2.33}$$

$$a_c^2 = \frac{q_{out}^2 q_1^2 \cdots q_n^2 q_{in}^2}{q_{out}} \tag{2.34}$$

The determination of charge vector elements involves applying fundamental principles to each state of the conversion period. Kirchhoff's current law is employed in each node, asserting that the sum of charge flow elements equals zero within each circuit node. In steady state, the sum of charge flow elements for every component is zero (ERICKSON; MAKSIMOVIC, 2020). Additionally, the output capacitor C_{out}, being significantly larger than the flying capacitors, operates as a voltage source in relation to the rest of the circuit, assuming no voltage ripple at the output node. These principles guide the systematic determination of charge vector elements, providing a comprehensive understanding of the charge dynamics in the converter circuit (Van Breussegem; STEYAERT, 2013).

2.9.2 CHARGE BALANCE ANALYSIS

Charge Balance Analysis focuses on the absolute amount of charge within the circuit, distinguishing it from Charge Flow Analysis, which revolves around the alteration of charge on the components. In contrast to the quantity Q_x used in Charge Balance Analysis, Charge Flow Analysis utilizes q_x, both measured in Coulombs. However, q_x represents a change in Q_x over a specific time interval Δ_t=t_1-t_0, this can be observed in equation 2.35 (ERICKSON; MAKSIMOVIC, 2020). This distinction clarifies the complementary roles of these analyses in understanding different aspects of the charge dynamics in the circuit (Van Breussegem; STEYAERT, 2013).

$$q_x = Q_{x,t=t1} - Q_{x,t=to} \tag{2.35}$$

In a steady state, the conservation of charge across both states of the switching period ensures a constant output voltage, as expressed in equation 2.36, where $\Sigma Q_{c,i}^{(1)}$ is the total charge on all flying capacitors during state 1, and so on.

$$\Sigma Q_{c,i}^{(1)} = Q_{out}^{(2)} + \Sigma Q_{c,i}^{(2)} \tag{2.36}$$

The calculation of charge stored on capacitors, including the output capacitor, relies on the voltage-capacitance-charge relationship (Q=C· V). The charge dissipated in the load is determined by Ohm's law, resulting in the charge conservation equation 2.37 (Van Breussegem; STEYAERT, 2013), (PALUMBO; PAPPALARDO, 2010).

$$C_{fly} \cdot (V_i[n-1] - V_{out}[n-1]) + C_{out} \cdot V_{out}[n-1] = \frac{V_{out}[n]}{2 \cdot R_{load} \cdot f_{sw}} + C_{fly} \cdot V_{out}[n] + C_{out} \cdot V_{out}[n] \tag{2.37}$$

This discrete-time equation is then transformed into the circuit's transfer function (TF) using the Z-transform (NILSSON; RIEDEL, 2015), given by equation 2.38.

$$\frac{V_{out}}{V_{in}} = \frac{C_{fly} \cdot Z^{-1}}{(C_{fly} + C_{out} + \frac{1}{2 \cdot R_{load} \cdot f_{sw}}) - (-C_{fly} + C_{out}) \cdot Z^{-1}} \tag{2.38}$$

The transfer function reveals the input-output voltage relationships in terms of switching frequency (f_{sw}), capacitor sizes (C_{out}, C_{fly}), and the load (R_{load}). Analyzing the unloaded case ($R_{load}=\infty$) and the case with no AC variation (Z=1) yields specific insight, as presented in equations 2.39 and 2.40 (Van Breussegem; STEYAERT, 2013).

$$\frac{V_{out}}{V_{in}} = \frac{C_{fly}}{(C_{fly} + C_{out}) - (C_{out} - C_{fly})} \tag{2.39}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{(2 + \frac{1}{2 \cdot C_{fly} \cdot R_{load} \cdot f_{sw}})} \tag{2.40}$$

The simplified input-output relationship in equation 2.41 further highlights the constant gain factor and load-dependent gain factor, resembling the gain of a resistive divider. This analysis suggests that a capacitive converter is characterized by a conversion ratio (N) and an output impedance, aligning with solutions from the Charge Balance Method applied to other topologies (Van Breussegem; STEYAERT, 2013), (ERICKSON; MAKSIMOVIC, 2020).

$$V_{out} = \frac{1}{2} \cdot V_{in} \cdot \frac{R_{load}}{(R_{load} + \frac{1}{4 \cdot C_{fly}} \cdot f_{sw})} \tag{2.41}$$

2.9.3 BRANCH ANALYSIS

The Charge Balance Analysis is an effective technique for analyzing a capacitive conversion block. However, for complex converter topologies, it can become an exhaustive method. To address this, the Branch Analysis, based on Tellegen's theorem, has been developed to determine the output impedance (MAKOWSKI; MAKSIMOVIC, 1995). The Branch Analysis utilizes two approximations of the output impedance: the Slow Switching Approximation, which considers only the effect of the switched-capacitor nature of the converter, and the Fast Switching Approximation, which focuses solely on the resistive nature of the converter (Van Breussegem; STEYAERT, 2013).

The Slow Switching Approximation, based on Charge Balance analysis, proposes modeling a capacitive converter as a voltage-dependent voltage source (or a DC transformer) with a non-zero output impedance. To determine this output impedance, a straightforward technique involves applying a test source at the output terminals and short-circuiting the input. Tellegen's theorem suggests that, for each state, the charge balance vectors are orthogonal to the voltages across the components. Combining both states yields the

equality show in equation 2.42 (Van Breussegem; STEYAERT, 2013), (MAKOWSKI; MAKSIMOVIC, 1995).

$$v_{out} \cdot (a_{out}^{(1)} + a_{out}^{(2)}) + \Sigma_{i=1}^{n}(a_{c,i}^{(1)} v_{c,i}^{(1)} + a_{c,i}^{(2)} v_{c,i}^{(2)}) = 0 \tag{2.42}$$

Simplifications, assuming $a_{out}^{(1)}+a_{out}^{(2)}=1$ and introducing $a_{c,i}=a_{c,i}^{(1)}=-a_{c,i}^{(2)}$ and $q_i=a_{c,i}q_{out}$. In equation 2.43 is show the simplification (Van Breussegem; STEYAERT, 2013).

$$v_{out}q_{out} + \Sigma_{i=1}^{n}(q_i \Delta_{vi}) = 0 \tag{2.43}$$

Assuming linear capacitor behavior $\Delta\ v_i=\frac{q_i}{C_i}$, dividing the equation 2.43 by q_{out}^2 result in equation 2.44 (Van Breussegem; STEYAERT, 2013), (PALUMBO; PAPPALARDO, 2010).

$$\frac{v_{out}}{q_{out}} - \Sigma_{i=1}^{n}(\frac{q_i}{q_{out}})^2 \cdot \frac{1}{f_{sw} \cdot C_i} \tag{2.44}$$

Defining $a_{c,i}=\frac{q_i}{q_{out}}$, the output impedance ($R_{SSL}$) is expressed in equation 2.45. It's crucial to note that this derivation ignores the influence of parasitic resistors in the circuit, making the output impedance valid under the assumption of negligible resistance impact (Van Breussegem; STEYAERT, 2013).

$$R_{SSL} = \Sigma_{i=1}^{n} \frac{a_{c,i}^2}{f_{sw} C_i} \tag{2.45}$$

The Fast Switching Approximation addresses scenarios where parasitic resistance cannot be ignored, and power loss due to these resistances is dominant (ERICKSON; MAKSIMOVIC, 2020). This approach involves determining a set of switch charge flow vectors using the methodology proposed in Charge Flow Analysis. Two switch charge vectors correspond to each state of the converter, with each element $a_{r,i}$ corresponding to the charge flow through a switch S_r (Van Breussegem; STEYAERT, 2013).

The average current through the switches is given by equation 2.46.

$$i_{r,i} = \frac{q_{r,i} \cdot f_{sw}}{D} \tag{2.46}$$

Considering $q_{r,i}=a_{r,i}q_{out}$, and $q_{out}=\frac{i_{out}}{f_{sw}}$, and assuming an optimal charge flow with duty cycle D=0.5 the equation 2.47 is considered in to formulate the equation 2.48.

$$i_{r,i} = 2a_{r,i} i_{out} \tag{2.47}$$

$$P_{loss,switches} = \Sigma(\frac{1}{2} R_i (2a_{r,i} i_{out})^2) \tag{2.48}$$

Thus, the output impedance is found using the equation 2.49.

$$R_{FSL} = 2\Sigma_i R_i a_{r,i}^2 \tag{2.49}$$

This approach results in a dual interpretation of a capacitive DC–DC converter's output impedance. One interpretation considers the capacitive nature, ignoring resistance, while the other considers the resistive nature, ignoring the switched capacitor nature. Both interpretations are unified by recognizing both natures as complementary (MAKOWSKI; MAKSIMOVIC, 1995). The total output impedance is accurately approximated using the equation 2.50 (Van Breussegem; STEYAERT, 2013).

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.50}$$

2.10 TAXONOMY

The topology of a capacitive DC–DC converter represents the spatial properties of the converter, detailing the structure and interconnection of its components. This can be conveyed through literal descriptions, such as a netlist, or graphical means, such as a schematic drawing. Given that capacitive converters exhibit variable-structure systems with different states, it is advantageous to represent each state with a separate schematic, as demonstrated in previous sections (Van Breussegem; STEYAERT, 2013).

The preceding analyses demonstrate that each capacitive capacitive converter topology possesses a distinct iVCR (instantaneous Voltage Conversion Ratio). This fundamental property significantly influences the utilization of these converters (PALUMBO; PAPPALARDO, 2010). Firstly, a single topology has an upper bound for the achievable conversion, i.e., the iVCR. Secondly, the efficiency has a corresponding upper bound determined by the ratio of the actual VCR to the iVCR as can be seen in equations 2.51, 2.52 (Van Breussegem; STEYAERT, 2013), (ERICKSON; MAKSIMOVIC, 2020).

$$VCR \leq iVCR \tag{2.51}$$

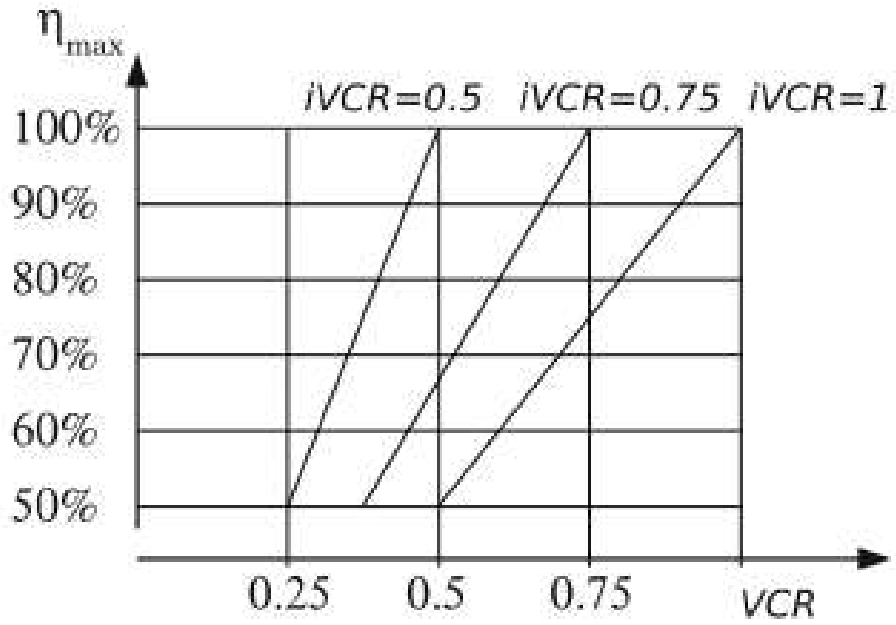
$$\eta_{max} = \frac{VCR}{iVCR} \tag{2.52}$$

This relationship is illustrated in Figure 11, depicting that the maximum attainable efficiency experiences a substantial decrease for deviations from the iVCR. This effect imposes constraints on the input-output voltage range of a capacitive converter topology when achieving high efficiency is a priority. Therefore, the VCR stands out as one of the primary considerations for capacitive DC–DC converters, necessitating the classification of these topologies (Van Breussegem; STEYAERT, 2013).

2.10.1 TOPOLOGY OCCURENCE THEOREM

The existence of various capacitive DC–DC converter topologies is governed by a significant theorem (MAKOWSKI; MAKSIMOVIC, 1995). This theorem predicts the achievable iVCR based on the number of capacitors in the system. For a two-state capacitive

Figure 11 – Maximum efficiency of VCR in three topologies.



Source: From (Van Breussegem; STEYAERT, 2013).

DC–DC converter with n flying capacitors, the flying capacitors can be configured to achieve an ideal VCR N, given by equation 2.53 (Van Breussegem; STEYAERT, 2013).

$$N(n) = \frac{V(n_{out})}{V(n_{in})} = \frac{P[n]}{Q[n]} \tag{2.53}$$

Here, N not only represents the ideal ratio of the output voltage to the input voltage but also corresponds to the ratio between two integer numbers P[n] and Q[n]. These characteristic numbers must satisfy inequalities in equation 2.54 (Van Breussegem; STEYAERT, 2013), (MAKOWSKI; MAKSIMOVIC, 1995).

$$MAX[ABS[P[n]], ABS[Q[n]]] \leq F_n Min[ABS[P[n]], ABS[Q[n]]] \geq 1 \tag{2.54}$$

In these equations, N is the ideal VCR, n is the number of flying capacitors, and F_n is the n-th Fibonacci number. If the number of flying capacitors is restricted to three, the conversion ratios in table 2 can be achieved (Van Breussegem; STEYAERT, 2013).

2.11 UP CONVERTERS

This type of converter have a VCR that is higher than one ($V_{out} > V_{in}$). They are usually applied in applications requiring high voltage generation from a lower supply, such as driving OLED displays, programming non-volatile memories, or as the initial stage in certain power systems (ERICKSON; MAKSIMOVIC, 2020). In the context of

Table 2 – Achievable VCR.

n flying capacitors	N_i
1	$\frac{1}{2}$, 1, 2
2	$\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{2}$, 1, 2, 3
3	$\frac{1}{5}$, $\frac{1}{4}$, $\frac{1}{3}$, $\frac{2}{5}$, $\frac{1}{2}$, $\frac{3}{5}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, 1, $\frac{5}{4}$, $\frac{4}{3}$, $\frac{3}{2}$, $\frac{5}{3}$, 2, $\frac{5}{2}$, 3, 4, 5

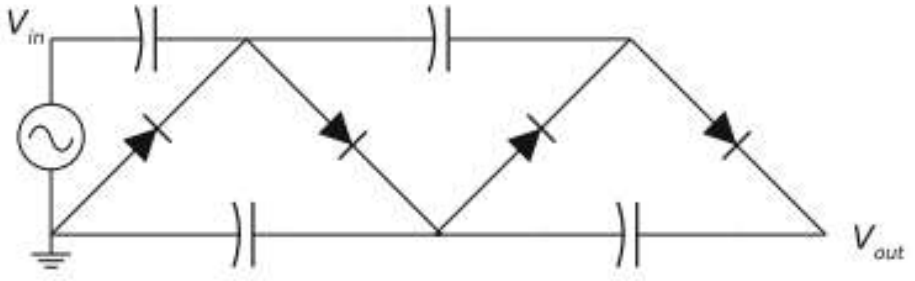
Source: From (Van Breussegem; STEYAERT, 2013).

switched-capacitor converters, these are often reffered to as voltage multipliers or Charge Pumps (Van Breussegem; STEYAERT, 2013).

2.11.1 GREINACHER MULTIPLIER

Invented in 1914 by the Swiss physicist Heinrich Greinacher (PALUMBO; PAPPALARDO, 2010), this converter is, in fact an AC-DC voltage multiplier, however, its fundamental structure was the conceptual basis for the creation of the Dickson DC-DC converter and othher switched-capacitor topologies. The Greinacher multiplier is a converter with a simple build, being required only diodes and capacitors; it does not require switches or active time circuits (Van Breussegem; STEYAERT, 2013). A two-stage Greinacher converter is shown in Figure 12.

Figure 12 – Greinacher topology.



Source: From (Van Breussegem; STEYAERT, 2013).

During the negative half-cycle of the AC input voltage, the upper branch capacitors are charged until the peak input voltage (V_{peak}). During the positive half-cycle, the lower branch capacitors are charged to two times the peak input voltage. The output DC voltage reaches a steady state equal to $2_n V_{peak}(n_{in})$, where n is the number of stages.

The converter is able to generate voltage that are 2_n times higher than the peak input voltage, while the individual components are faced with a voltage that correspond only to twice the peak voltage of the AC input. The system as a whole deals with high output voltages, but the individual components deal with a small fraction of the total high voltage. This crucial concept is known as voltage domain stacking (BAKER, 2019).

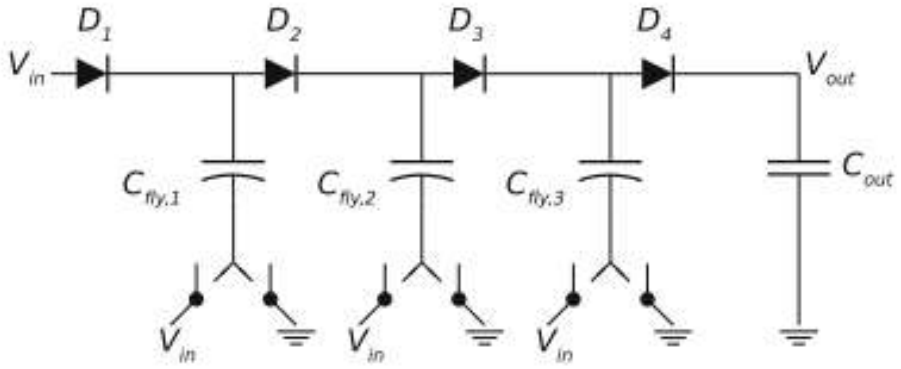
This principle is widely utilized in state-of-the-art DC-DC converters to allow topologies to use components (like MOSFETs) with limited voltage capability by ensuring they are exposed to only a fraction of the total system voltage.

The primary bottleneck of the Greinacher multiplier is that this converter is highly sensitive to the parasitic capacitance caused by the series connection of the capacitors. This problem was effectively circumvented by the subsequent Dickson topology (Van Breussegem; STEYAERT, 2013).

2.11.2 DICKSON CHARGE PUMP

The converter shown in Figure 13, was developed in 1976 to address the need for on-chip high-voltage generation, where the outout voltage must surpass 10 V for effective operation. To erase and write the non-volatile solid-state memory, these high voltages are necessary. It's structure is based on a parallel connection of the capacitor, showing a much lower output impedance and higher resilience to the stray capacitance (Van Breussegem; STEYAERT, 2013).

Figure 13 – Dickson topology.



Source: From (Van Breussegem; STEYAERT, 2013).

A Charge Pump (CP) is an electronic circuit designed to transform the supply voltage V_{DD} into a DC output voltage V_{OUT}, surpassing V_{DD} by several times. Essentially, it functions as a DC-DC converter with a lower input voltage (V_{DD}) and a higher output voltage (V_{OUT}). In contrast to conventional DC-DC converters that utilize inductors, Charge Pumps exclusively consist of capacitors and switches (or diodes) (PALUMBO; PAPPALARDO, 2010).

Charge pump (CP) circuits can function as step-up power converters. In comparison to inductor-based boost power converters, capacitor-based CPs offer advantages such as reduced electromagnetic interference, enhanced self-start-up capability, and a lower count of off-chip components. This makes them particularly well-suited for low-power energy harvesting systems with space constraints. However, it is important to note that

CPs are associated with lower power conversion efficiency (PCE) and diminished driving capability (WANG et al., 2017).

The equation 2.55 shown the output voltage of a unloaded Dickson converter with n stages, n flying capacitors of the same size, having a total flying capacitance C_{fly}, α is the stray capacitance, f_{sw} is the switching frequency, and the I_{LOAD} is the load current (Van Breussegem; STEYAERT, 2013).

$$V_{OUT} = V_{IN} + \frac{n}{1+\alpha} \cdot (V_{IN} - \frac{I_{LOAD}}{f_{sw} C_{fly}}) \tag{2.55}$$

In the first state of operation of the Dickson charge pump, the diodes D_1 and D_3 of the diode string are conducting and transferring charges in the direction of the load through the diode string. In the second stage, diodes D_1 and D_3 are now blocking, while the diodes D_2 and D_4 conduct and transfer the charges. This process is initiated by alternating the bottom plate potential of the flying capacitors using switches (Van Breussegem; STEYAERT, 2013).

2.11.3 PARALLEL-SERIES CONVERTER

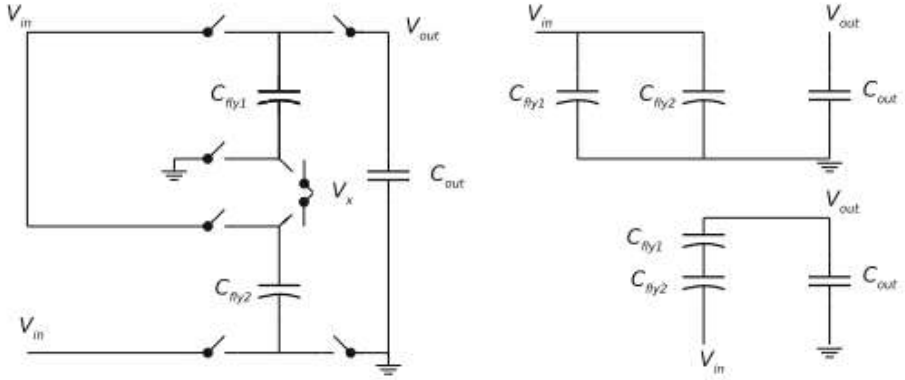
This type of converter depicted in Figure 14, is known for its ability to combine parallel and series configurations in its operation. It is also one of the most direct and fundamental capacitive DC-DC converters (PALUMBO; PAPPALARDO, 2010).

The operation alternates between two phases.

Charging phase (ϕ_1), The flying capacitor(s) (C_{fly}) are charged by the input source (V_{in}) in a parallel configuration.

Discharge/Transfer phase((ϕ_2), The capacitors are discharged in a series configuration, where the energy is transferred to the output node. This discharg occurs effectively between the input and output node (Van Breussegem; STEYAERT, 2013).

Figure 14 – Parallel-series topology.



Source: From (Van Breussegem; STEYAERT, 2013).

The flying capacitors play a crucial role in managing voltage levels and achieving the desired voltage multiplication. The switching operation and the control of the charge and discharge of the flying capacitors must be carefully managed (Van Breussegem; STEYAERT, 2013), (BAKER, 2019).

The parallel-series converter have an ideal voltage multiplication of (n+1), this means that the converter is capable of achieving an output voltage that is (n+1) times the input voltage, when under ideal operating conditions (Van Breussegem; STEYAERT, 2013).

2.12 DOWN CONVERTER

This class of topologies are DC-DC converters that reduce the DC voltage to a lower level ($V_{out} < V_{in}$). This means that the output voltage is lower than the input voltage, a configuration widely used in point-of-load regulation in digital systems. Compared to step-up (boost) converters, the conversion efficiency is usually higher in step-down converters, primarily because the switches and passive components are subjected to lower voltage stresses for a given power level (ERICKSON; MAKSIMOVIC, 2020). For these converters, the ideal Voltage Conversion Ratio (iVCR) is always lower than one (iVCR < 1) (Van Breussegem; STEYAERT, 2013).

2.12.1 SERIES-PARALLEL CONVERTER

The series-parallel converter in Figure 15 function as the inverse of the parallel-series converter, making it a fundamental step-down topology (PALUMBO; PAPPALARDO, 2010). Its operation is defined by two primary states.

Charging phase (ϕ_1), initially, in the first state, the n flying capacitors are connected in a series configuration. They are charged by the input voltage (V_{in}) until each capacitor carries a fraction of the input voltage.

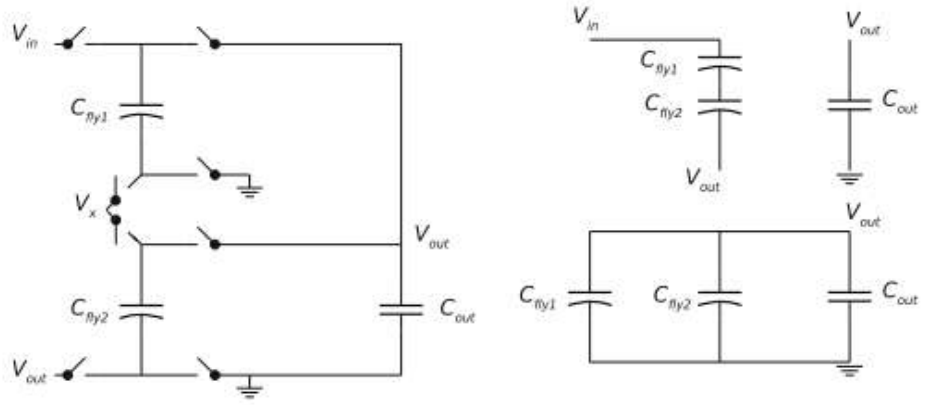
Discharge/Transfer phase((ϕ_2), in the second state, the capacitors assume a parallel configuration and are connected to the output, effectively summing their charges to drive the load.

The series-parallel converter has an ideal Voltage Conversion Ratio (iVCR) of $\frac{1}{(n+1)}$, where n is the number of flying capacitors. This means that the output voltage is $(n + 1)$ times smaller than the input voltage ($V_{out}=\frac{1}{(n+1)}V_{in}$) under ideal operating conditions (Van Breussegem; STEYAERT, 2013).

2.12.2 LADDER CONVERTER

The ladder converter in Figure 16, is comprised of dual series-capacitor arrangements that shift in unison during the process of charging from the power source and discharging toward the load. This converter have a n number of flying capacitors that

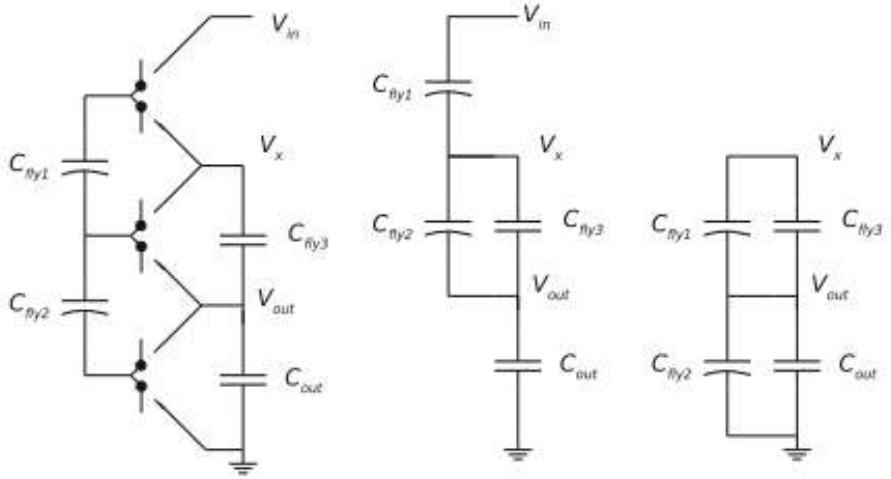
Figure 15 – Series-Parallel topology.



Source: From (Van Breussegem; STEYAERT, 2013).

executes a primary conversion at a ratio of $\frac{2}{(n+3)}$. Each capacitor will reach a voltage of $\frac{(n+3)\cdot V_{in}}{2}$, when charging, in the event of no load being connected (Van Breussegem; STEYAERT, 2013).

Figure 16 – Ladder topology.



Source: From (Van Breussegem; STEYAERT, 2013).

significant advantage of this converter is that the DC voltage can be extracted from multiple nodes, making it an inherently a multiple-output converter . However, when multiple nodes are loaded simultaneously, the total output impedance rises, potentially impacting the converter efficiency adversely if other specifications remain constant (PALUMBO; PAPPALARDO, 2010).

Furthermore, the capacity to support multiple DC nodes allows the implementation of voltage-domain stacking for the internal components, making it appropriate for high-input-voltage implementation where component voltage stress is a concern (BAKER, 2019). However, despite the converter being efficient in managing voltage outputs, its complexity

demands a substantial quantity of switches, leading to a solution heavily reliant on switch components and potentially increasing the total chip area in integrated designs (Van Breussegem; STEYAERT, 2013).

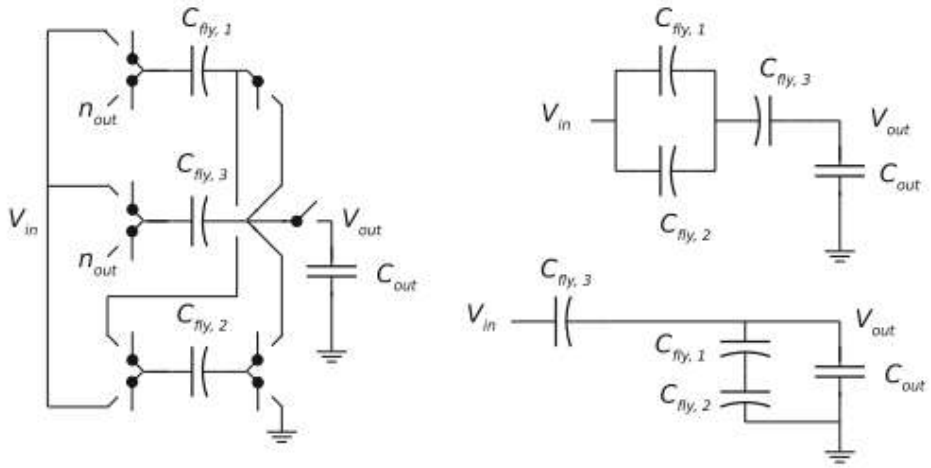
2.12.3 FRACTIONAL CONVERTER

The Fractional Converters present a unique category of converters that differ from the previously outlined types (like integer step-up or $\frac{1}{(n+1)}$ step-down converters). Determining the ideal Voltage Conversion Ratio (iVCR) for these converters often proves challenging when based solely on visual inspection, requiring formal analysis methods like the Branch Analysis (PALUMBO; PAPPALARDO, 2010).

While the existence of this converter type is anticipated by the theorems in (MAKOWSKI; MAKSIMOVIC, 1995) - specifically the Topology Occurrence Theorem—the synthesis process for achieving a specific fractional ratio lacks a standardized, universal methodology. In practice, Fractional Converters span a broad range of conversion ratios, with the constraint of keeping the number of flying capacitors below four (n≤4)due to the rapid increase in output impedance with the number of capacitors.

In Figure 17, it can be observed a $\frac{4}{5}$ fractional converter topology, showcasing the component configuration for both conversion state on the right (Van Breussegem; STEYAERT, 2013). The primary advantage of these converters is their ability to achieve a ratio close to unity (e.g., $\frac{4}{5} = 0.8$) with high efficiency, which is valuable for fine-grained voltage regulation.

Figure 17 – Fractional converter topology.



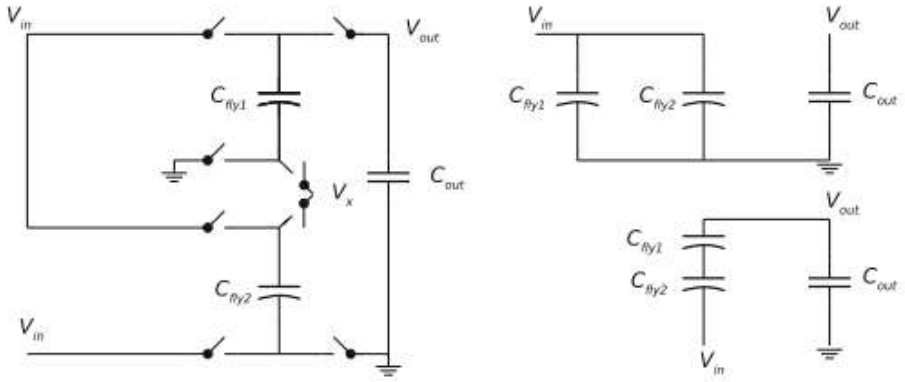
Source: From (Van Breussegem; STEYAERT, 2013).

2.13 MULTI-TOPOLOGY CONVERTER

Multi-topology converters refers to a class of converters that can be configured into various topologies, which allow for multiple operation modes or circuit configurations,

offering flexibility to switch between different topologies. This flexibility is what makes this type of converter highly adaptable to different loads conditions, input sources, and others systems requirements (WANG et al., 2017).

Figure 18 – Multi-Topology.



Source: From (Van Breussegem; STEYAERT, 2013).

The correlation between the converter's topology and its iVCR places restrictions on the converter's ability to handle the input-output variations and affects its performance. To enhance efficiency and adaptability across a broader spectrum of conversion scenarios, there is a clear necessity for capacitive converters with multiple topologies (Van Breussegem; STEYAERT, 2013).

These converters consist of a capacitor-switch array capable of shifting between the two states of the primary topology, as well as transitioning between various alternative topologies. Each of theses topologies is designed to handle a specific segment of the input-output range. The topologies have a maximum VCR that aligns with the iVCR. Alternatively, each topology exhibits reduced performance (lower maximum efficiency η_{max}) when the VCR significantly deviates from the iVCR. However, through the integration of multiple topologies within a single structure and the ability to switch the structure based on the desired VCR, this limitation can be overcome (Van Breussegem; STEYAERT, 2013), (PALUMBO; PAPPALARDO, 2010).

However, through the integration of multiple topologies within a single structure and the ability to dynamically switch the structure based on the desired VCR or efficiency level, this fundamental limitation of fixed-ratio converters can be effectively overcome (Van Breussegem; STEYAERT, 2013).

3 STATE-OF-THE-ART

This chapter provides a comprehensive literature review on the diverse applications of DC-DC converters, encompassing various employed topologies. The initial section offers an overview of the primary applications of DC-DC converters as documented in the literature. The discussion notably emphasizes energy harvesting applications, which aligh closely with the central focus of this work.

Furthermore, the chapter delves into an exploration of state-of-the-art works pertaining to topologies and methodologies employed for achieving multiple voltage conversion ratios, particularly through the use of switched capacitor DC-DC converters.

Within this chapter, an comphensive review is conducted on the latest advancements documented in the literature regarding the applications of energy harvesting, DC-DC converters, and Maximum Power Point Tracking (MPPT). The synthesis of current research and innovative approaches in these domains is presented to offer a comprehensive understanding of the evolving landscape in energy conversion and management.

By assimilating insights from recent works, this chapter aims to contribute to the broader understanding of the applications and technological advancements in the realms of energy harvesting, DC-DC converters, and MPPT techniques.

3.1 DC-DC CONVERTERS FOR ENERGY HARVESTERS

DC-DC converters have emerged as a central point in the state-of-the-art landscape of energy harvesting applications. These converters play a pivotal role in efficiently extracting and managing energy from ambient sources, catering to the increasing demand for sustainable and self-powered systems. Leveraging the principle of energy transfer between different voltage levels, DC-DC converters offer a versatile solution for obtaining multiple voltage conversion ratios. This capability proves particularly advantageous in energy harvesting scenarios where the input voltage varies, requiring adaptive and efficient conversion. The literature abounds with notable works showcasing innovative topologies and approaches employed in DC-DC converters for energy harvesters. Researchers have explored techniques to enhance efficiency, minimize energy losses, and address the unique challenges associated with fluctuating input sources. This chapter delves into the forefront of these advancements, presenting a comprehensive review of the state-of-the-art in DC-DC converters within the context of energy harvesting applications.

In the work (DEVARAJ et al., 2019) is proposed a switched capacitor energy harvester converter topology with multiple inputs, more specifically a photovoltaic and a piezoelectric energy source inputs. The converter is a two-phase reconfigurable charge pump, it consist of a solar charge pump and a piezo charge pump. The solar charge pump initial stage achieves integer conversion ratios of 1, 2, and 3, while the subsequent stage handles fractional conversion ratios of 1/3 and 2/3. Through the integration of both stages, the solar charge pump achieves a comprehensive conversion range spanning from 1/3 to

11/3. The piezo charge pump in a similar fashion provides a total conversion ratio that span from 1/3 to 5/3.

In (CHENG et al., 2020) is proposed a redistributable switched capacitor converter topology for batteryless IoT devices. This converter employs a two-stage charge pump, operating in sleep and active modes, with a total of 16 submodules, and utilizes a multiphase interleaving technique. In the sleep mode, 14 submodules function in a storage state, capturing and storing photovoltaic (PV) energy with maximum power point tracking (MPPT) for the storage capacitor (C_{STO}). Simultaneously, the remaining two submodules operate in a recycling state, delivering a regulated 1.5 V output voltage for the loading circuit. In active mode, all 16 submodules operate in the recycling state to convert V_{STO} to V_{OUT} through the pulse-skip modulation technique (PSM).

(SILVA; SEVERO; GIRARDI, 2020) propose a reconfigurable switched capacitor converter topology having its focus on ultra low power (ULP) devices application that are powered by PV cells in an indoor light environments. The fully integrated conversion system is digitally adjustable, offering 19 distinct voltage conversion ratios (VCRs). Utilizing four Divider/Doubler modules and one Adder/Subtractor module, the system is is capable to to deliver VCRs ranging from 0.25 to 8.

(YOON; CARREON-BAUTISTA; SáNCHEZ-SINENCIO, 2018) describes an energy harvester featuring a reconfigurable capacitor charge pump created using 130 nm CMOS technology. The harvester achieves a 7× step-up in voltage, providing a 1 V output from a low input voltage (TEG $>$ 270 mV) to power IoT applications. By distributing on-chip capacitors to each step-up stage, the design optimizes silicon area and facilitates three-dimensional Maximum Power Point Tracking (3D MPPT). The system dynamically adjusts parameters (N, fsw, and CS,eff) to extract maximum power from a TEG with a small internal impedance ($>$ 1 Ω). Despite its compact size, the harvester delivers up to 500 μW of power, maintaining a regulation of 1 V and achieving an end-to-end peak power efficiency of 64%.

In (CHEN; SU; FAN, 2018) is introduced a high-efficiency, one-stage thermoelectric interface circuit for energy-efficient IoT devices. The design incorporates a capacitive bootstrapping technique (CBT) with a reconfigurable charge pump (CP) to double or triple the output voltage (VOUT), mitigating large on-resistance in the power flow path. For ultralight loads down to 1 μW, a constant on-time (COT) digital pulse-skipping modulation (DPSM) simplifies the controller design and reduces switching losses. The proposed circuit operates efficiently at low input and output voltages, demonstrating enhanced power conversion efficiency. The combination of CBT, a reconfigurable two-stage CP, and an on-demand (OD) strategy minimizes conduction and switching losses over a wide output power range. Employing a low-quiescent-power DPSM controller with a digital zero-current detection (ZCD), the converter achieves a maximum efficiency of 76.4% across an output power range of 1 μW to 500 μW. Notably, the converter maintains over

60% efficiency from 6 μW to 500 μW.

The (JHANG et al., 2020) describes a boost DC-DC converter designed for thermoelectric energy harvesting. The converter features fully built-in startup circuits, eliminating the need for post-fabrication trimming or external components during startup. A novel low-leakage logic gate design and various low-voltage startup techniques are introduced. The measured minimal startup voltage is 82 mV, and the maximum efficiency achieved is 78.55%. The startup procedure involves three steps: initial activation of the startup circuit, gradual voltage increase using a voltage-triggered pulse generator, and transitioning through open-loop and closed-loop states. Voltage detectors monitor the operational states, with power-saving measures in the open-loop state. The closed-loop state employs pulse-frequency modulation for regulation, comparing reference and output voltages to control power MOSFETs and maintain a stable 1.8 V output.

(YANG et al., 2022) introduces a single-inductor triple-mode DC-DC converter designed for energy harvesting in IoT edge nodes. This converter optimally schedules switching sequences to achieve auto-buck-boost operation, ensuring compatibility with a wide input-voltage range. It minimizes the number of switches in a cycle for efficiency and offers a fast load transient response. The design integrates both input and output feedback loops to balance the energy harvester and load requirements. It enables the maximum power point (MPP) tracking of input sources like photovoltaic cells, maintaining harmonious and stable operation. The triple-mode structure enhances overall efficiency and transient response across a wide load range. The proposed converter achieves a maximum output power of 90 mW with a peak efficiency of 88.7% and a rapid load response of less than 450 μs, meeting the power needs of IoT edge nodes.

(CHEN; LIANG; TSAI, 2019) describes a single-cycle SI-DIDO (Solar Input-Dual Inductive Dual Output) DC-DC converter designed to harvest both solar and piezoelectric energy. In one cycle, the converter can efficiently charge a battery and supply power to the load. Photovoltaic (PV) cells are optimized for maximum power point tracking, and a power management system ensures a stable output voltage. The battery serves as an energy reservoir, supplying power when the PV cell output is insufficient and storing excess energy during surplus. The converter incorporates a Zero Current Detection (ZCD) mechanism based on a Delay-Locked Loop (DLL) to establish a consistent timing window before the inductor current reaches zero. This approach minimizes static power consumption and enhances transient response compared to traditional current detectors. The proposed converter achieves a maximum output power of 180 mW, meeting the power requirements for Wireless Sensor Network (WSN) applications, with a peak efficiency of 88.1%.

(JO et al., 2023) presents a boost converter for Thermoelectric Generator (TEG) energy harvesting, featuring a digital Synchronous Timing Zero Current Detector (ST-ZCD). The proposed method employs dead time in Discontinuous Conduction Mode (DCM) to implement time-domain Maximum Power Point Tracking (MPPT) without the

need for additional series switching. This eliminates the requirement for an extra time slot dedicated to MPPT generation, improving efficiency. The digital ST-ZCD operates with high efficiency, unaffected by comparator performance, and consumes low power without using a comparator. The design utilizes a D-flip flop's clock for robust VX node falling edge detection, minimizing the impact of voltage ringing. Fabricated with a 180 nm CMOS process, the chip has a die area of 600 μm $\times$ 475 μm. The measured peak efficiency of the energy harvesting boost converter is 85.5%.

(KUKUNURU; NAEIMI; SALEM, 2023) article presents a series-parallel SPV (Solar Photovoltaic) DC–DC converter with five conversion ratios. This innovative converter replaces capacitors with PV cells to eliminate explicit passive components. By switching PV cells themselves, the converter automatically balances voltage across series-connected cells, addressing mismatch conditions. The converter's voltage balancing capability ensures equal distribution of generated charge, mitigating the impact of mismatches. A proof-of-concept integrated circuit was fabricated in 180 nm technology, demonstrating up to a 30.2% efficiency improvement over prior work, especially under partial shading conditions.

In (ABDELMAGID; HMADA; MOHIELDIN, 2023) introduces a fully-integrated reconfigurable dual-output Thermoelectric Generator (TEG) energy harvesting system. It utilizes a secondary path to adaptively store excess power on a supercapacitor (SC), implement Maximum Power Point Tracking (MPPT), and regulate the primary output. The system dynamically reconfigures its parameters, such as the number of charge pump stages and switching frequencies, through a finite state machine (FSM) to maximize end-to-end efficiency. The dual-output TEG system, implemented in 180 nm CMOS technology, incorporates a secondary path for additional energy storage and output regulation. The FSM optimizes system parameters to maximize the switching frequency of the secondary path, enhancing end-to-end efficiency and achieving MPPT. The system, occupying a total area of 3.24 mm $\times$ 1.525 mm, demonstrated good agreement between theoretical and measured results. It effectively regulates the charge pump output at 1.59 V with a peak-to-peak ripple of 115 mV for a load current change of 100 μA. The measured end-to-end efficiency is 72% at a total output power of 1.24 mW.

The work of (KEE et al., 2023) introduces a CMOS reconfigurable charge pump (CP) for low-voltage energy harvesting, leveraging a series-parallel CP architecture with a novel dynamic source-fed oscillator. The CP adapts its configuration based on input voltage, adjusting the voltage conversion ratio (VCR) to limit the output voltage below 1.8 V. The series-parallel CP architecture optimizes performance, utilizing low effective resistance in parallel CP to enhance power conversion efficiency (PCE). The dynamic source-fed oscillator enables frequency modulation without affecting clock amplitude. Fabricated in 65 nm CMOS, the prototype achieves a peak PCE of 62% within an input voltage range of 0.26 V to 0.64 V. The proposed design outperforms state-of-the-art alternatives, offering a 97% voltage conversion efficiency with lower circuit complexity.

In (LIU et al., 2023) it discusses a novel 0.4 V startup, dead-zone-free, four-mode converter designed for cooperative power supply between energy harvesting devices and a battery. Implemented in a 180 nm standard CMOS process, the converter incorporates a Dead-Zone-Free Four-Mode Control (DZFFC) scheme to address dead-zone issues, ensuring high efficiency in transition regions and favorable Electromagnetic Interference (EMI) characteristics. Adaptive peak and valley current control, along with a reused slope compensation circuit, enhances light-load efficiency. The internal integrated startup scheme, without low-VTH MOSFETs, simplifies realization and enables startup as low as 400 mV in standard CMOS. This feature broadens the input voltage range, making the converter suitable for low-voltage and wide-input scenarios.

In (MARIN et al., 2020) is proposed the implementation and evaluation of a reconfigurable Switched Capacitor Converter (SCC) designed for energy harvesting applications. Implemented in a 28 nm CMOS technology, the prototype demonstrates a compact design with a die area of 3.52 mm^2. The SCC utilizes off-chip ceramic capacitors for energy storage and achieves output voltage regulation through frequency modulation. The efficiency analysis indicates competitive performance across various output currents and a wide input voltage range. The SCC exhibits a quick response to load transients, settling in about 500 ηs. A comparison with state-of-the-art converters highlights the proposed design's flexibility over a broad input voltage range and competitive efficiency.

The realm of energy harvesting applications has witnessed remarkable advancements in the domain of DC-DC converters. These converters, integral to efficiently extracting and managing energy from ambient sources, address the growing demand for sustainable and self-powered systems. By leveraging the principle of energy transfer between different voltage levels, DC-DC converters provide a versatile solution, offering multiple voltage conversion ratios. This adaptability proves particularly advantageous in energy harvesting scenarios with varying input voltages, necessitating adaptive and efficient conversion. The extensive literature review has highlighted innovative topologies and approaches employed in DC-DC converters, showcasing researchers' efforts to enhance efficiency, minimize energy losses, and tackle challenges associated with fluctuating input sources. This chapter provides a comprehensive overview of the state-of-the-art in DC-DC converters, underscoring their pivotal role in the landscape of energy harvesting applications. The DC-DC converters reviewed in this chapter are compared in table 9.

3.2 CHAPTER SUMMARY

This chapter has thoroughly explored the literature of DC-DC converters within the context of energy harvesting applications. The examination has revealed a narrative of progress and innovation, emphasizing the crucial role that these converters play in addressing the surging demand for sustainable and self-powered systems.

The adaptability of DC-DC converters, demonstrated in their capacity to efficiently

Table 3 – Comparison of DC-DC Converter

	Number of VCRs	MPPT	Type	Tech Node	Peak Efficiency	Input Voltage (V)	Output Voltage (V)	Energy Source	Area (mm^2)	Inductor
(DEVARAJ et al., 2019)	11	Yes	Up/Down	65 nm	74.6%	0.55	1.8-2.5	Piezo/Light	0.414	No
(CHENG et al., 2020)	3	Yes	Up	180 nm	91%	0.45-0.9	1.5	Indoor Light	1.69	No
(SILVA; SEVERO; GIRARDI, 2020)	19	No	Up/Down	180 nm	94.26%	0.05-1.6	0.4	Indoor Light	0.282	No
(YOON; PARK; YU, 2018)	6	Yes	Up	130 nm	64%	0.27-1	1	Thermal	0.835	No
(CHEN; SU; FAN, 2018)	1	No	Up	180 nm	76.4%	0.1	0.5-0.6	Thermal	1.3	Yes
(JHANG et al., 2020)	N.R	No	Up	180 nm	78.55%	0.06-0.46	1-1.8	Thermal	0.5292	Yes
(YANG et al., 2022)	9	Yes	Up/Down	180 nm	88.7%	1.2-4	1-4	Light	1.317	Yes
(CHEN; LIANG; TSAI, 2019)	N.R	Yes	Up/Down	180 nm	88.1%	0.5	1.8	Light	10.53	Yes
(JO et al., 2023)	N.R	Yes	Up	180 nm	85.5%	0.2-0.7	1.2	Thermal	0.285	Yes
(KUKUNURU; NAEIMI; SALEM, 2023)	5	Yes	N.R	180 nm	91.3%	N.R	0.5-2.2	Light	0.91	No
(ABDELMAGID; HMADA; MOHIELDIN, 2023)	5	Yes	Up	180 nm	72%	0.35-1	1.6-2.99	Thermal	4.941	No
(KEE et al., 2023)	3	No	Up	65 nm	62%	0.26-0.64	1.8	N.R	0.346	No
(LIU et al., 2023)	4	No	Up/Down	180 nm	90.8%	0.4-3.3	1.8	Light	3.23	Yes
(MARIN et al., 2020)	5	No	Down	28 nm	85%	1.9-6.3	0.9	N.R	3.52	No

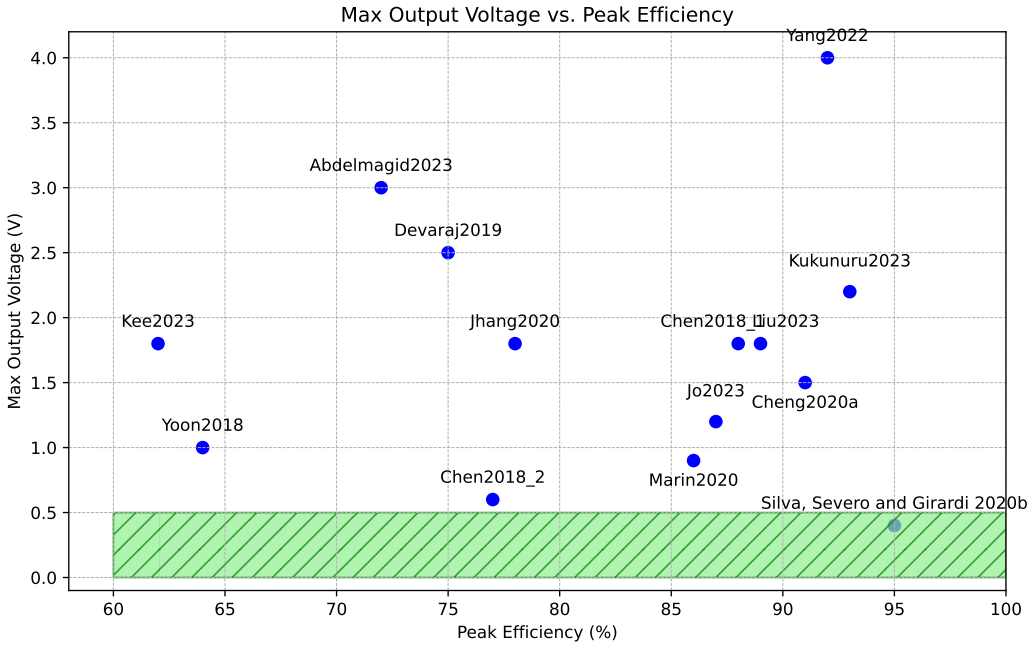
extract and manage energy from ambient sources, highlights their significance in tackling the dynamic challenges of energy harvesting. Their versatility in handling varying input voltages positions them as key enablers in optimizing energy conversion processes.

As evidenced by the comprehensive review of the state-of-the-art literature, researchers have made significant contributions to advancing DC-DC converters. Notable works have introduced innovative topologies and approaches, aiming to enhance technical efficiency and overcome the unique hurdles associated with fluctuating input sources.

The literature review conducted in this chapter serves to underscore the enduring importance of DC-DC converters in shaping the future of energy harvesting. Their role extends beyond technical intricacies; they embody a pathway towards a more sustainable and energy-efficient future.

In Figure 19 illustrates a comparative analysis between the maximum output voltage and peak efficiency. The desired target for achievement is indicated by the region below the green line.

Figure 19 – Comparative analysis between maximum output voltage and peak efficiency.



4 SMALL SIGNAL MODELING AND PARAMETER EXTRACTION METHOD FOR PV CELL INTEGRATION IN INDOOR VLC SYSTEMS

Photovoltaic (PV) cells are being adopted as a viable and cost-effective option for implementing receivers within Visible Light Communication (VLC) systems, primarily in indoor environments. Accurately estimating the generated current and voltage of the PV cell based on incident light is crucial when designing VLC systems.

The primary objective of conducting a AC small signal analysis on the PV cell is to quantitatively determine its high-frequency performance and data transmission capability when subjectc to modulated light. For this assessment, the 1D2R electrical equivalent model, which incorporates a diode and two resistors, is employed.

In AC small signal analysis, the diode is replaced by its dynamic counterpart, which comprises a dynamic resistance in parallel with an equivalent capacitance. This study introduces an approach to measure and characterize the small-signal parameters of a PV cell operating at the maximum power point (MPP), open circuit (OC), and short circuit (SC) bias points. This is achieved through a closed-loop frequency response system, calibrated to encompass illuminance levels ranging from 50 to 500 lux.

The procedure for estimating the AC response of the PV cell is outlined, and the outcomes are subsequently employed in an analytical parameter extraction methodology. Experimental results from a 20 x 40 mm PV cell reveal that MPP represents the least favorable bias point in terms of bandwidth, whereas the SC bias point exhibits the most favorable performance. This observation validates the hypothesis that the optimal bias point for energy harvesting in PV cells is the worst bias point for communication purposes.

4.1 LIGHT AS A POWER SOURCE FOR PV CELLS IN INDOOR VLC SYSTEMS

Light is a commonly used ambient energy source for energy harvesting. Besides being renewable energy, light is abundant in nature and has a very high power density (on the order of 10 $\mu W/cm^2$ indoors and 100 $\mu W/cm^2$ outdoors) (TRAN; CHA; PARK, 2017; DUTRA et al., 2023). Photovoltaic (PV) cells are common transducers used to harvest electrical energy from light, including natural sunlight, lasers, light-emitting diodes (LEDs), and other types of lamps.

Despite the widespread use of solar cells to harness light outdoors, there has recently been a growing interest in using PV cells to harness light indoors to power electronic Internet of Things (IoT) devices (DAS et al., 2021). In addition, PV cells are also suitable as receivers for visible light communication (VLC), which uses visible light to transmit data. This is a very cost-effective wireless method of data transmission because it can share existing lighting infrastructure. It also has advantages in terms of security, as the light signal does not penetrate walls, limiting the reception area. In this context, the light is modulated by an LED through small changes in illuminance

and detected by a photovoltaic cell in the form of voltage or current fluctuations. Other advantages of VLC are its insensitivity to electromagnetic interference and the availability of a large and unregulated band worldwide (DHARANIPRAGADA; LEON-SALAS, 2022). A disadvantage is the communication limiting factor caused by noise, especially in VLC systems that often rely on non-coherent signal detection. In addition, achieving low noise in a receiver circuit usually comes at the cost of increased power consumption (DHARANIPRAGADA; LEON-SALAS, 2022). Another limitation is the low bandwidth offered by a PV cell.

The VLC opens up the possibility of developing new applications for IoT, such as smart agriculture, smart cities, underwater communications, biomedical devices, and others, which has recently led to the introduction of a number of commercial off-the-shelf products that use this technology (CELIK et al., 2023).

In recent years, the trade-off between energy harvesting and data communications has been explored. In the work of (FAKIDIS; HELMERS; HAAS, 2020), an AC-DC separation receiver capable of transmitting lightwave information and energy simultaneously at a data rate of 784 Mb/s and a harvested power of 1 mW using a gallium arsenide (GaAs) vertical-cavity surface emitting laser (VCSEL) was developed. In another work, the feasibility of a communication link with a data rate of 11.84 Mbps with a bit error rate (BER) of $1.6 \cdot 10^{-3}$ was demonstrated for a received optical signal with a peak-to-peak amplitude swing of 4780 lux (WANG et al., 2015).

A good PV cell electrical model is important for the development and simulation of a VLC system, both in DC and AC. Moreover, accurate extraction of model parameters is essential for proper estimation of generated voltage and current as a function of incident light intensity.

The most typical electrical model of a PV cell is the 1D2R, which consists of a diode and two resistors. There are several studies presenting different evaluation methods to extract and estimate the DC parameters of this model (KHURSHEED et al., 2021; BADER; MA; OELMANN, 2019; HAMADANI; CAMPANELLI, 2020), but little is said about the equivalent small-signal AC model, which is of great interest for communication applications.

In this work, we present a technique for measuring and modeling the small-signal parameters of a PV cell in different bias regions using a closed-loop frequency response system. It is calibrated for low illuminance levels and thus provides an accurate model of the PV cell bandwidth for indoor communication purposes. A setup for measuring the PV cell AC response is described and the results are applied to an analytical parameter extraction procedure. In our analysis, we assume that the PV cell has a constant temperature since the goal is to model it for indoor use. However, temperature variations affect both DC and AC behavior and should be considered for outdoor applications, as discussed in (GONTEAN et al., 2018).

The main contribution of this work is the description of an analytical procedure for parameter extraction of the PV cell small signal model under different illuminance and bias conditions.

4.2 PV CELL ELECTRICAL MODEL

The prevalent static electrical model for photovoltaic (PV) cells is referred to as the 1D2R model. It encompasses a diode alongside two resistors, as depicted in Figure 20 (CELIK; ACIKGOZ, 2007). This specific electrical model presents the best trade-off between parameter count and accuracy (ARAÚJO; SOUSA; COSTA, 2020). The resulting output current, denoted as I_{out}, can be determined through circuit analysis, as follows:

$$I_{out} = I_{pv} - I_s \left(e^{\frac{V_{out\_pv} + R_s I_{out}}{nV_t}} - 1 \right) - \frac{V_{out\_pv} + R_s I_{out}}{R_{sh}} \tag{4.1}$$

There are five model parameters that depend on the PV cell fabrication process. I_{pv} is the equivalent current source modeling the current generated by the photovoltaic effect, I_s is the diode saturation current, n is the diode ideality factor, R_s is the PV cell series resistance and R_{sh} is the PV cell shunt resistance.

There is also a dependence of temperature T, modeled by the thermal voltage $V_t = \frac{kT}{q}$, in which q is the electron charge and k is the Boltzmann constant. The current I is implicit in Eq. 4.1, so it is necessary to implement a numerical solver to estimate it as a function of the output voltage (V) and free parameters.

Consider that the PV cell is biased in DC and a small AC component i_{pv} is applied representing a received signal. If $i_{pv} << I_{pv}$, diode D_1 can be replaced by its dynamic model, which comprises a dynamic resistance r_d in parallel with an equivalent capacitance C_{eq}, as shown in Fig. 21 (LORRIERE et al., 2020) (KIM et al., 2013). The equivalent capacitance is a parallel association of diffusion capacitance C_d and junction capacitance C_j that determines the dynamic properties of the PV cell (HERMAN; JANKOVEC; TOPIč, 2013). The diffusion capacitance C_d occurs due to stored charge of minority electrons and minority holes near the depletion region. C_d is thus proportional to the minority carrier lifetime. The junction capacitance C_j in forwarded biased p-n junction is dependent on doping concentration, material and geometry properties. Both capacitances are non-linear with respect to the bias voltage, which results in a variation for different illuminance levels and output loads.

4.3 MEASUREMENT SETUP

To obtain a real estimate of the bandwidth of a PV cell for communication purposes in an indoor environment, we performed a series of electrical measurements for DC and AC characterization. The target is a 20 x 40 mm polycrystalline Si cell illuminated by an array of conventional white LEDs. The illuminance is between 50 and 500 lux, which

Figure 20 – PV Cell 1D2R static electrical model.

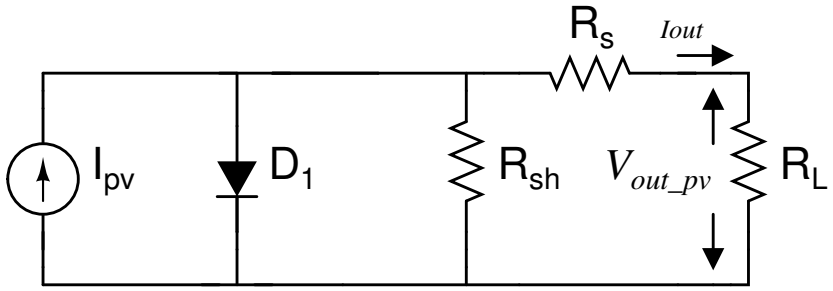
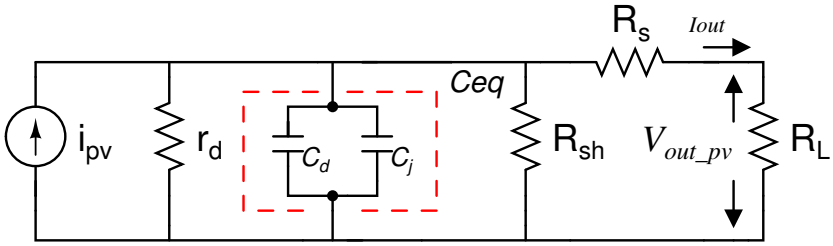


Figure 21 – PV Cell AC small-signal electrical model.



corresponds to a typical illuminance in an office room with artificial light. The following subsections detail the measurement setups for DC and AC characterization.

4.3.1 MEASUREMENT OF THE I-V CHARACTERISTIC CURVE

To obtain real data for parameter extraction, I-V measurements were performed on a compact 20x40 mm crystalline silicon photovoltaic (PV) cell. Illumination was provided by a cold LED lamp, more specifically a 50 W MTX mini floodlight model, and tests were conducted during nighttime to mitigate any interference from natural light. The ambient temperature during the measurements was about 24°C. The measurement arrangement is depicted in Figure 22, which shows the block diagram of the whole setup. The output of the PV cell was connected to a B1500A semiconductor parameter analyzer, which acted as a voltage source that could be varied from 0 to 1 V with a step of 0.6 mV. This setup effectively simulated a variable load resistance (R_L) ranging from 0 to infinite. To measure illuminance, an Instrutherm LD -550 luxmeter was strategically positioned near the target PV cell. The configuration of the actual experimental setup is shown in Figure 23.

The I-V characteristics were obtained for different illuminances between 50 and 500 lux. The illuminances were obtained by placing the light source at different distances from the PV cell.

4.3.2 MEASUREMENT OF THE AC RESPONSE

The configuration for performing measurements is illustrated by the block diagram shown in Fig. 24. For this purpose, the low-frequency transfer function module LF3L5 of the Agilent E5061B network analyzer is used to generate a frequency sweep signal and to

Figure 22 – Block diagram of the PV cell I-V measurement setup.

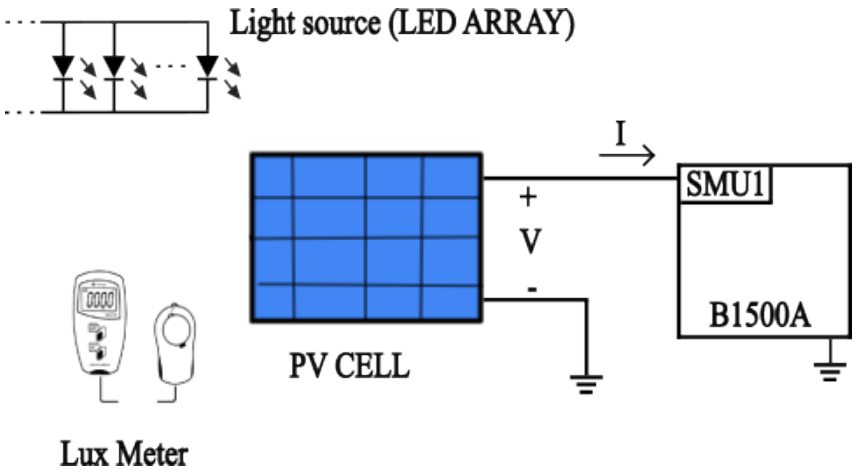


Figure 23 – Experimental setup for the PV cell I-V measurement.

measure the AC transfer function of the proposed characterization system. The generated AC signal is amplified and combined with a DC level to finally drive an array of LEDs. This amplification is performed by the amplifier shown in Figure 25. By varying the resistor R_B, the DC collector current of the transistor can be adjusted directly proportional to the DC base current (Ib), thus controlling the light intensity emitted by the LEDs. The PV cell is located a short distance of 45 cm from the LED array in an enclosed compartment, ensuring that the illuminance cannot be affected by external fluctuations. Next to the PV cell is a digital luxmeter (model MLM-1020), employed to measure the illuminance. To obtain a comprehensive evaluation, the output voltage generated by the PV cell is connected back to the network analyzer, creating a closed loop that allows the system gain to be measured. By sweeping the frequency of the input AC signal, the overall AC response of the solar cell can be measured. By changing the load resistance R_L, the PV cell can be biased across different operating conditions. A visual representation of the implemented measurement setup can be found in Fig. 26.

Figure 24 – Block diagram for PV cell AC measurement setup.

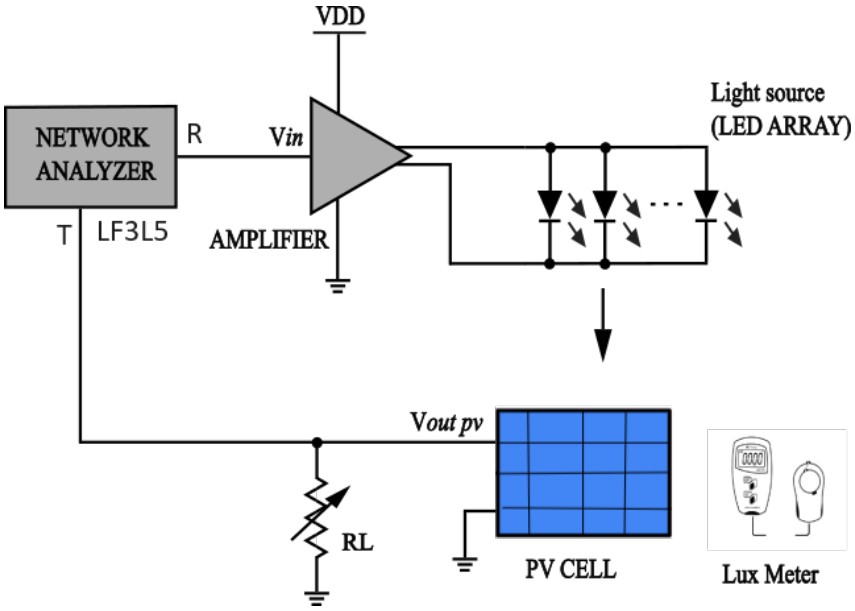
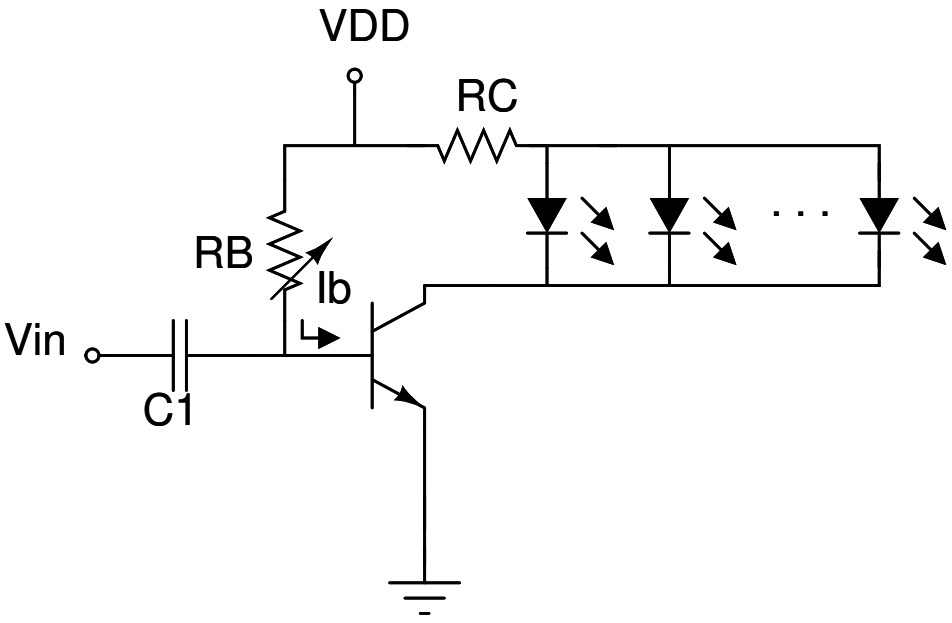


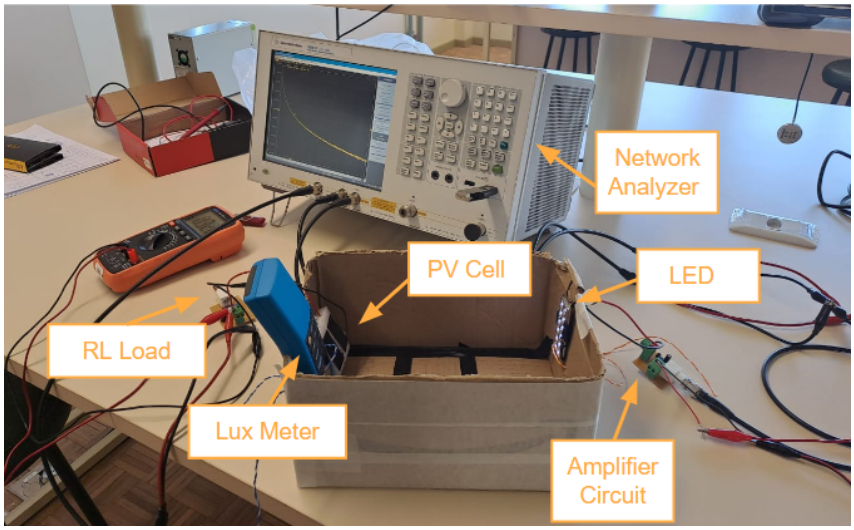
Figure 25 – LED amplifier circuit.



The AC response obtained from the measurements can be seen in Fig. 27 for three different operating conditions: maximum power point (MPP), open circuit (OC) and short circuit (SC). The input AC power was configured at -30 dBm, with the ambient temperature held constant at 24°C.

The illuminance incident on the PV cell ranged from 50 lux to 500 lux, encompassing the entire range of interest. All plots show normalized voltage gain, with the -3 dB frequencies (cutoff frequencies) indicated by blue markers. The graphs of cutoff frequencies versus illuminance is shown in Figure 28. It can be seen that f_c exhibits a linear increase with illuminance, albeit at different rates depending on the operating point of the PV cell.

Figure 26 – PV cell AC characteristics measurement setup. Box containing the PV cell is closed during measurement so that the illuminance level does not suffer variation from external sources.



The narrowest bandwidth is observed at MPP, where f_c ranges from 880 Hz to 2.8 kHz and increases at a rate of 4.4 Hz/lux. Meanwhile, in OC, the cutoff frequency increases at a rate of 8.8 Hz/lux, whereas in SC it increases even faster to 20.9 Hz/lux. This leads to a f_c peak of 10.8 kHz at 500 lux in the SC scenario.

It is not practical to measure the AC characteristics of a PV cell for all illuminances. Therefore, translation equations are required to scale the characteristic points of the cell as a function of illuminance G (TEH et al., 2021). Three measured points were selected (50, 250, and 500, in Fig. 29 in orange) and the translation functions (in blue) were estimated by a curve fitting procedure, resulting in the following expressions:

$$f_c(MPP) = 4.3662 \cdot G + 661.3750 \tag{4.2}$$

$$f_c(OC) = 8.7315 \cdot G + 349.7316 \tag{4.3}$$

$$f_c(SC) = 20.8752 \cdot G + 271.7869 \tag{4.4}$$

With these expressions, it is possible to estimate the cutoff frequency for all intermediate points in the range of interest.

Looking at the behavior of the cutoff frequency as a function of PV cell load, we can see that it is not linear. Fig. 30 shows the measurement results for the cutoff frequency as a function of the output voltage generated by the PV cell illuminated at 200 and 300 lux. A high output voltage means operation close to open circuit, while a low output voltage refers to the operation close to short circuit. It can be seen that there is a point of minimum bandwidth between 0.15 and 0.20 V, which match with the maximum power point. This result confirms the hypothesis that the best bias point of the PV cell for energy harvesting is the worst bias point for visual light communication.

Figure 27 – Measurement results for the closed loop gain of a 20 x 40 mm PV cell biased in 3 different points: a) MPP; b) open circuit; c) short circuit.

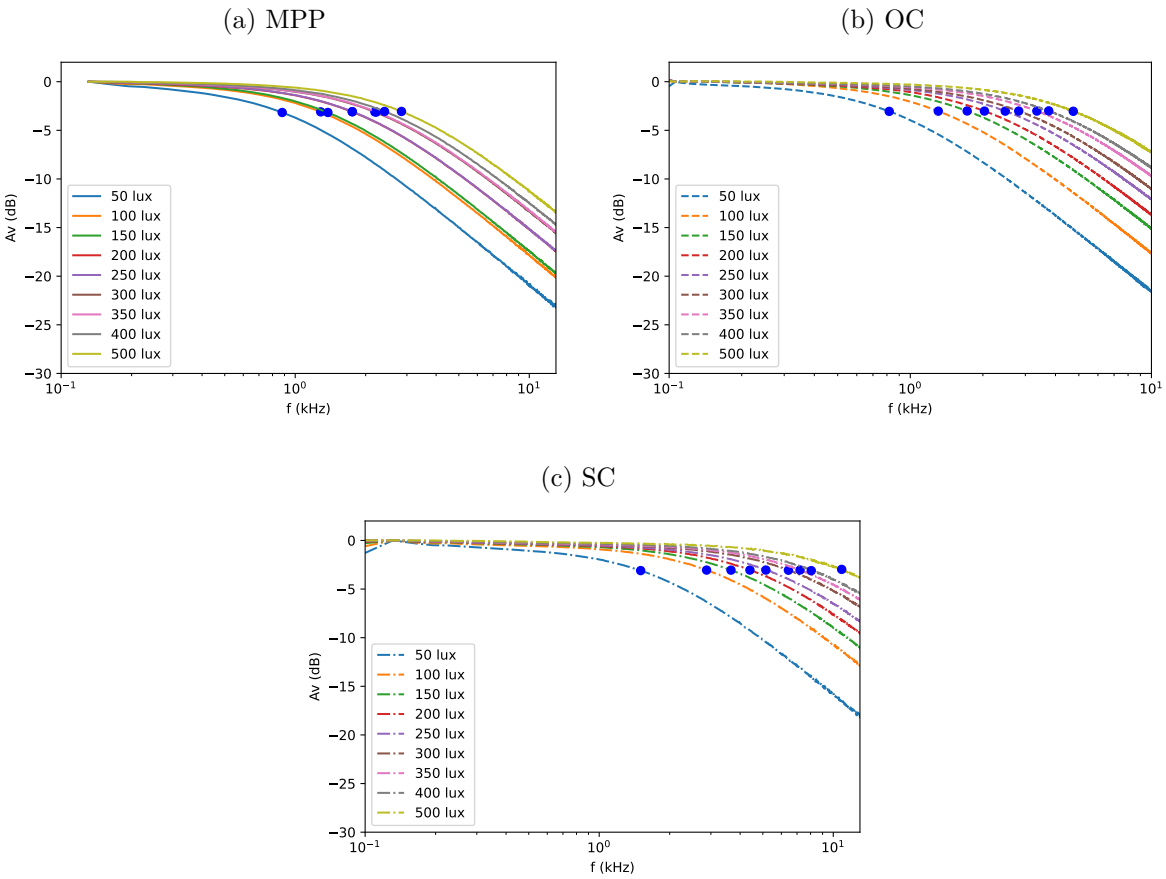
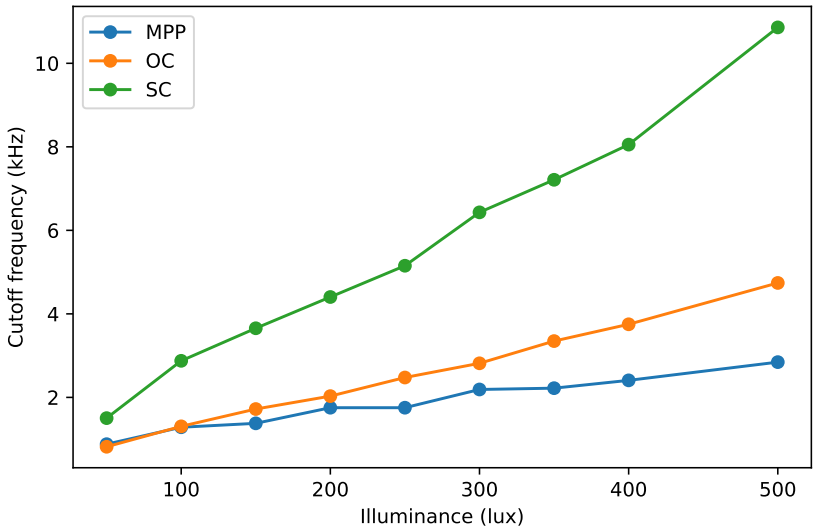


Figure 28 – Measurements of cutoff frequency in function of illuminance for three different bias conditions.



If we consider the PV cell has to simultaneously perform VLC and power transfer, it is possible to define a figure of merit combining both performance parameters as:

Figure 29 – Translated cutoff frequency x Illuminance. a) In MPP; b) Open circuit; c) Short circuit. Red dots represent the measured points, and the highligthed dots are the points used to determine the translation function.

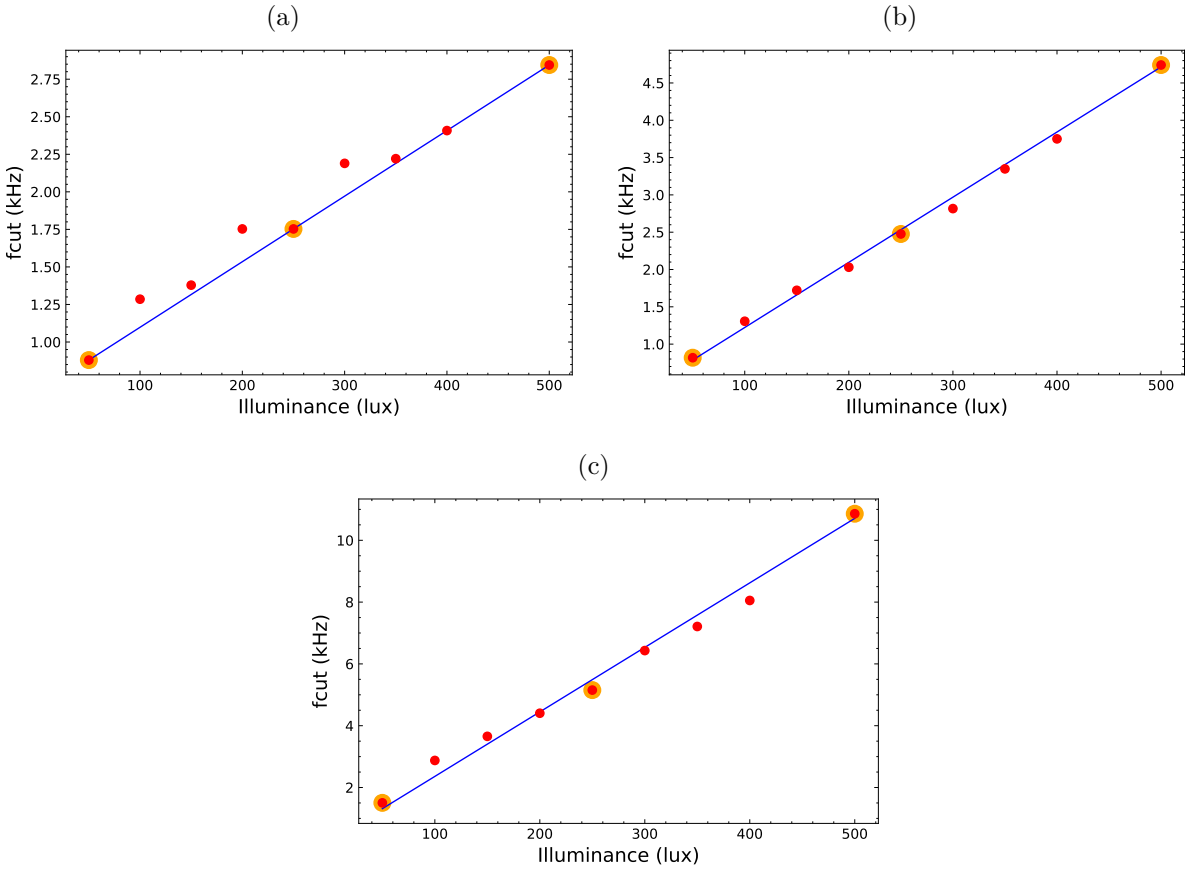


Figure 30 – Measurement of cutoff frequency versus output voltage.

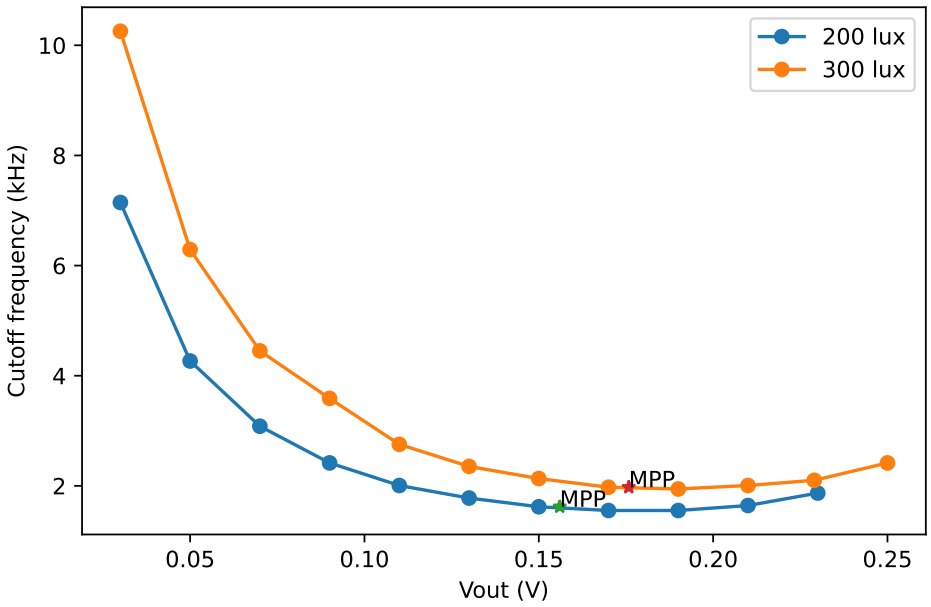
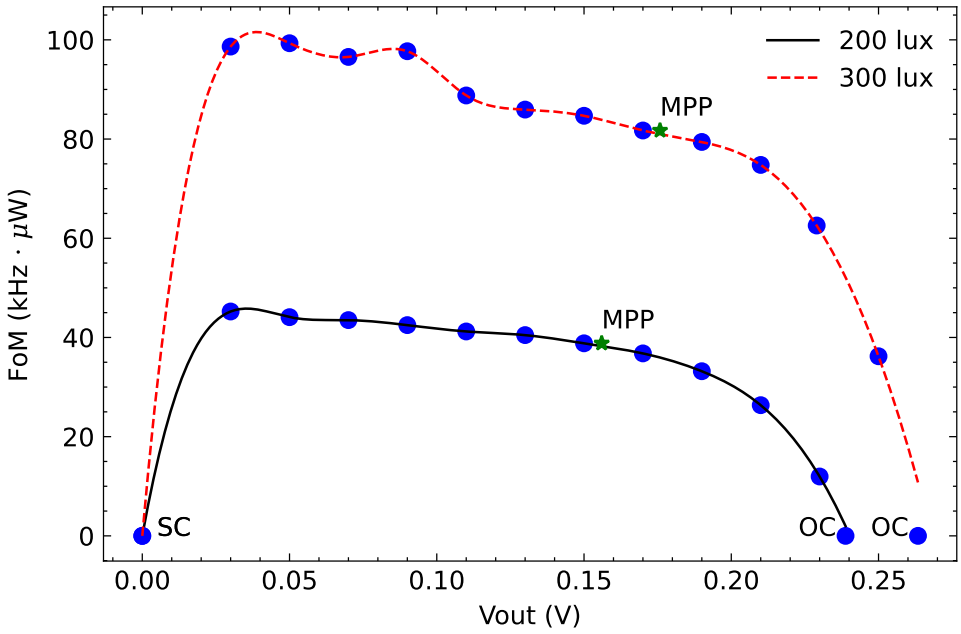


Figure 31 – Figure of merit (eq. 4.5) for different loads.



$$FoM = f_c \cdot P_{out} \tag{4.5}$$

Here P_{out} is the power delivered by the PV cell at its output. Relating the FoM to V_{out}, the results can be seen in Fig. 31. The higher FoM is located a few mV from the short-circuit bias point and decreases slightly up to MPP. While the maximum bandwidth is achieved under short-circuit condition, the energy harvest at this point is negligible due to the extremely low DC voltage. Therefore, biasing the PV cell at MPP can be a good choice to compromise between delivered power and bandwidth. When V_{out} is biased higher than MPP, the FoM decreases sharply, and this region must be avoided in both cases. The open circuit point leads to the worst FoM.

4.4 PARAMETER EXTRACTION PROCEDURE

Based on the obtained measurements, it is possible to extract the AC parameters of the PV cell small-signal electrical model shown in Fig. 21. To do this, we first need to extract the DC parameters for the 1D2R PV cell model. We implemented the extraction method described in (MONTEIRO et al., 2022) considering the same illuminances used in the AC measurements and extracted the values of n, I_S, I_{PV}, R_S, and R_{SH} that model the equivalent circuit of Fig. 20.

4.4.1 DC PARAMETERS

Six significant characteristics points can be discerned and extracted from the plotted curves. One of them, the open circuit voltage (V_{oc}), is determined at the points

where $I = 0$, as shown in Figure 32a. The short-circuit current (I_{sc}) can be estimated by examining the I-V characteristic curves at the points where $V = 0$. Additionally, two parameters, namely the reciprocals of the slopes at the open-circuit and short-circuit points, are denoted as R_{s0} and R_{sh0}, respectively. These values are calculated according to the following expressions:

$$R_{s0} = -\frac{dV}{dI}\bigg|_{V=V_{oc}} \tag{4.6}$$

$$R_{sh0} = -\frac{dV}{dI}\bigg|_{I=I_{sc}} \tag{4.7}$$

For calculating the slope of $1/R_{sh0}$ we used the first 100 points of the curves of Fig. 32a, which corresponds to a ΔV of 60 mV. For calculating $1/R_{s0}$ we used the last 15 points of the curves, corresponding to the steady-state region which results in a ΔV of 9 mV. These specific number of points was were empirically chosen to provide a reliable average while minimize the influence of numerical noise at the end of the curve.

The maximum power point can be seen from the power-voltage curves (Fig. 32b). At these points it is possible to estimate the voltage V_{mp} and current I_{mp} that extract the maximum power from the PV cell.

From these 6 measured characteristic points it is possible to calculate the 5 parameters of the 1D2R PV cell model using the following procedure (MONTEIRO et al., 2022).

The shunt resistance is estimated to be equal to R_{sh0}:

$$R_{sh} = R_{sh0} \tag{4.8}$$

The value of n can be extracted from the maximum power point as:

$$n = \frac{V_{mp} + I_{mp}R_{s0} - V_{oc}}{V_t\Big(\ln(I_{sc} - \frac{V_{mp}}{R_{sh}} - I_{mp}) - \ln(I_{sc} - \frac{V_{oc}}{R_{sh}}) + \frac{I_{mp}}{I_{sc} - \frac{V_{oc}}{R_{sh}}}\Big)} \tag{4.9}$$

The diode saturation current I_s can be defined as:

$$I_s = (I_{sc} - \frac{V_{oc}}{R_{sh}})e^{\frac{-V_{oc}}{nV_t}} \tag{4.10}$$

Considering equation (4.6) and assuming R_{sh} is large, we obtain:

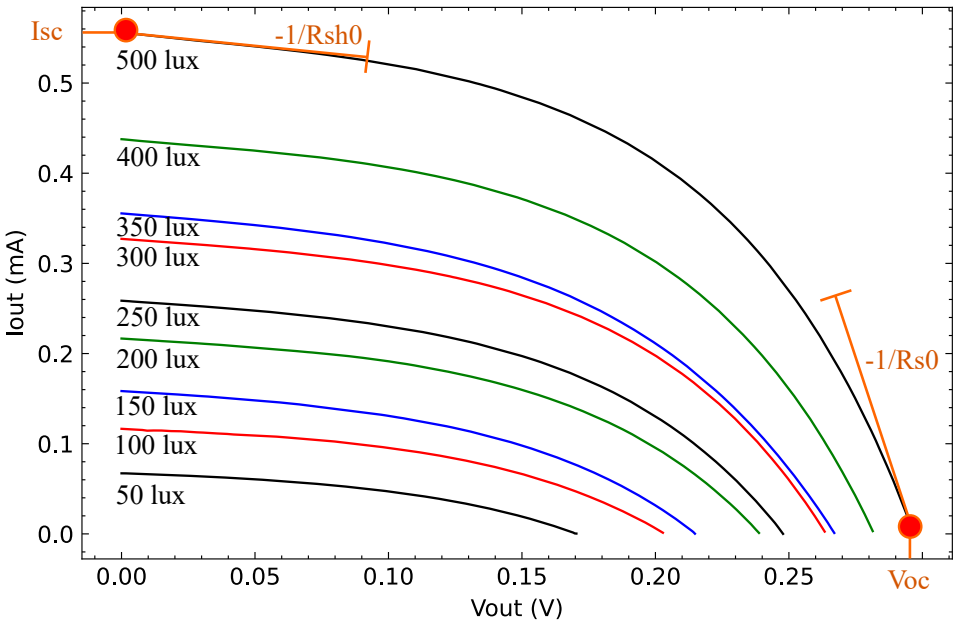
$$R_s = R_{s0} - \frac{nV_t}{I_s}e^{\frac{-V_{oc}}{nV_t}} \tag{4.11}$$

Finally, I_{pv} can be isolated as:

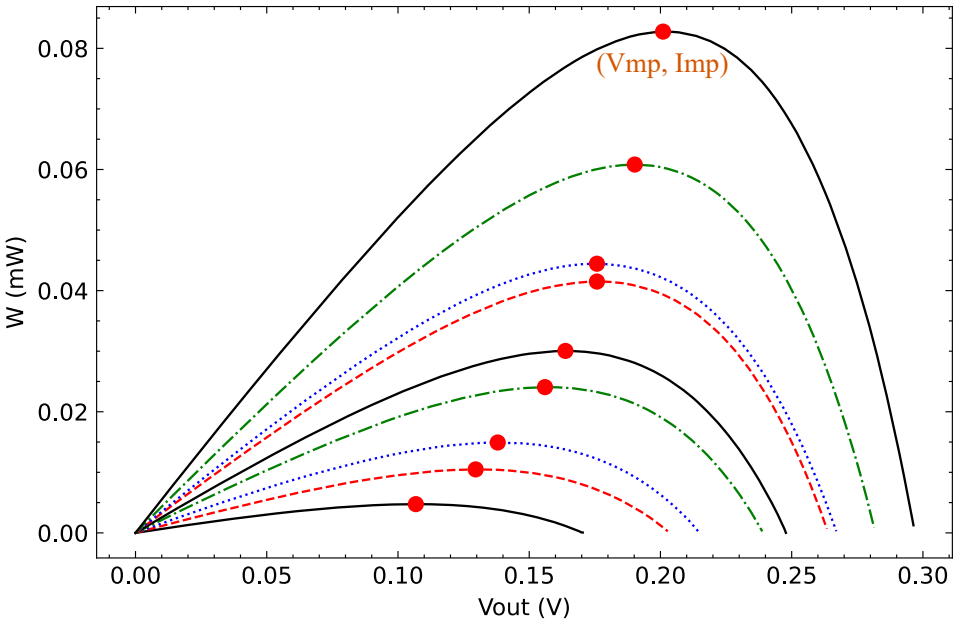
$$I_{pv} = I_{sc}(1 + \frac{R_s}{R_{sh}}) + I_s(e^{\frac{I_{sc}R_s}{nV_t}} - 1) \tag{4.12}$$

Figure 32 – Measurement results for a 20 x 40 mm PV cell. a) Current-voltage characteristics; b) Power-voltage characteristics with the indication of maximum power points (red dots).

(a)



(b)



The results for the extraction of DC parameters of the 1D2R model are presented in Tab. 4. An increase in I_{pv}, I_s and n with illuminance can be observed, whereas R_s and R_{sh} exhibit the opposite behavior. The RMSE column reports the root mean square error of the analytical output current relative to the measured values.

Table 4 – Extracted DC 1D2R model parameters for different illuminance levels.

Illuminance (lux)	I_{pv} (mA)	I_s (μA)	n	R_s (Ω)	R_{sh} (kΩ)	RMSE (mA)
50	0.0708	0.0748	1.0382	373.6491	6.9897	0.0014
100	0.1202	0.2164	1.3123	195.5369	6.5076	0.0014
150.4	0.1620	0.4592	1.5107	98.9600	4.6656	0.0022
200	0.2206	0.4778	1.5770	82.9531	4.8232	0.0021
250	0.2624	0.6964	1.6907	57.9388	4.3668	0.0026
300	0.3320	0.6788	1.7078	57.2898	4.2135	0.0021
350	0.3623	0.8041	1.7611	65.9515	3.6991	0.0034
400	0.4429	0.8858	1.8078	41.2964	3.8660	0.0024
500	0.5622	0.8758	1.8282	32.1803	3.1983	0.0029

4.4.2 AC PARAMETERS

The parameters for the AC PV Cell from Fig. 21 are extracted based on the DC parameters and the closed-loop measurements as a function of frequency shown in Fig. 27 (MONTEIRO et al., 2023).

The dynamic resistance can be estimated from the following static parameters:

$$r_d = \frac{n \cdot V_t}{I_{pv}} \tag{4.13}$$

This dependence results in a variation of r_d with illuminance, reducing the value as the illuminance increases.

The effective minority carrier lifetime τ is given equation 4.14:

$$\tau = r_d \cdot C_{eq} \tag{4.14}$$

The small-signal model reveals a single-pole circuit whose equivalent resistance r_0 can be estimated as:

$$r_0 = \frac{1}{\frac{1}{r_d} + \frac{1}{R_{sh}} + \frac{1}{R_s + R_L}} \tag{4.15}$$

It can be related to an equivalent first-order lowpass filter whose -3 dB cutoff frequency f_c is given as:

$$f_c = \frac{1}{2 \cdot \pi \cdot r_0 \cdot C_{eq}} \tag{4.16}$$

So, the diode equivalent capacitance can be estimated as follows:

$$C_{eq} = \frac{1}{2 \cdot \pi \cdot f_c \cdot r_0} \tag{4.17}$$

Resistance r_d is in the same order of magnitude than R_s and is much lower than R_{sh}. It can be seen that the pole location is dependent on the load R_L applied to the PV cell. In open circuit (very high R_L), the equivalent output resistance approaches the value

of r_d. On the other side, if the PV cell is operating in short circuit (very small R_L), r_0 approaches $r_d||R_s$.

The bandwidth is subject to variations influenced by temperature and injection level, as it is intrinsically governed by the minority carriers lifetime (τ). As stated in (LORRIERE et al., 2020), due to the correlation between the efficiency of a solar cell (with regards to energy harvesting) and the lifetime of the minority carriers, achieving a photoreceiver with elevated bandwidth cannot be anticipated when employing a highly efficient PV cell operating at the maximum power point (MPP).

Knowing the values of n and I_{PV} we extract the diode dynamic resistance r_d using eq. 4.13. For the three bias regions (MPP, OC and SC), and for illuminances ranging from 50 to 500 lux, the equivalent output resistance r_0 is calculated by eq. 4.15 using the DC parameters R_s and R_{sh}. With the measured values of f_c, the value of the diode equivalent capacitance C_{eq} can be estimated using eq. 4.16. The extracted AC parameters are summarized in Tab. 5. The load resistance R_L was adjusted to bias the PV cell in MPP for the maximum delivered power scenario. For open circuit, R_L was fixed in 100 MΩ. For emulating the SC scenario, R_L was set to the minimum value that approached V_{out} to zero (although not achieving exactly 0 V due to limitations in the measurement equipment).

The graphs in Fig. 33 show the estimated values of r_d, r_0, and C_{eq} as a function of illuminance for the three bias regions of interest. It is clear that the resistances decrease with increasing illuminance in all cases. Since the cutoff frequency increases linearly with illuminance, and it is related to r_0 as defined in eq. 4.16, the equivalent resistance r_0 decreases proportionally to 1/G. This behavior is confirmed with the extracted parameters. The equivalent capacitance, on the other hand, behaves differently in the MPP than in the OC and SC regions, but with a smaller variation as a function of illuminance.

To evaluate the quality of the extracted parameters with respect to the measurement results, we simulated the PV cell closed loop response, as shown in Fig. 34. It is possible to notice the good fitting between analytical and measurement results, demonstrating that the proposed parameter extraction procedure is adequate for simulating the device for communications.

4.5 PV CELL BIASING FOR COMMUNICATION

As shown before, the near-SC region presents the best FoM for simultaneous use of the PV cell for generating power and for communications purposes. However, operating close to the SC region makes the voltage signal to be very small, reducing the signal to noise ratio (SNR) of the communication signal. Thus, at SC operation it is interesting to use the output AC current signal instead the output AC voltage signal. In this case, a transimpedance amplifier (TIA) should be employed to convert the AC current level in a reasonable voltage level.

Any voltage signal developed across the PV cell reacts with the internal P-N junction capacitance, shunting the output current at higher frequencies. Reducing the effects of the voltage across the PV cell capacitance greatly improves bandwidth. This can be achieved by isolating the signal voltage from the PV cell using a current-to-voltage converter (GRAEME, 1995). The circuit depicted in Fig. 35 implements this function. It is a transimpedance amplifier (TIA), an active converter that transforms input current to a corresponding output voltage. This configuration represents a simple inverting amplifier with negative feedback. A feedback resistor, R_f, connects the output to the inverting terminal of the amplifier. The virtual ground at the input of the operational amplifier forces the PV cell to operate near the short-circuit bias point.

We have implemented this circuit using an AD823AN operational amplifier with R_f equal to 8.18 kΩ. Its high input impedance makes the input current practically negligible. Consequently, all the current generated by the PV cell flows through R_f. Challenges arise from the input of the operational amplifier, which introduces an inherent parasitic capacitance that results in an undesirable second pole location and consequently a poor phase margin. To mitigate this instability, the solution is to introduce a feedback capacitor C_f (1013 pF in our implementation) that operates in parallel with R_f to compensate this pole. The bandwidth of the whole circuit thus depends mostly on the value of C_f and R_f, and only to a very small extent on the internal capacitance of the PV cell.

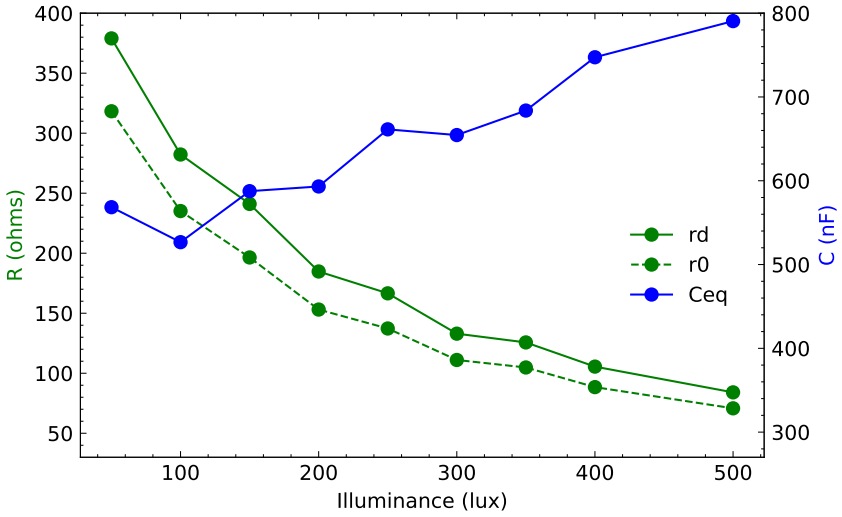
Fig. 36a shows the measured frequency response of the PV cell connected to the TIA for illuminances from 50 to 250 lux. It can be seen that the voltage gain remains relatively constant as the illuminance changes from DC to 30 kHz. In Fig. 36b the phase response is shown. At low frequencies, minimal phase variations can be seen as the illuminance changes. On the other hand, significant variations can be noticed at higher frequencies. Driving the PV cell with a TIA at a low illuminance of only 50 lux increased f_c by approximately 20×, whereas at 500 lux f_c increased roughly 3×. Therefore, this approach is essential for a wider bandwidth VLC system for indoor use.

This simple TIA produces a significant offset for higher gain applications. Alternatives are to replace the R_f resistor with a tee-network or with a DC offset cancellation loop, as demonstrated in (ZHANG et al., 2019).

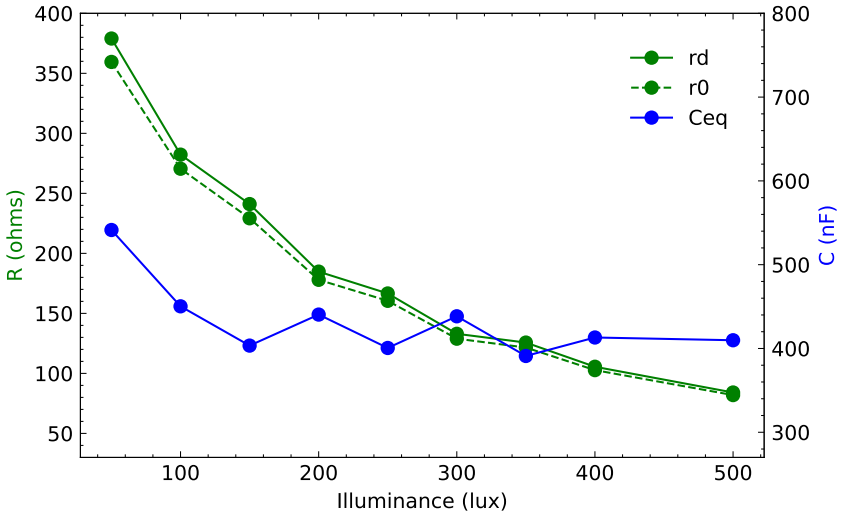
The measurement results confirm the bandwidth improvement by the TIA circuit, which is important for the adoption of PV cells as receivers in VLC systems.

Figure 33 – Extracted dynamic resistance r_d, equivalent resistance r_0 and equivalent capacitance C_{eq} versus the illuminance level.

(a) MPP



(b) OC



(c) SC

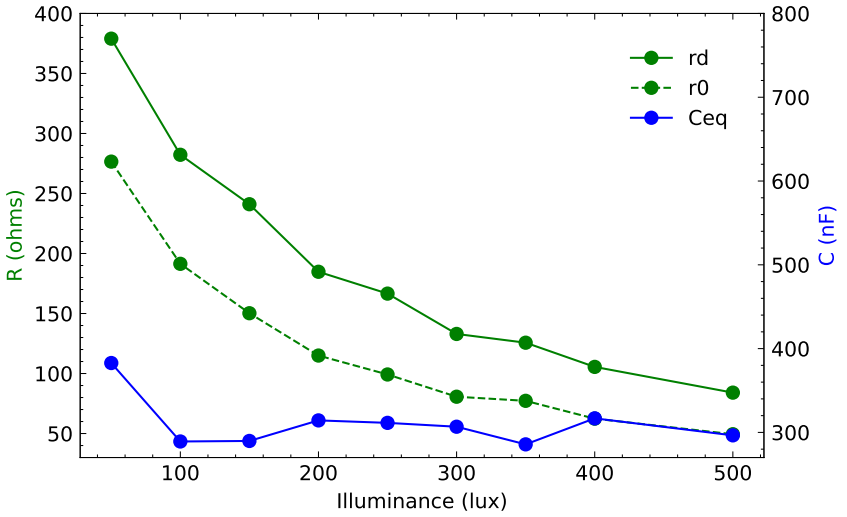
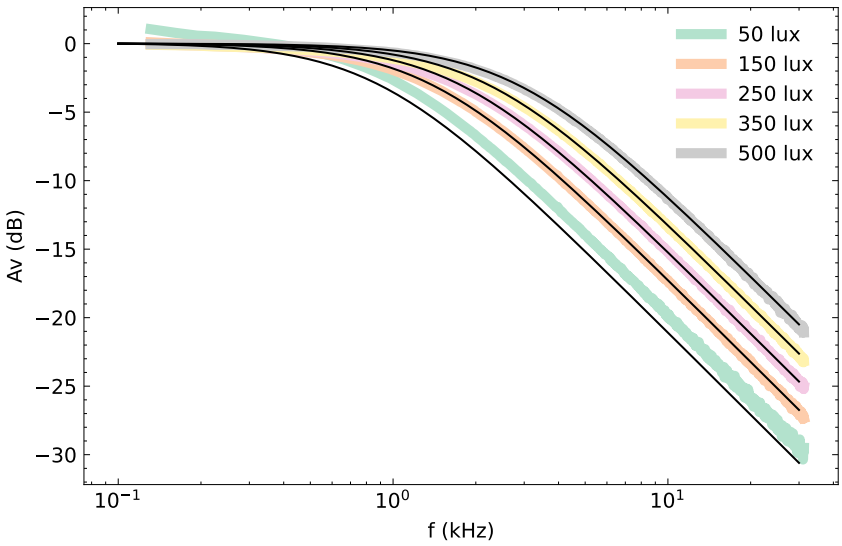
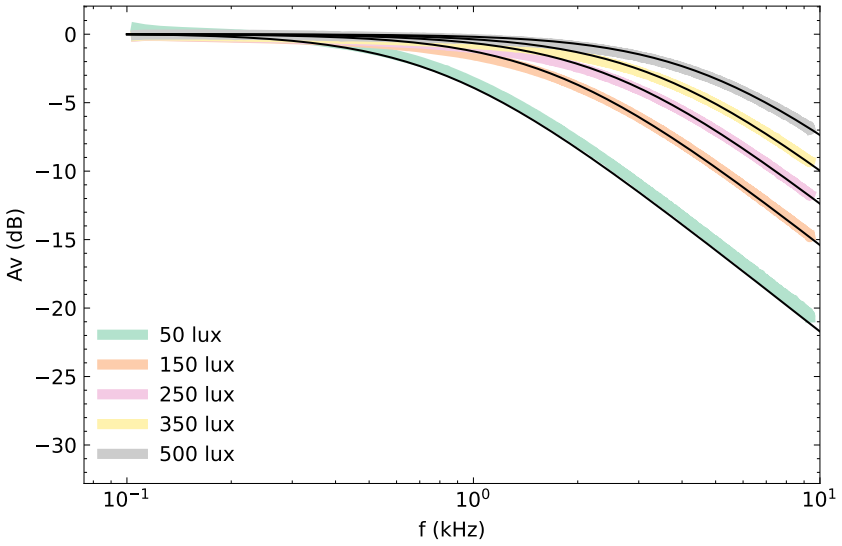


Figure 34 – Comparison of measurement (thick color lines) and analytical (thin black lines) closed loop characteristic of the PV cell for three bias conditions: a) Maximum power point; b) Open circuit; c) Short circuit.

(a) MPP



(b) OC



(c) SC

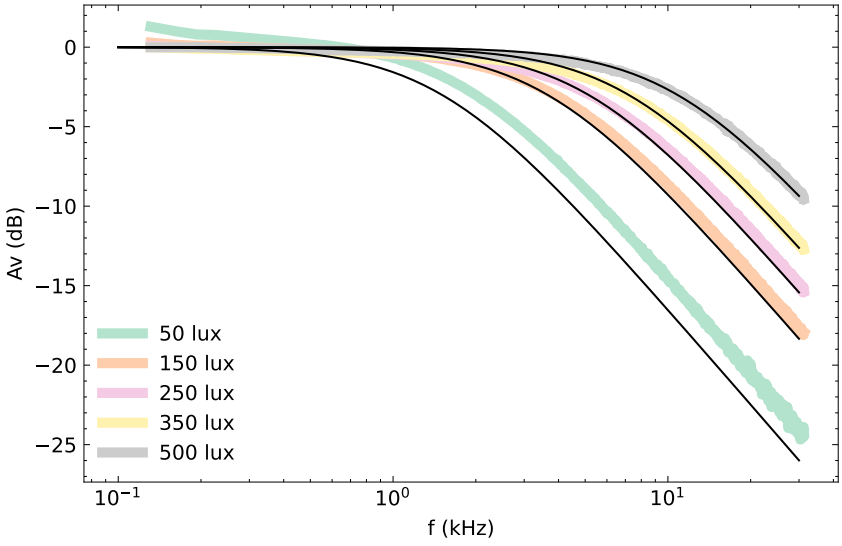


Figure 35 – PV-Cell connected to a transimpedance amplifier (TIA).

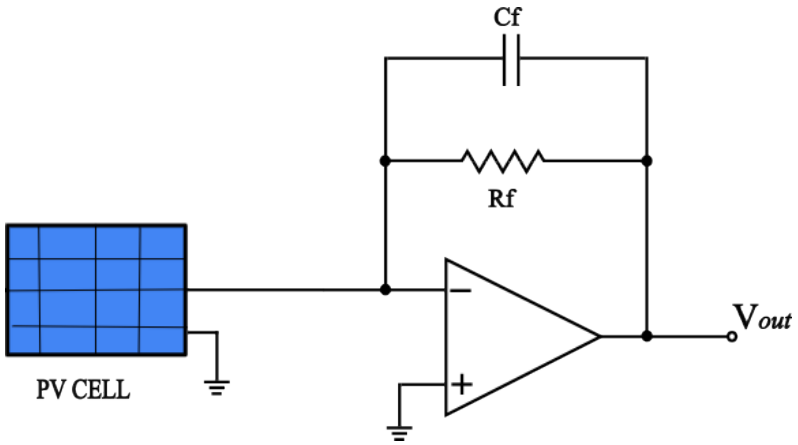
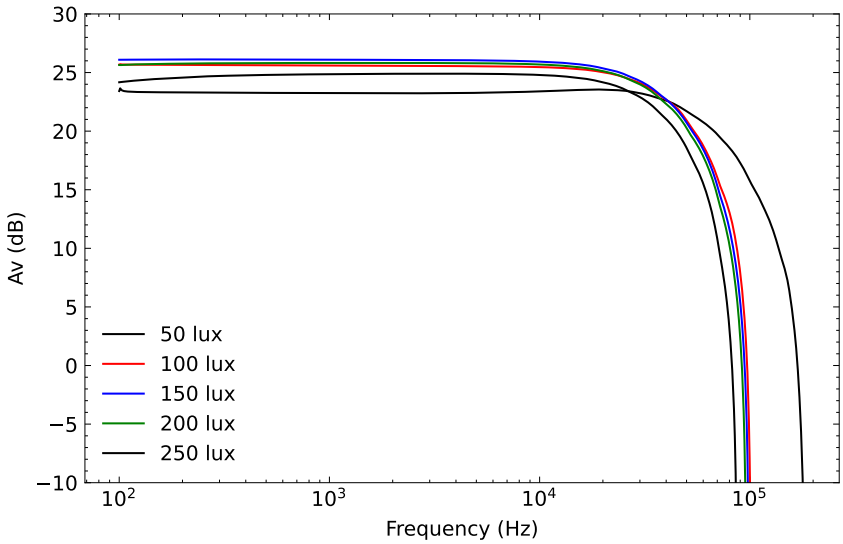


Figure 36 – Measured AC response of the PV cell driver by the TIA circuit of Fig 35 for different illuminance levels.

(a) Gain



(b) Phase

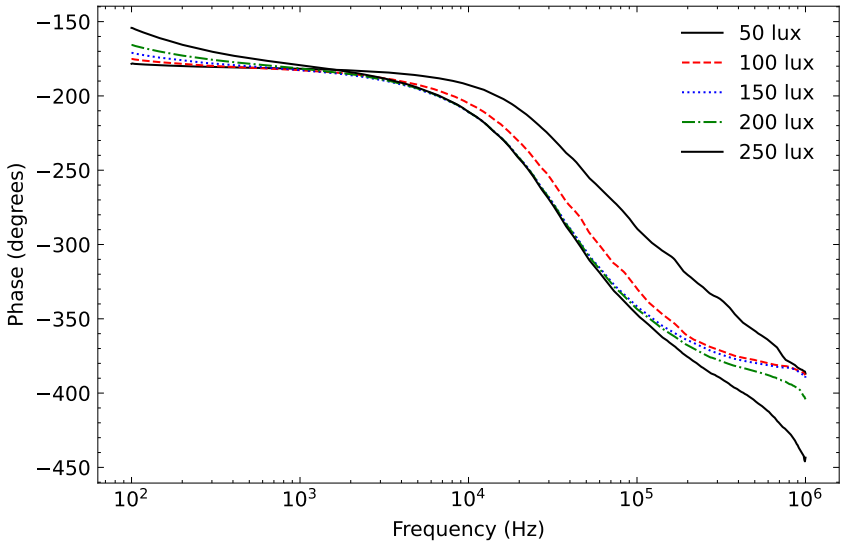


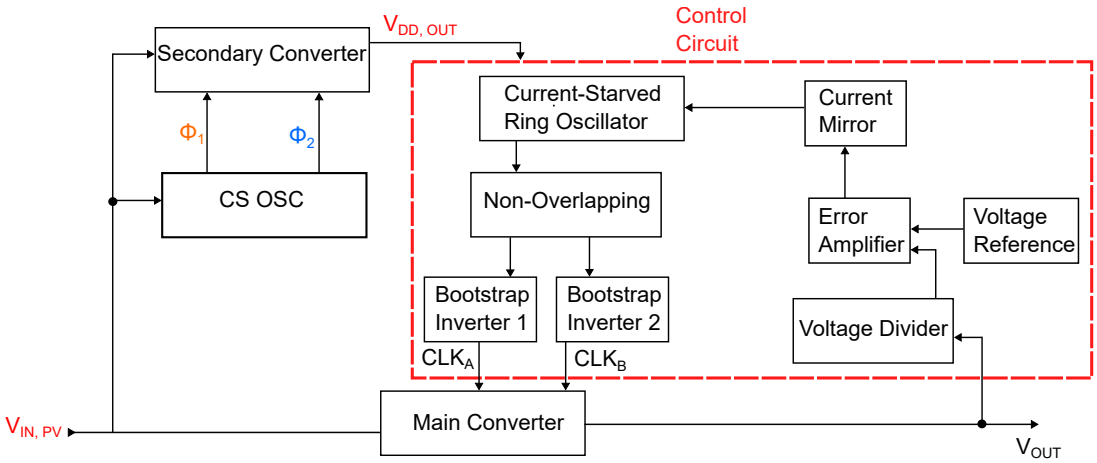
Table 5 – Extracted AC PV cell model parameters for different illuminance levels in three bias conditions.

Bias	Illum. (lux)	r_d (Ω)	R_s (Ω)	R_{sh} (Ω)	R_L (Ω)	r_0 (Ω)	C_{eq} (nF)	τ (μs)	f_c (kHz)
MPP	50	378.98	373.65	6989.75	2402.59	318.28	568.44	180.92	0.88
	100	282.24	195.54	6507.59	1602.10	235.13	526.71	123.84	1.29
	150	241.06	98.96	4665.63	1276.12	196.47	587.57	115.44	1.38
	200	184.78	82.95	4823.15	1011.15	153.06	593.17	90.79	1.75
	250	166.58	57.94	4366.81	893.03	137.29	661.32	90.79	1.75
	300	132.97	57.29	4213.48	744.79	111.05	654.53	72.69	2.19
	350	125.67	65.95	3699.14	695.41	104.81	683.76	71.67	2.22
	400	105.52	41.30	3865.98	594.82	88.44	747.38	66.10	2.41
	500	84.07	32.18	3198.29	488.15	70.78	790.53	55.95	2.84
OC	50	378.98	373.65	6989.75	100 M	359.49	541.39	194.63	0.82
	100	282.24	195.54	6507.59	100 M	270.51	450.31	121.81	1.31
	150	241.06	98.96	4665.63	100 M	229.22	403.42	92.47	1.72
	200	184.78	82.95	4823.15	100 M	177.96	440.45	78.38	2.03
	250	166.58	57.94	4366.81	100 M	160.46	400.60	64.28	2.48
	300	132.97	57.29	4213.48	100 M	128.90	438.41	56.51	2.82
	350	125.67	65.95	3699.14	100 M	121.55	391.06	47.53	3.35
	400	105.52	41.30	3865.98	100 M	102.72	413.10	42.43	3.75
	500	84.07	32.18	3198.29	100 M	81.92	409.82	33.57	4.74
SC	50	378.98	373.65	6989.75	824.86	276.54	382.80	105.86	1.50
	100	282.24	195.54	6507.59	458.88	191.40	289.17	55.35	2.88
	150	241.06	98.96	4665.63	337.11	150.24	289.80	43.54	3.66
	200	184.78	82.95	4823.15	241.90	114.97	314.33	36.14	4.40
	250	166.58	57.94	4366.81	201.92	99.20	311.38	30.89	5.15
	300	132.97	57.29	4213.48	158.31	80.67	306.78	24.75	6.43
	350	125.67	65.95	3699.14	146.00	77.25	285.73	22.07	7.21
	400	105.52	41.30	3865.98	117.62	62.39	316.77	19.76	8.05
	500	84.07	32.18	3198.29	92.46	49.43	296.48	14.66	10.86

5 PROPOSED SWITCHED CAPACITOR CONVERTER TOPOLOGY

The proposed components for the energy harvesting system outlined in this chapter are indeed designed to address various aspects of energy harvesting and power management. The characterization of photovoltaic (PV) cells involves understanding their behavior under varying conditions, which is crucial for optimizing their performance. The cold-start circuit, composed of a ring oscillator, a non-overlapping clock circuit powered by a clock-booster and voltage-booster, two bootstrap inverters, and a Dickson charge pump, serves as a crucial element for initiating the operation of the energy harvesting system, particularly in low-power or startup conditions. The complete schematic diagram of the proposed work is presented in Figure 37.

Figure 37 – Complete Schematic Diagram of the Energy Harvester.



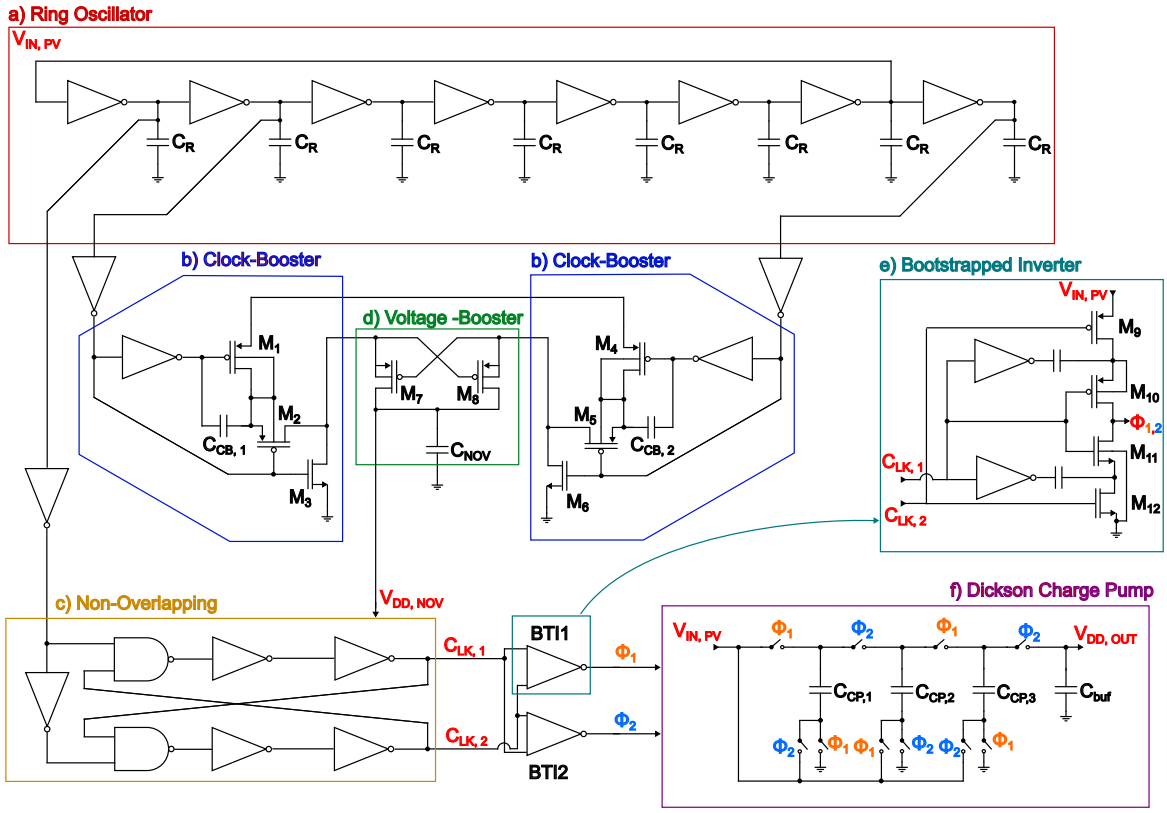
5.1 COLD-START SYSTEM

Energy harvesting systems typically comprise an energy transducer tailored to the specific energy source, a DC-DC converter serving as a voltage regulator, and a feedback control circuit. Nevertheless, the voltage produced by the transducer fluctuates due to external influences. Consequently, the DC-DC converter is employed to stabilize the variable DC voltage from the transducer, ensuring a consistent voltage level suitable for operation of IoT circuits.

Numerous DC-DC converters utilize either switched-capacitor (SC) or switched-inductor (SI) techniques. These converters rely on a switching frequency to move between various topological states. However, the generation of this switching frequency is directly influenced by the output voltage of the DC-DC converter. When the output voltage decreases to a point where the clock generation circuit cannot oscillate effectively to drive the control mechanisms, a significant issue arises.

The possible issues mentioned above make necessary the implementation of a cold-start circuit and typically they consist of a low-voltage oscillator, a clock boosting unit, and a multi-stage charge pump circuit. The cold-start system can be deactivated after

Figure 38 – Cold-Start Circuit.



the startup phase, once the converter system stabilizes and reaches a steady operational state. At this point, the converter's output voltage becomes sufficient to power the control system effectively.

The output voltage of a DC-DC converter for ultra-low voltage (ULV) application ranges from 0.4 to 0.5 V (SILVA; SEVERO; GIRARDI, 2020). However, the voltage generated by the transducer in energy harvesting systems fluctuates due to external factors. This variability poses a challenge as the resulting voltage might not be sufficient to power the clock generation system adequately. Higher switching frequencies and voltage swings are essential to drive the switches effectively and reduce the converter's output resistance.

Consequently, even after the converter system stabilizes, the cold-start circuit remains operational to supply the entire control system with the necessary higher voltage. This circuit's unique design combines a low cold-start voltage with high-frequency switching capability, ensuring effective operation with low input voltages while still enabling energy harvesting.

A cold-start circuit is indeed indispensable in energy harvesting systems, allowing them to function reliably even with extremely low input voltages. Recently, integrated switched-capacitor (SC)-based cold-start circuits have emerged for DC-DC energy harvesters. These circuits effectively merge a low cold-start voltage requirement with a

remarkable high-frequency switching capability, further enhancing the efficiency and versatility of energy harvesting systems.

Employing a ring oscillator such as in Figure 38(a) to provide the required oscillation frequency for the charge pump is a strategic choice due to its ability to self-start using a small supply voltage (BOSE; ANAND; JOHNSTON, 2018). This characteristic is particularly advantageous in the context of energy harvesting systems, where the availability of initial power may be limited. By leveraging the self-starting capability of the ring oscillator, the energy harvesting system can effectively initiate its operation even when the supply voltage is relatively low, thereby enhancing its overall efficiency and reliability, especially during startup or in low-power conditions. This design consideration aligns with the objective of developing a robust and energy-efficient energy harvesting system, making the ring oscillator a suitable choice for fulfilling the oscillation frequency requirements of the charge pump in such applications.

The non-overlapping circuit in Figure 38(c) is an essential component in several systems such as switched capacitors (SC) (KARIMI et al., 2020). This circuit deliver two non-overlapping clock phases to control corresponding switches responsible for charging and discharging flying capacitors (SH et al., 2015). The non-overlapping circuit is comprised of logic gates that introduces a delay between signals originating from the ring oscillator. This delay is implemented to prevent short circuits when both signal phases are active. The circuit is positioned before the bootstrap inverter rather than preceding the charge pump as the signals are already swing-boosted, indicating an increased amplitude.

The clock booster circuit in Figure 38(b) is designed to increase the amplitude of two input antiphase clocks, which is necessary to power the non-overlapping circuit. To achieve this, two clock booster circuits are used to charge a voltage booster circuit in Figure 38(d), which generates a power output to charge the non-overlapping clock circuit. The non-overlapping circuit requires a higher amplitude clock signal to operate effectively, and the clock booster circuit provides the necessary boost to the amplitude of the clock signal being forwarded to the bootstrap inverter. This process ensures that the non-overlapping circuit operates correctly and prevents short circuits when both signal phases are active.

A bootstrapped CMOS inverter in Figure 38(e) is a type of CMOS inverter that uses a bootstrapping technique to improve its performance, particularly in terms of speed and power consumption (AL-DALOO; YAKOVLEV; HALAK, 2016). The bootstrapping technique involves using the output of the inverter to charge the gate of the next inverter, which can lead to faster switching times and lower power consumption (GARCIA; MONTIEL-NELSON; NOOSHABADI, 2006). The bootstrapped inverter receives the clock signal from the non-overlapping circuit and generates a boosted overlapped signal, which will be responsible for controlling the switches of the Dickson Charge Pump. This ensures that the Dickson Charge Pump operates efficiently and effectively, providing the

necessary power to the circuit. The clock booster circuit is a critical component in the overall operation of the circuit, ensuring that the non-overlapping circuit operates correctly and preventing short circuits when both signal phases are active.

The Dickson charge pump in Figure 38(f) assumes a pivotal role in energy harvesting systems, leveraging its capability to amplify the input voltage to reach a desired level, contingent upon the number of stages integrated into the charge pump circuit. As previously mentioned, the switches within the circuit are regulated by signals originating from the bootstrap inverter, while the capacitors facilitate the transfer of charges to the output, thereby enabling voltage boosting (MAHMOUD et al., 2019).

Overall, the integration of these components and the utilization of light energy harvesting through a PV cell demonstrate a comprehensive approach to developing an efficient energy harvesting system, enabling the capture and utilization of light energy to power electronic devices or systems.

5.2 COLD-START SIMULATION RESULTS

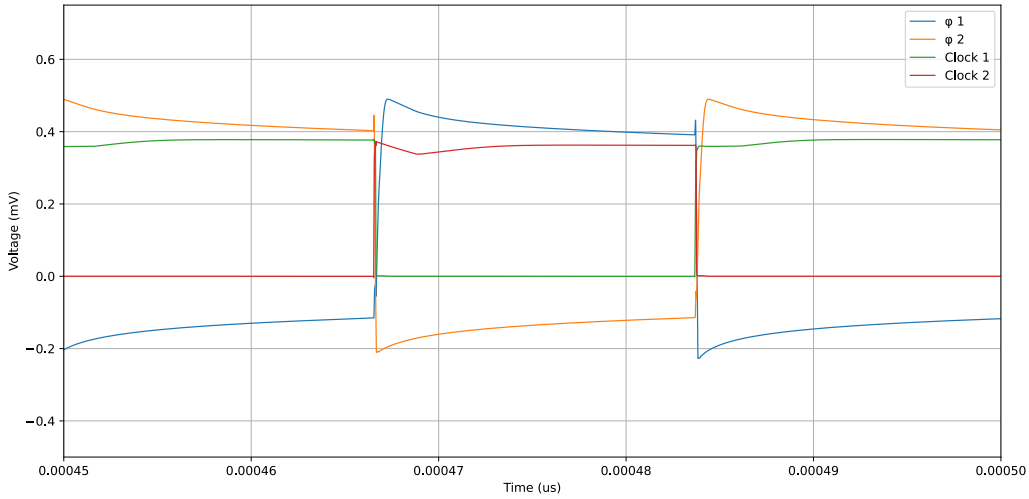
The cold-start circuit design underwent meticulous schematic-level simulation utilizing Spectre circuit simulator. Employing a comprehensive array of typical corner parameters and systematically varied resistive loads. Specifically, the simulation was customized to set up the photovoltaic (PV) cell model to receive incident light intensity equivalent to 500 lux, representing typical ambient lighting conditions. Consequently, the observed $V_{IN,PV}$ under these conditions measured 297.21 mV, while the output voltage (V_{OUT}) was recorded at 590.57 mV, resulting in a VCR of 1.98. The minimum input voltage generated by the PV cell at 50 lux was 172.53 mV. This precise evaluation aimed to provide nuanced insights into the circuit's behavior, ensuring its efficacy and reliability across a spectrum of real-world scenarios.

Figure 38(a) illustrates the seven-stage ring oscillator function at a frequency of 18.7 MHz. Notably, the design parameters of the inverters in the ring oscillator are finely adjusted to maximize performance. This precise setup guarantees that the inverters work at their best, enhancing the efficiency and operation of the oscillator circuit.

As depicted in Figure 38(b), the logic gates that constitue the non-overlapping circuit comprises five inverters, and two NAND logic gates. Operating in conjunction with the ring oscillator, the non-overlapping circuit incorporates an intermediary inverter for achieving a 180^o phase shift between signals. Figure 39 provides visual representation of the resulting clock signals generated by the non-overlapping circuit, alongside the phase signals produced by the bootstrap inverter. Furthermore, the output signals ϕ_1 and ϕ_2 are delivered with amplitudes spanning from -227 mV to 491.5115 mV, ensuring compatibility with downstream circuitry.

The voltage-boosting mechanism provides the non-overlapping circuit with an average voltage of 801.1 mV, a critical aspect in sustaining reliable operation within the

Figure 39 – Clock Signal and Phase Signal.



desired voltage range.

Using a load of 400 kΩ, the output voltage of the dickson charge pump is around 590.57 mV and the power delivery of arounf 17.57 nW. The sizing of the the MOSFET's and capacitors of the cold start circuit are detailed in table 6.

5.3 SWITCHED CAPACITOR CONVERTER

Switched capacitor converters are a key component in the modern energy conversion systems. They were originally designed to serve load circuits with extended active periods, addressing the challenge of maintaining energy efficiency when operating under low duty cycles. The efficiency of switched capacitor converters is influenced by differents factors, such as the conduction loss, the bottom plate parasitic capacitance, gate drive loss and control circuit overhead (EL-DAMAK; BANDYOPADHYAY; CHANDRAKASAN, 2013).

The switched capacitor converters offer a range of advantages including simplicity in implementation, compactness, and efficiencies exceeding 90%. They eliminate the necessity of inductors, reducing the converer size and lowering the electromagnetic interference (EMI), it also lower the cost when compared to a tradicional power converer topologies. Even with their high efficiency potential, the parameter selection is crucial for the optimal performance (LAPS, 2023).

5.4 SERIES-PARALLEL SWITCHED CAPACITOR CONVERTER CIRCUIT

The series-parallel switched capacitor converter in Figure 40, was chosen over other types os switched capacitor converter due to its specific advantages. This converter is

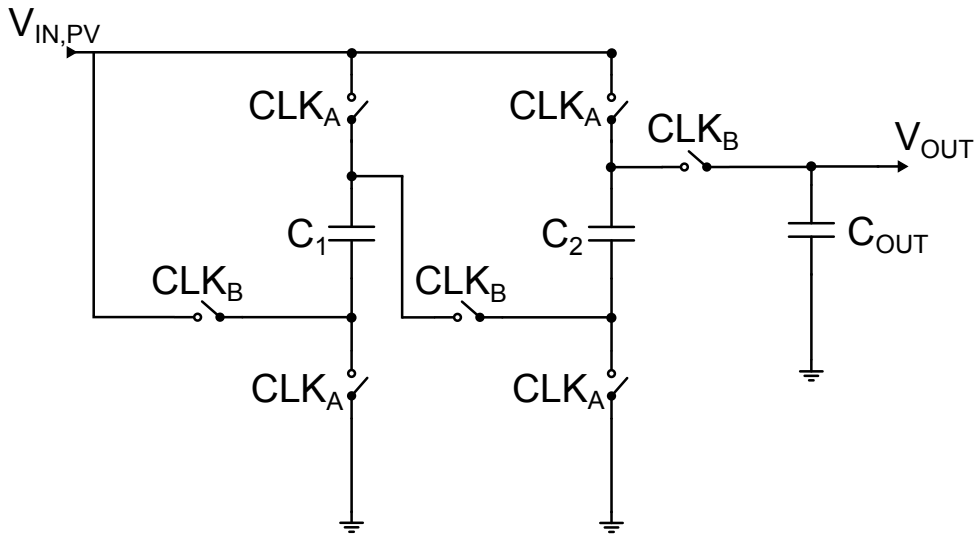
Table 6 – NMOS and PMOS Sizing

Circuit Block	W_N (nm)	L_N (nm)	W_P (nm)	L_P (nm)	Number of Finger (NMOS/PMOS)	Capacitor (F)
Ring Oscillator	500	60	1235	60	1/1	255.5 f
Clock-Booster	200/120	60	200	60	1/1	200 f
Non-Overlapping (NAND/INV)	400/200	60	480/480	60	1/1	N/A
Voltage-Booster	N/A	N/A	600	60	1/1	1.6 p
Bootstrap Inverter	200	60	600	60	1/8	100 f
Dickson Charge Pump (TG)	200	60	540	60	8/8	50 p (C_{fly})/ 10.500 n (C_{LOAD})
Inverter	200	60	480	60	1/1	N/A

easy to integrate into IC fabrication, cost-effective, and free from inductive noise elements. However, it cannot achieve 100% theoretical efficiency and is more complex than linear or switching regulators (HSIA; KIDD, 2019).

The series-parallel topology of this converter operates by connecting capacitors first in series and then in parallel, allowing for different conversion ratios based on the ratio of parallel chains used (HSIA; KIDD, 2019; SEEMAN, 2009).

Figure 40 – Switched Capacitor Converter Serie-Parallel.



As shown in section 4, the higher voltage at 500 lux is 297.14 mV, seeing that we want a output voltage of 500 mV, we need a voltage gain of approximately of 1.68.

A serie-parallel switched capacitor converter can be configured for multiple levels of voltage gain, depending on the architecture. we will use a 2-stage configuration to achieve a gain of 2. In one stage, the output voltage is approximately the sum of the inut voltages (series topology), and in another stage the capacitors are used to divide and stores charges.

The circuit is composed of capacitors and transmission gates. The capacitors that will accumulate and redistribute the charge. It better to choose capacitors with low equivalent series resistance (ESR) and sufficient capacitance to stabilize the output and minimize ripple. The transmission gates act as switches, controlling the conection of the capacitors in series or parallel.

The operation of a series-parallel converter is cyclic, alternating between two stages. Chage stage (Series Mode), where the capacitors are charged in series, where the output voltage is the sum of the input voltages. At the end of this stage, the voltage on the capacitors will be close to the input voltage multiplied by the number of capacitors. Transfer stage (Parallel Mode) where the capacitors are connected in parallel to transfer the charge to the output resulting in a higher output voltage.

In this case, for a gain of 1.68, it's possibel to use a two-capacitor switched architecture, where the input voltage of $V_{IN} = 297.14$ mV is doubled in one stage and

then adjusted to 500 mV.

The capacitors must be sized to ensure that the voltage ripple (variation in output voltage) is minimal. The voltage variation ΔV in a switched capacitor is given by equation 5.1.

$$\Delta V = \frac{I_{OUT} \cdot \Delta t}{C} \tag{5.1}$$

Where I_{OUT} is the output current, Δt is the switching time, and C is the capacitance.

The switching frequency f_{SW} affects the efficiency of the converter. Higher frequencies allow for smaller capacitors but increase switching losses. Based on the R*on* value of the transmission gates and the input voltage, we can define a reasonable frequency (typically in the range of 1 to 10 MHz for low-power circuits).

5.4.1 SWITCHING CYCLE IMPLEMENTATION

Cycle 1 (Charge-Series): During the charge-series phase, the flying capacitprs (C_1 and C_1) are configured to charge in series from the input source $V_{IN,PV}$, which in this work is 297.14 mV.

The switches actuated by CLK_A isolate the input and connect C_1 and C_2 in series between $V_{IN,PV}$ and ground. Specifically, one terminal of C_1 is connected to the input, its other terminal to C_2 to ground through the corresponding switch controlled by CLK_A. All other switches remain open to prevent alternate current paths (Van Breussegem; STEYAERT, 2013).

This series connection ensures the same current flows through both capacitors, enabling them to store charge simultaneously. The input voltage divides across the two capacitors, allowing to accumulate charge proportional to its capacitance (Van Breussegem; STEYAERT, 2013).

Ideally, both capacitors store equal charge, defined by equation 5.2, where C is the capacitance of each flying capacitor. In this mode, the sum of the capacitor voltages approaches the input voltage, considering perfectly matched capacitors and ideal switches (Van Breussegem; STEYAERT, 2013).

$$Q_1 = Q_2 = C \cdot V_{IN,PV} \tag{5.2}$$

The series connection in the charge phase is pivoltal for setting up the subsequent voltage boost in the discharge phase. The energy retained on each capacitor provides the basis for increased output voltage during (Van Breussegem; STEYAERT, 2013).

Cycle 2 (Discharge-parallel): Upon entering the second phase, the topology reconfigures so that C_1 and C_2 can discharge in parallel to the output node (Van Breussegem; STEYAERT, 2013).

Clock CLK_B closes the switches that connect both capacitors previously charged terminals to the output node (V_{OUT}), and their other sides to ground. This parallel configuration doubles the effective capacitance available to support the load, permitting more efficient charge transfer (Van Breussegem; STEYAERT, 2013).

The charges stored on C_1 and C_2 are combined and rapidly delivered to the output capacitor (C_{OUT}). The output node sees the sun of both capacitors charge, boosting the output voltage (Van Breussegem; STEYAERT, 2013).

The output peak voltage during parallel discharge is calclated using equation 5.3, under idela circumstances, the voltage is doubled relative to each capacitor's charge, and the total transfered charge raises the output quickly (Van Breussegem; STEYAERT, 2013).

$$V_{OUT,peak} \approx \frac{Q_1 + Q_2}{2 \cdot C} \tag{5.3}$$

Simulations measurement validate that, given an input of 297.14 mV, the output can reach up to 500 mV during efficient cycle operation. This result highlights the topology's suitability for stepping up low input voltages in integrated applications (Van Breussegem; STEYAERT, 2013).

The effectiveness of this two-phase approach derives from the core charge-pump principle, by charging capacitors in series and discharging them in parallel, it is possible to achieve a voltage multiplication effect.

5.4.2 SWITCH TOPOLOGY WITH LOW SERIES RESISTANCE

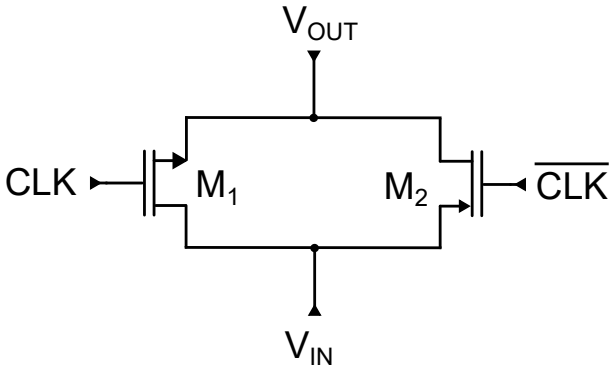
To ensure that the PV cell operates near its maximum power point (MPP), it is crucial to design the switching circuit in a way that minimizes power loss. This requires the switch to have the lowest possible resistance, preventing excessive power drainage from the PV cell.

The switch used in this design is a transmission gate, as shown in Figure 41. A transmission gate is a widely used circuit for controlled signal transmission, consisting of complementary MOS transistors (NMOS and PMOS) connected in parallel. This configuration allows for efficient bidirectional signal flow with minimal resistance. Transmission gates are commonly employed in applications such as multiplexers, flip-flops, and low-power logic circuits.

To design a transmission gate, first it necessary to understand it's basic circuit, the NMOS transistors conduct when the control voltage is high (logical 1), and the PMOS transistor conducts when the control voltage is low (logical 0).

These transistor are connected in parallel, and their gates are connected to complementary control signals. When one is activated, the other is also activated, allowing the transmission of an input signal to the output. The gate of the NMOS transistor receives the control signal directly while the gate of the PMOS transistor receives the complemented control signal.

Figure 41 – Transmission Gate



Typically, PMOS has lower electron mobility than NMOS, which means that the width (W) of PMOS needs to be larger to match the on-resistance (R_{on}) of both transistors. Usually, the width of the PMOS (W_{PMOS}) is two to three times larger than that of the NMOS (W_{NMOS}) to balance the performance.

The resistance of the transmission gate in the conducting state, also known as "on-resistance" (R_{ON}), is given by equation 5.4.

$$R_{on} = \frac{V_{OUT} - V_{IN}}{I_{IN}} \tag{5.4}$$

where and represent the output and input voltages of the switch, respectively, and is the current flowing through it.

Figure 42 presents the relationship between the voltage drop across a MOSFET switch and its corresponding R_{ON} for a fixed device width of 30 μm. The data shows a near-linear increase in voltage drop as R_{ON} rises, with the voltage across the switch reaching values as high as approximately 175 Ω. This indicates that the effective switch resistance directly contributes to voltage losses during operation. Minimizing R_{ON} through device sizing is therefore imperative to reducing power dissipation and enhancing overall converter efficiency (KESTER; ERISMAN; THANDI, 1998).

Extending the analysis, Figure 43, provides a three-dimensional surface visualization illustrating how R_{ON} varies the Wn rangin from 10 μm to 30 μm and the Wp ranging from 24 μm to 72 μm, simultaneously and voltage across the switch (0 to 1.2 mV). The plot revels a pronounced peak in R_{ON} between approximately 0.4 mV and 0.6 mV voltage drop, with the magnitude of this peak decreasing as device size increases. Larger device widths inherently exhibit lower peak R_{ON} due to improved channel conduction capabilities.

Notably, beyond the peak voltage region, R_{ON} sharply descreases, indicating enhanced efficiency at operating voltages above this threshold. This behavior underscores a crucial design trade-off, while increasing transistor size reduces conductions losses (lower R_{ON}), it also incurs area and switching capacitance penalties which can adversely impact switching speed and dynamic power consumption (KESTER; ERISMAN; THANDI, 1998).

Figure 42 – R_{ON} of the CMOS switch for the SC Converter

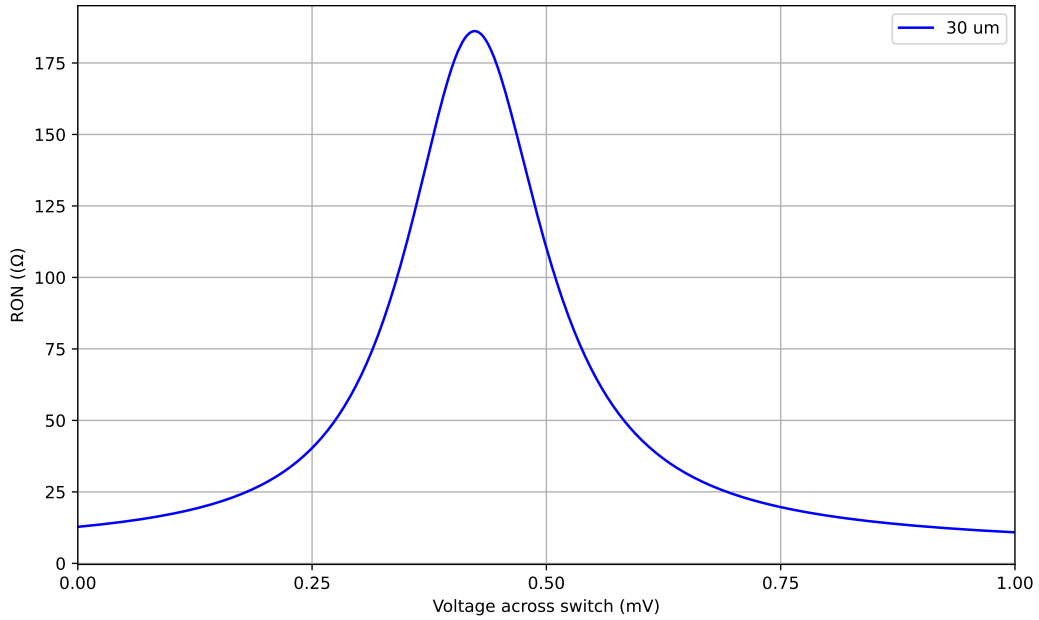
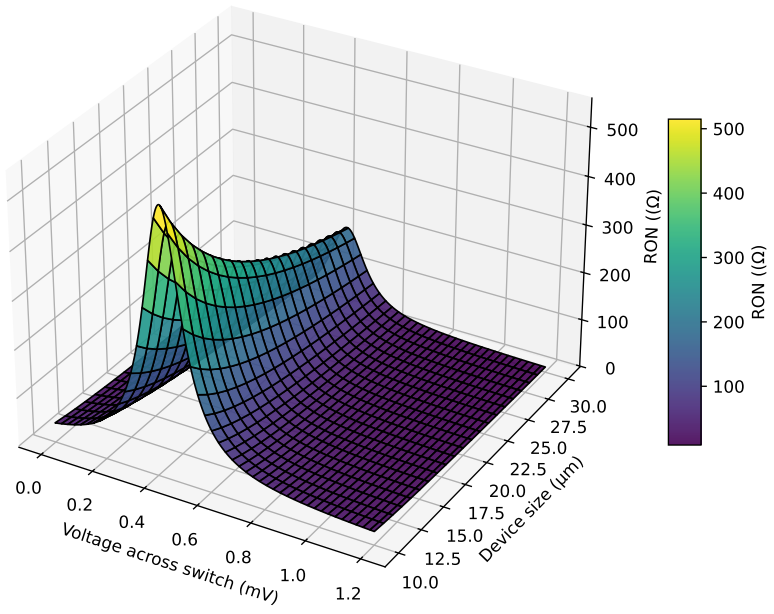


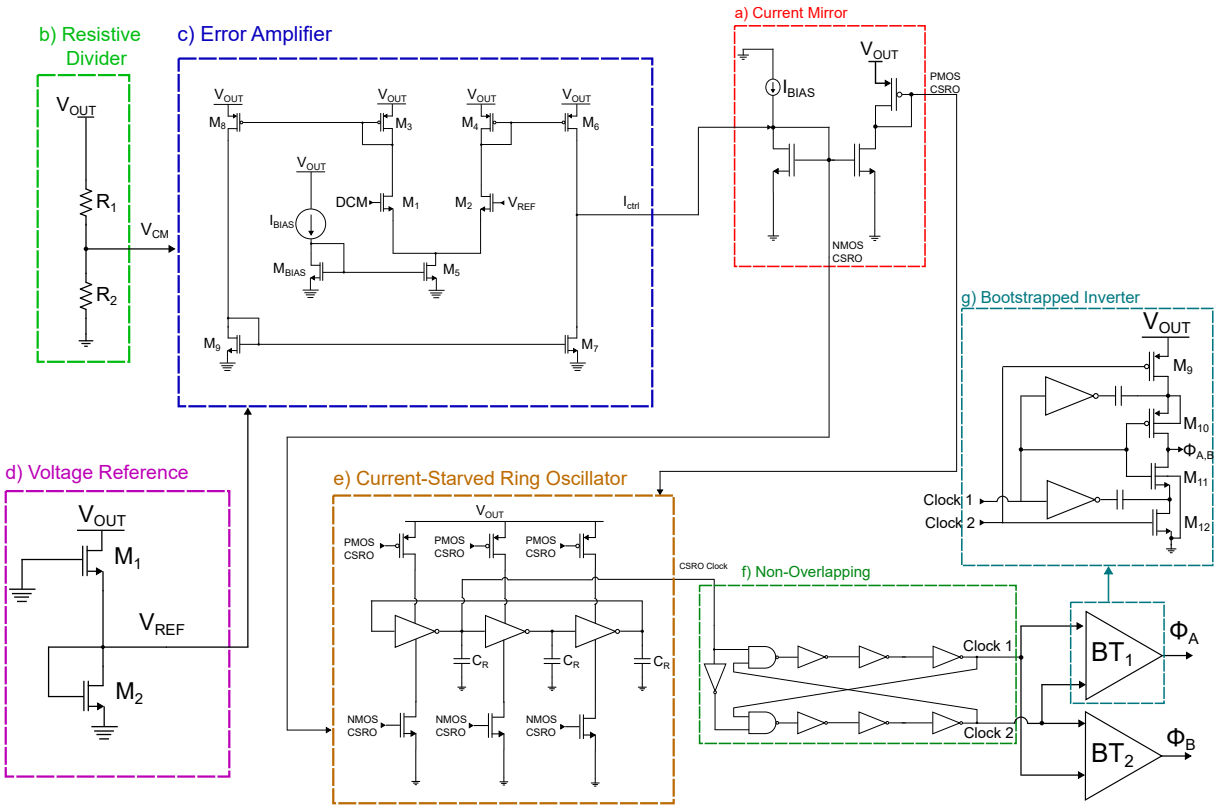
Figure 43 – Dependence of switch R_{ON} on voltage drop and device size in CMOS SC converter



5.5 CONTROL CIRCUIT

Following the establishment of a stable power supply voltage facilitated by the cold-start circuit, the subsequent critical phase entails the meticulous design and implementation of the control circuit. This circuit assumes responsability for crucial functions including voltage referencing, current regulation by means of the error amplifier and the current mirror, and the precise generation of the clock signal. The control block, depicted in Figure 44, embodies a sophisticated array of components, notably featuring a three-stage current-starved ring oscillator (CSRO) as its cornerstone. This CSRO is tasked with generating the essential clock signal,

Figure 44 – Control Circuit.



5.5.1 ERROR AMPLIFIER

The error amplifier circuit under study, depicted in Figure 45, is implemented using a CMOS transistor topology optimized for low power consumption and stable operation. The amplifier employs differential input pairs, labeled M_1 and M_2, along with active load transistors (M_3, M_4, M_6, M_7, M_8 and M_9), and a dedicated biasing transistor (M_{BIAS} and M_5), which collectively define the amplifier's gain, bandwidth, and power characteristics.

The operational principle relies on the push-pull configuration of MOSFETs operating in weak inversion (subthreshold) region. In this regime, the gate-to-source

voltage (V_{GS}) is below the threshold voltage (V_{th}), resulting in exponentially dependet drain current (I_D) as described by the relation in Equation 5.5 (BARIK; RAMKUMAR, 2024).

$$I_D = I_{D0} \cdot (\frac{W}{L}) \cdot exp(\frac{q \cdot V_{GS}}{n \cdot k \cdot T}) \tag{5.5}$$

Where I_{D0} is a characteristic current, and n is the slope factor. This mode of operation enables very low bias currents and thus reduces power consumption substantially, which is essential in energy harvesting applications (BARIK; RAMKUMAR, 2024).

The simulation results demonstrate the following performance parameters, summarized in table 7.

Table 7 – Error Amplifier Simularions Results

Gain	18.89 dB
Phase Margin	84.10^o
GBW	2.111 MHz
Power Analysis	652.1 ηW
Slew Rate	0.4 V/μs
CMRR	48.28 dB

The gain is approximately 18.89 dB corresponding to a voltage gain factor of about 8.7, primarily determined by the transconductance of the differential pair (M_1, M_2) and the output resistance of the active loads (M_6, M_8) according to the Equation 5.6 (BARIK; RAMKUMAR, 2024).

$$A_v = g_{m2}(r_{ds2}||r_{ds4}) \cdot (g_{m6} + g_{m8}) \cdot (r_{ds6||r_{ds7)}} \tag{5.6}$$

The Phase margin of 84.10^o, indicates stable operation resulting from the presence of a dominant single pole, managed principally by transistor M_5 and compensation capacitances (BARIK; RAMKUMAR, 2024).

The gain-bandwidth product (GBW) is 2.111 MHz represents the frequency range over which the amplifier maintais gain, depending on the bias current through M_{BIAS} and load capacitance as expressed in Equation 5.7.

$$GBW = \frac{g_{m1}}{2 \cdot \pi \cdot C_L} \tag{5.7}$$

A low simulated power consumption of 652.1 ηW, enabled by subthreshold biasing currents and appropriate transistor sizing (BARIK; RAMKUMAR, 2024).

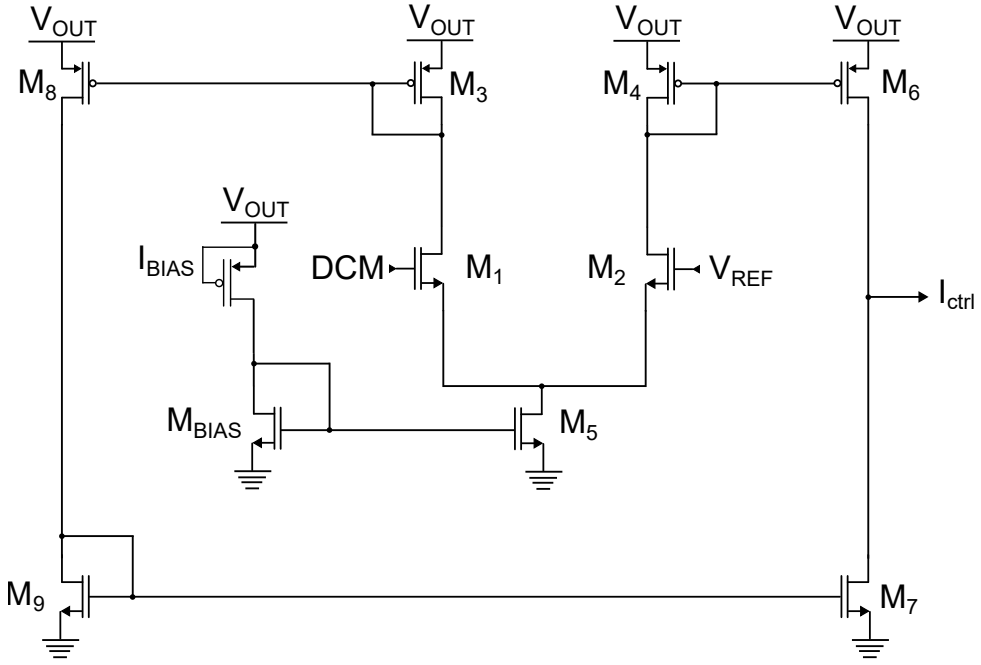
A slew Rate of 0.4 V/μs, is limited by the maximum current available to charge and discharge the output stage capacitance, set via current mirrors involving transistors M_8 and M_9 (BARIK; RAMKUMAR, 2024).

Common-mode rejection ratio (CMRR) of approximately 48.28 dB reflects the differential input pair's ability to reject common-mode noise, based on transistor matching and offset voltage control (BARIK; RAMKUMAR, 2024).

The transistor-level schematic of Figure 45 clearly maps the roles of each transistors stage: the input differential pair (M_1, M_2), active loads (M_3, M_4), output current mirrors (M_6, M_7, M_8, M_9), and bias control (M_5, M_{BIAS}). The simulation results align well with theoretical models and provide strong evidence of the circuit's potential for low-power, stable error amplification in analog feedback systems (BARIK; RAMKUMAR, 2024).

The error amplifier in Figure 45 functions essentially as a differential amplifier that compares the output voltage of the DC-DC switched converter to a reference voltage. The resulting error signal biases a current mirror, which modulates the NMOS and PMOS transistors of a current-starved ring oscillator (CSRO). In this configuration, the error amplifier plays a critical role in regulating the CSRO's switching frequency based on the converter's output voltage.

Figure 45 – Error Amplifier.

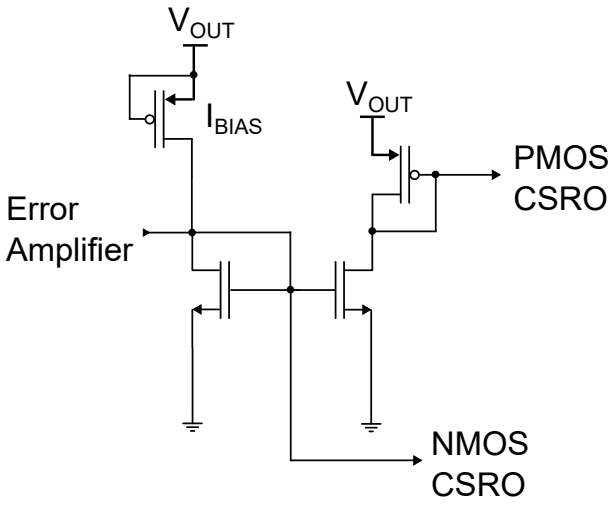


5.5.2 CURRENT MIRROR INTERFACE AND MODULATION OF CURRENT-STARVED RING OSCILLATOR (CSRO)

The output signal of the error amplifier is an analog voltage or current that requires conversion into a control current to regulate the oscillation of the CSRO whithin the DC-DC converter system. This conversion is effectively performed by a current mirror circuit, a fundamental building block in analog CMOS design.

A current mirror is a circuit configuration that copies or mirrors a reference current through one active device, typically a MOSFET, to another device, providing a

Figure 46 – Current Mirror



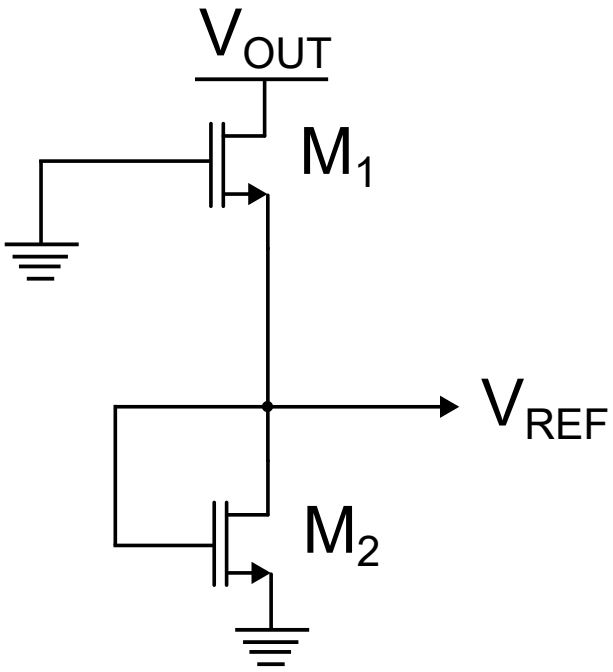
stable and proportional output current. The primary function of the current mirror in this context is to translate the error amplifier's output into a bias current that controls the NMOS and PMOS transistors of the CSRO. By modulating this bias current, the switching frequency of the CSRO can be dynamically adjusted to maintain the desired output voltage regulation (GRAY et al., 2024), (BARIK; RAMKUMAR, 2024), (RAZAVI, 2016).

Figure 46 illustrates a typical current mirror connection between the error amplifier output and the CSRO input stage. The current provides a high output impedance, ensuring the bias current is stable and largely independet of output voltage variations, an accurate current replication, maintaining the linearity of the control signal, compatibility with subthreshold operation to preserve low power consumption, consistent with the system's design goal (ALLEN; HOLBERG, 2002), (VITTOZ; FELLRATH, 1977).

The current-starved aspect of the ring oscillator implies that the delay elements of the oscillator are biased by limited currents. By controlling the magnitude of these currents through the current mirror, the charging and discharging times of the oscillator nodes are regulated, effectively controling the oscillation frequency (BARIK; RAMKUMAR, 2024), (GRASSO et al., 2015).

Designing this current mirror involves careful matching to minimize errors, operation within the subtreshold region to maintain ultra-low power, and minimizing voltage headroom to optimize dynamic range and linearity (GRAY et al., 2024), (RAZAVI, 2016). The integration of the current mirror as the interface stage effectively bridges the analog feedback output and the frequency control input which is paramount for the overall regulation performance of the switched-capacitor converter.

Figure 47 – Voltage Reference circuit



5.5.3 VOLTAGE REFERENCE AND RESISTIVE DIVIDER

A well-regulated and stable reference voltage is a critical component in analog integrated circuits, providing a baseline agaist which other signals are measured or controlled. In the context of the error amplifier and DC-DC converter system, the voltage reference cicuit generates a stable voltage (denoted as R_{REF} in Figure 47) that serves as a comparison point for the output voltage V_{OUT}. The error amplifier detects deviations between these voltages and generates an appropriate error current or voltage to regulate the system (RAZAVI, 2016).

Voltage reference circuits provide a constant voltage output largely independet of supply voltage, temperature, and process variations (GONZALEZ; ALLEN, 2006). Common voltage reference design include bandgap references, subthreshold MOSFET based references, and low-dropout (LDO) regulator output reference voltages (MEGAW, 2008).

Bandgap references exploit the complementary temperature coefficients of the base-emitter voltage of bipolar junction transistors and a proportional-to-absolute-temperature voltage to generate temperature-independent voltages, typically around 1.2 V (RAZAVI, 2016; Renesas Technology Corp., 2005). Although widely used, they can consume moderate power and area, which might be unsuitable for ultra-low power indoor energy harvesting.

Subthreshold MOSFET voltage references utilize the exponential current-voltage relationship in weak inversion for low power but may require careful design to compensate temperature and process effects (CHIA, 2008).

In low-voltage, low-power system such as indoor energy harvesting, the choice of voltage reference is often a tradeoff between stability, power consumption, and implemen-

tation simplicity.

A 2-Transistor Voltage Reference circuit is a simple and compact circuit design used to generate a stable reference voltage with low power consumption and small silicon area. It typically uses two MOS transistors operating in the weak inversion (subthreshold) region, where the gate-source voltages and threshold voltage differences of the transistors are exploited to create a voltage that is relatively independent of supply voltage and temperature variations. The circuit achieves temperature compensation by balancing the complementary-to-absolute temperature (CTAT) behavior of the threshold voltage with the proportional-to-absolute temperature (PTAT) component from the thermal voltage. This design can operate at ultra-low voltages, often below 1V, making it suitable for low-power and ultra-low-power applications such as RFID and sensor systems. Its simplicity and effectiveness make it an attractive choice for integrated circuit design where minimizing power and area while maintaining a stable reference voltage is critical (SEOK et al., 2012; OLMOS et al., 2015)

A resistive voltage divider is a simple passive network used to generate a scaled-down version of an input voltage. It consists of two resistors connected in series between the input voltage V_{OUT} and ground, with the output taken from the junction node between the resistors. The output voltage V_{CM} is given by Equations 5.8.

$$V_{CM} = V_{OUT} \cdot \frac{R_2}{R_1 + R_2} \tag{5.8}$$

Where R_1 is connected to V_{OUT}, and R_2 is connected to ground.

In the context of an error amplifier, the resistive divider is used to furnish the reference voltage V_{REF} from a higher stable voltage source. It is important to choose the resistor values carrfully to minimize power consumption (large resistor value) while maintaining signal integrity and noise performance (small resistor value reduce thermal noise and offset) (GONZALEZ; ALLEN, 2006; CASAÑAS et al., 2022).

In the error amplifier schematic depicted in Figure 45, the transistor M_1 receives the feedback voltage V_{CM} scaled from the output voltage V_{OUT}. This transsistor, as part of the input differential pair with transistor M_2, compares the feedback signal agaist the stable reference voltage V_{REF}, provided by the voltage reference circuit, is applied to the gate of M_2. The differential pair's resulting current difference controls the subsequent amplification stages, producing the control current I_{ctrl} that regulates the converter output.

Design optimization ensures that the reference voltage remains stable under varying supply voltages and temperature, and that the resistive divider introduces minimal loading and noise to sensitive amplifier input (RAZAVI, 2016; MEGAW, 2008)

5.5.4 CURRENT-STARVED RING OSCILLATOR

The current-starved ring oscillator (CSRO) depicted in Figure 48, represent a significant class of voltage-controlled oscillators (VCO) widely employed in integrated

circuit design for the generation of clock signals and frequency references. These oscillators operate by forming a ring of inverters, where the delay introduced by each inverter stage dictates the overall oscillation frequency. Notably, in CSRO cicuits, this delay can be controlled by voltage, offering a versatile means of fequency modulation and adjustment (HUQ et al., 2021; SUMAN; SHARMA; GHOSH, 2016).

To design a 3-stage CSRO that generates the specific frequencies for the parallel-serie switched capacitor converter it will be necessary to calculate the oscillation frequency using the Equation 5.9.

$$f = \frac{1}{2 \cdot N \cdot T_{delay}} \tag{5.9}$$

Where N is the number of stages, and T_{delay} is the delay of each inverter stage. It will be necessary to adjust the current (bias current) that control the delay of each stage to achieve the desired frequencies.

The delay per stage is directly related to the desired frequencies. For each frequency, it can be calculated using the Equation 5.10.

$$T_{delay} = \frac{1}{2 \cdot N \cdot f} \tag{5.10}$$

In a current starved ring oscillatorr, each inverter's delay is controlled by the current flowing through it. This current is set by the transistors placed in series with the pull-up and pull-down networks of each inverte. The delay of each inverter can be modeled by Equation 5.11.

$$T_{delay,inv} \approx \frac{C_R \cdot V_{OUT}}{I_{REF}} \tag{5.11}$$

Where the C_R is the load capacitance at each inverter node, V_{OUT} is the supply voltage, and I_{REF} is the current controlling the charging and discharging of C_{LOAD}.

To switch between the different target frequencies, you can implement a digitally controlled current source or a current mirror with biasing. This will allow the bias current I_{BIAS} to be set dynamically, thereby adjusting the frequency of the CSRO.

5.5.5 NON-OVERLLAPING CIRCUIT

The non-overlapping circuit depicted in Figure 49 generate the clock signals that are essentials in SC circuits, where two (or more) phases control the switches for charge transfer. These signals are designed so that during the transitions from one phase to another, both phases are momentarily low, ensuring that switches controlled by different phases are never ON simultaneously. This prevents charge sharing, signal corruption, and reduces clock feedthrough errors (AGARWAL; AGARWAL, 2021)

The typical implementation uses delay elements and logic gates to produce two clocks with a guaranteed non-overlapping interval,

Figure 48 – Current-Starved Ring Oscillator.

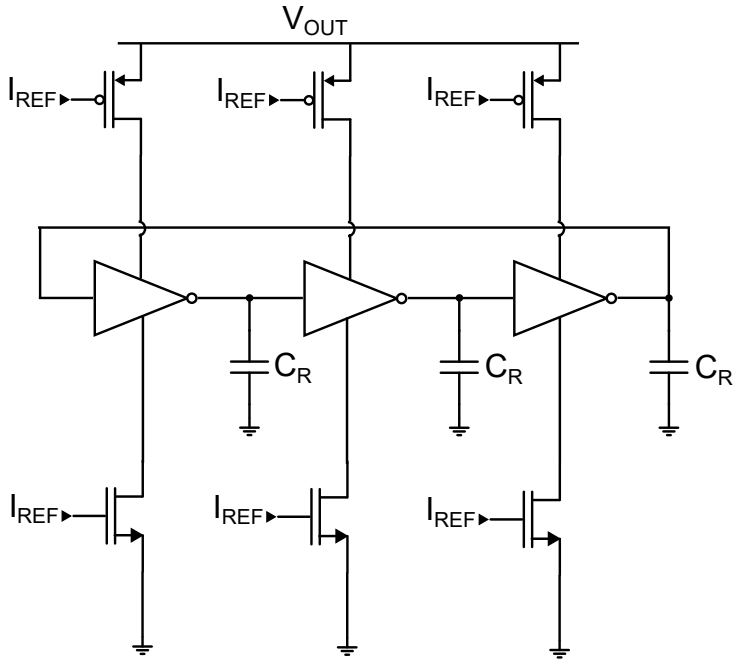
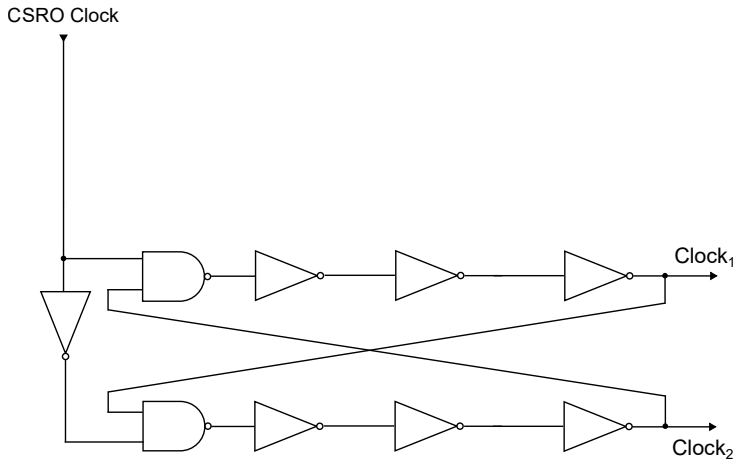


Figure 49 – Non-Overlapping circuit

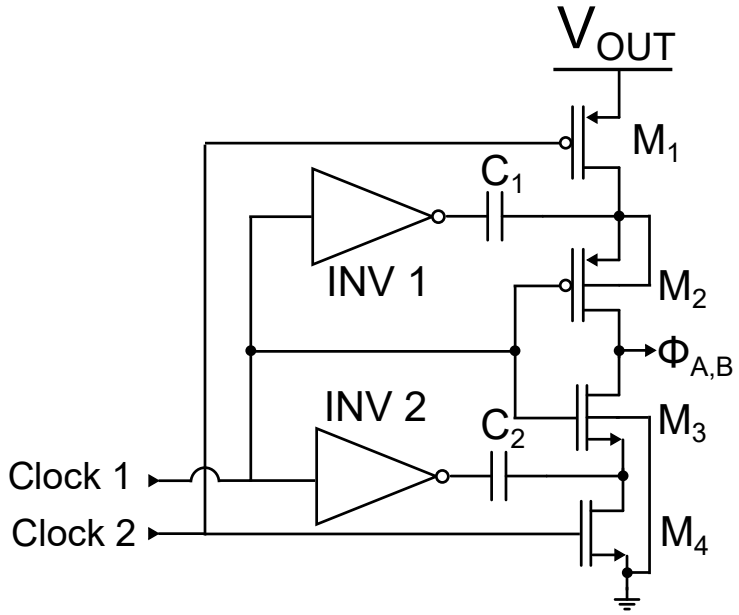


The width of the non-overlap interval must be carefully tuned: too small, and switches may overlap; too large, and throughput is unnecessarily limited. Patented solutions focus on optimizing the delay to maximize operating frequency while retaining safe operation for the SC cells (GARRITY; RAKERS; EBERHARDT, 1998).

5.5.6 BOOTSTRAPPED CIRCUIT

Transmission gates (series connection of NMOS and PMOS switches) require sufficient gate overdrive for low on-resistance and minimal distortion. In many cases, especially at low supply voltages, conventional gate driving is inadequate. A bootstrap circuit addresses this by dynamically boosting the gate voltage of the transmission gate switches to maintain a high gate-to-source voltage during operation (Analog Devices, Inc., 2012; STMicroelectronics, 2022).

Figure 50 – Bootstrap Circuit



A typical bootstrap circuit, as depicted in Figure 50, uses capacitive coupling and clocked inverter logic, During the clock phase Clock 1, capacitor C_1 is charged from the supply through inverter INV1 and transistor M1, when $Clock_2$ is activated, C_2 and INV2 similarly charge M2. The clever sequencing of non-overlapping of $clock_1$ and $clock_2$ ensures that no path directly connects the supply and ground at any instant, while the charge stored in C_1 and C_2 boosts the gate voltage at the switch stack (M3/M4), resulting in a gate voltage V_ϕ higher than the supplied by the non-overlapping. (Analog Devices, Inc., 2012).

This raises the effective gate-to-source voltage, substantially reducing switch resistance and improving linearity. The arrangement also minimizes signal-dependent charge injection and ensures high-fidelity charge transfer, vital in precise SC applications (RAZAVI, 2015).

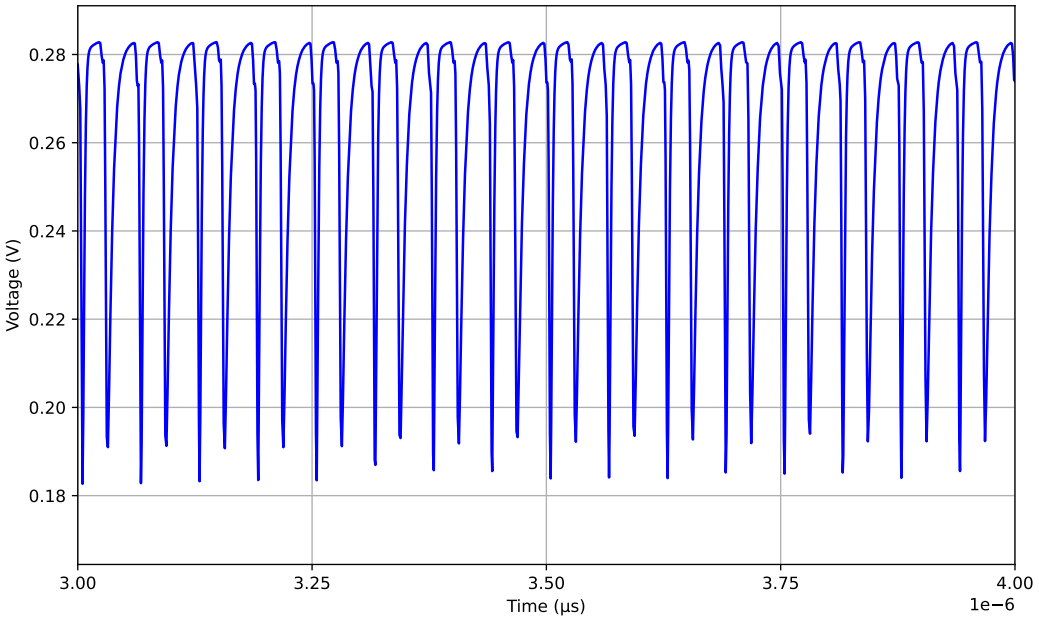
5.6 SIMULATION RESULTS

Figure 51 presents the transient voltage waveform of the photovoltaic (PV) cell module over a 1 µs interval. The PV cell output voltage ranges between approximately 0.18 V and 0.28 V, demonstrating stable operation within the expected voltage range for indoor light energy harvesting applications The power analysis of the PV cell result in a power delivery of approximatelly 28.09 μW.

The waveform is characterized by a smooth voltage profile with minor fluctuations, indicative of typical variations in output caused by changes in illumination levels or load conditions. The relatively steady voltage confirms the PV cell's ability to provide a consistent input source for the switched-capacitor energy harvesting system.

The low output voltage underscores the necessity for efficient voltage boosting

Figure 51 – Photovoltaic Cell wave form



and conversion stages, such as the bootstrap and switched-capacitor DC-DC converters, to achieve usable supply voltages for integrated circuits operating at ultra-low power.

The stability and amplitude of the PV cell output observed here validate its suitability as a primary energy source for the designed harvesting system, aligning with targeted input voltage levels in subsequent converter stages.

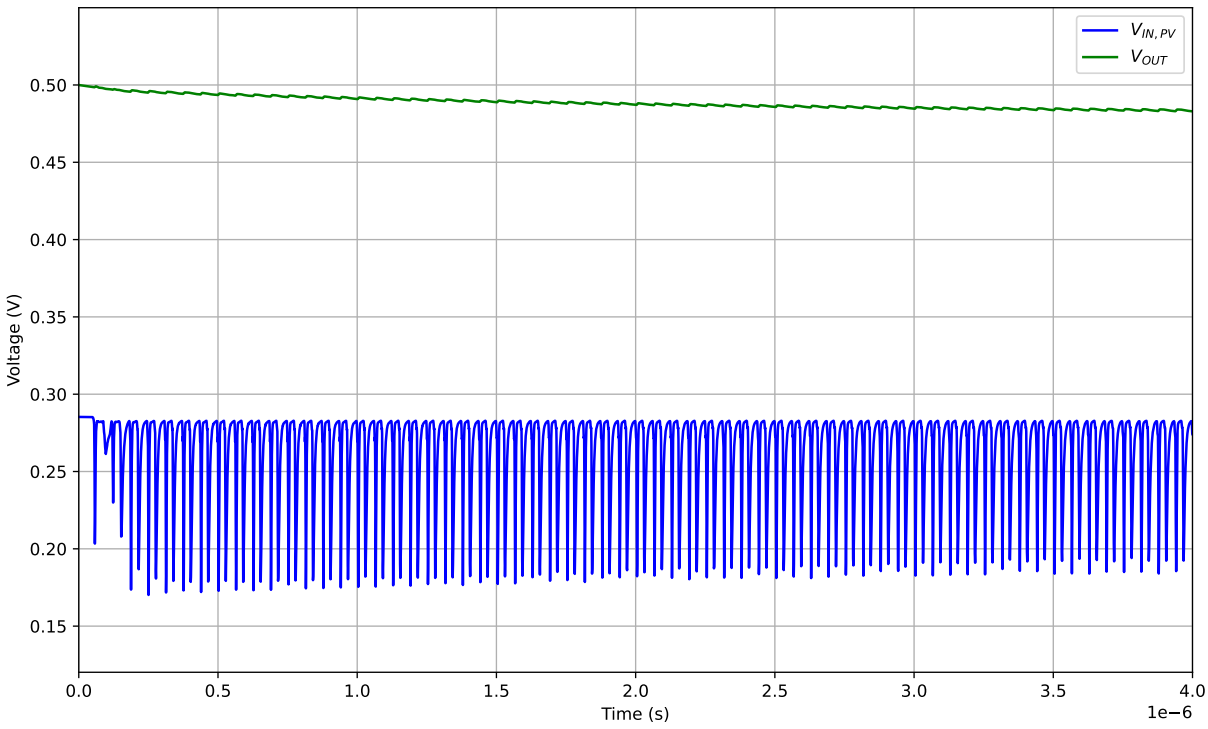
Figure 52 shows the transient voltage waveform at the output of the parallel-series switched-capacitor converter operating in a voltage multiplication mode over a 1 µs time interval. The output voltage ranges between approximately 0.48 V and 0.50 V, indicating a successful step-up conversion from the lower input voltage levels typical of photovoltaic energy harvesting.

The waveform exhibits stable oscillations with clear and well-defined transitions, demonstrating effective charge transfer and minimal loss during the switching process. The relatively low ripple amplitude confirms the high efficiency and fast response of the converter topology.

This stable output voltage is essential for powering subsequent low-voltage circuits in energy harvesting systems, as it elevates the harvested energy to usable levels while maintaining low noise and distortion. The results validate the designed switched-capacitor converter's capability to reliably perform voltage multiplication in an integrated system. The dissipated power of the switched capacitor is 883.63 nW, with a resistive load of 150 kΩ and a capacitive load of 1nF.

Figure 53 illustrates the transient waveform of the clock signal generated by the

Figure 52 – PV cell and parallel-series switched capacitor converter output wave form



Current Starved Ring Oscillator (CSRO) over a 1 µs time interval and is operating at a frequency of 16.02 MHz. The CSRO is responsible for producing the oscillation frequency that drives the non-overlapping clock circuitry and subsequently the bootstrap circuit in the switched-capacitor system.

The waveform exhibits a stable and periodic square wave with a peak-to-peak voltage of approximately 0.4 V, which corresponds to the supply voltage level used in the oscillator design. The rising and falling edges are well-defined and consistent over the observed time span, indicating low jitter and precise timing control, crucial for reliable clock generation in ultra-low power switched-capacitor circuits.

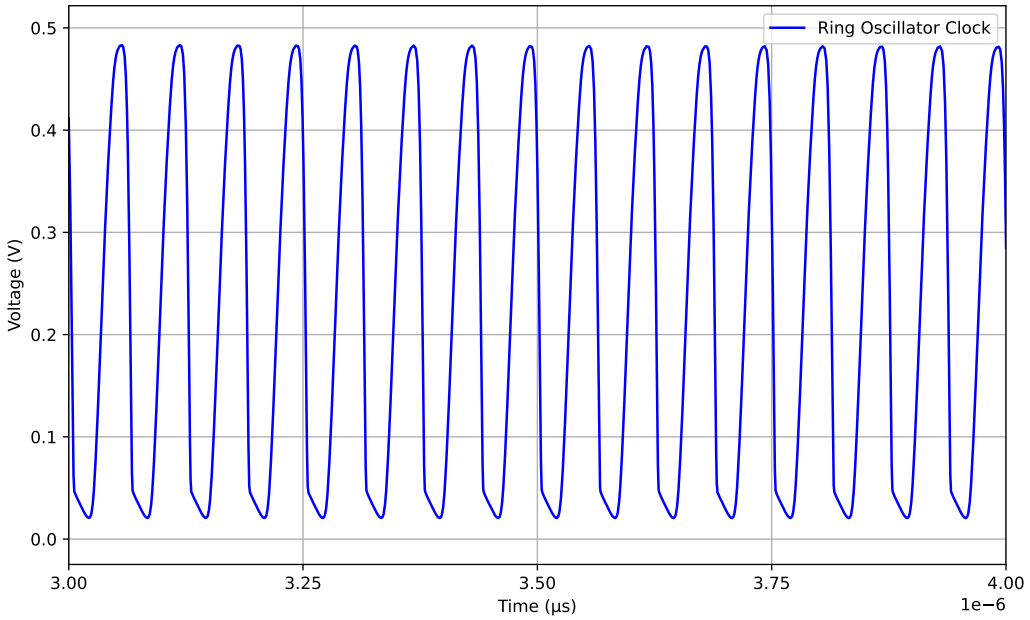
The current starving mechanism effectively regulates the charging and discharging currents of the inverter stages, allowing fine control over the oscillation frequency through an external bias. This results in a tunable clock source capable of adapting to varying load conditions and power constraints.

The clean waveform and sharp transitions demonstrate the proper functionality of the CSRO, validating its suitability as a clock source in the designed energy harvesting switched-capacitor converter system.

Figure 54 presents the transient voltage waveforms of the generated non-overlapping clock signals, labeled Clock 1 and Clock 2, over a 0.20 μS time interval. These signals are the input clocks driving the bootstrap circuit and switched-capacitor switches.

The non-overlapping interval, visually evident as the temporal gap between the falling edge of Clock 1 and the rising edge of Clock 2—and vice versa—ensures reliable

Figure 53 – Current Starved Ring Oscillator wave form



switch operation by mitigating charge sharing and short-circuit risks.

Both waveforms maintain stable amplitudes, peak at around $0.4 \approx 0.5$ V, and possess sharp transitions with minimal overshoot or ringing. These characteristics are critical for minimizing timing uncertainties and ensuring consistent charge transfer in switched-capacitor circuits.

The successful generation of clean, non-overlapping clock signals confirms the efficacy of the clock generation circuitry and sets the foundation for the bootstrap stage and overall SC converter performance.

The waveforms exhibit distinct high and low phases with timing control, clearly demonstrating the engineered non-overlapping interval between them. At no point do the two clocks overlap in their high states, effectively preventing simultaneous conduction of transmission gate switches controlled by these signals.

Figure 55 shows the plot of the two bootstrapped clock waveforms generated by the bootstrap circuit under test. The waveforms ϕ_1 and ϕ_2 illustrate the voltage signals over a time interval of 0.20 μs.

The transient dynamics of the waveforms reveal well-defined rising and falling edges with minimal overshoot or ringing, which is critical for ensuring fast switch actuation and reliable timing margins in switched-capacitor circuits. The similarity of both waveforms suggests good repeatability and circuit robustness.

Minor variation in amplitude and transition timing between ϕ_1 and ϕ_2 could arise from inherent circuit parasitics or simulation tolerances, yet these differences are within

Figure 54 – Signals Clock 1, and Clock 2 from the Non-Overlapping clock circuit

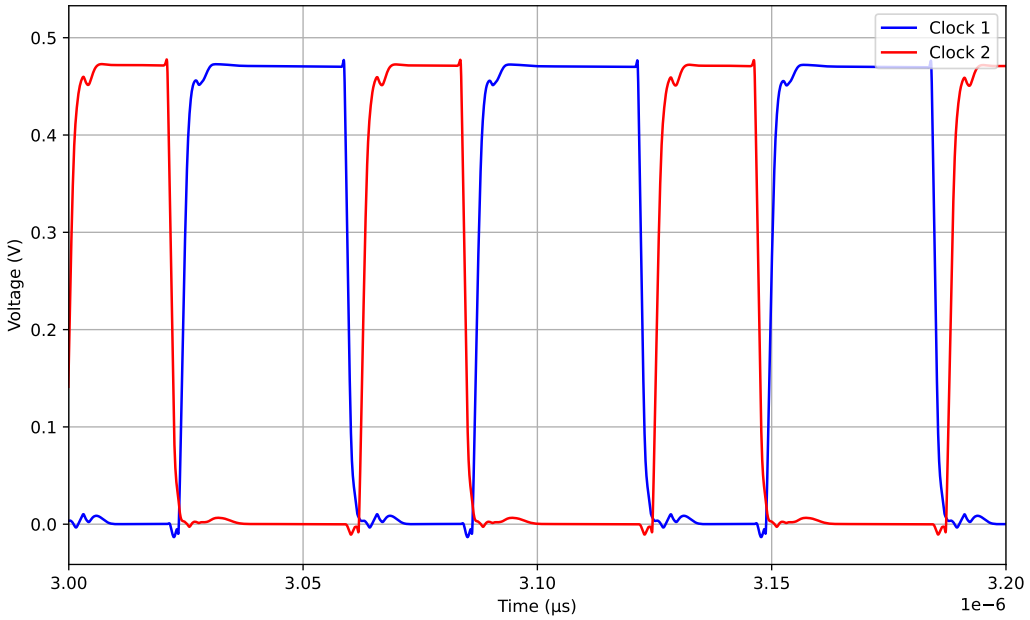
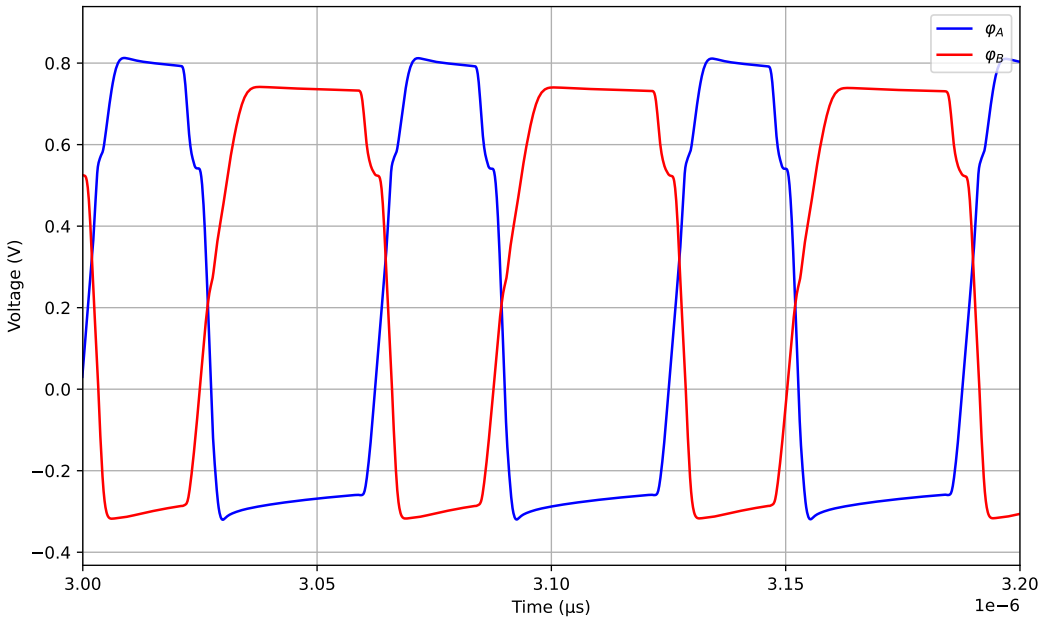


Figure 55 – Signals ϕ_1 and ϕ_2 from the bootstrapped inverter circuit



acceptable boundaries and do not impair overall functionality.

These results validate the bootstrap circuit's capability to produce stable, high-quality clock signals suitable for driving low-resistance, linear transmission gates essential

in precision switched-capacitor applications.

Figure 56 illustrates the transient waveforms of the non-overlapping input clocks Clock 1 and Clock 2, together with the output bootstrap clock signal $\mathrm{CLK}_{\phi 1}$. As shown, CLK_A and CLK_B maintain a clear non-overlapping interval preventing concurrent activation of switches. The bootstrap output $\mathrm{CLK}_{\phi 1}$ achieves a voltage amplitude that exceeds the nominal supply voltage V_{OUT} by approximately 200 mV, consistent with theoretical expectations based on capacitive charge coupling through C_1 and C_2.

Figure 56 – Signals ϕ_1 andϕ_2 from the bootstrapped inverter with Clock 1 and Clock 2 as input from the non-overlapping clock circuit.

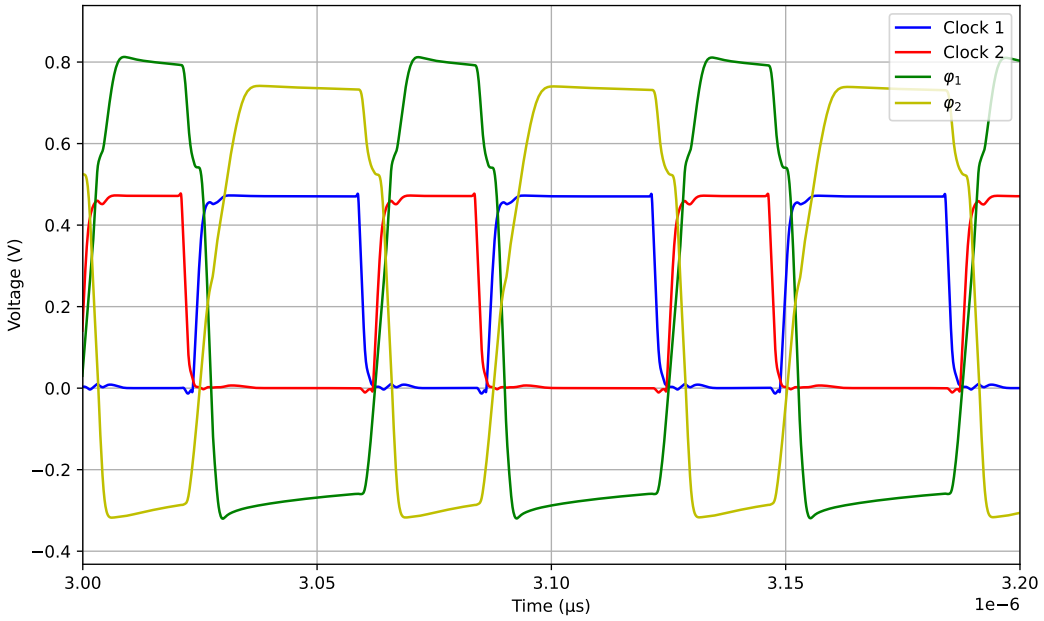


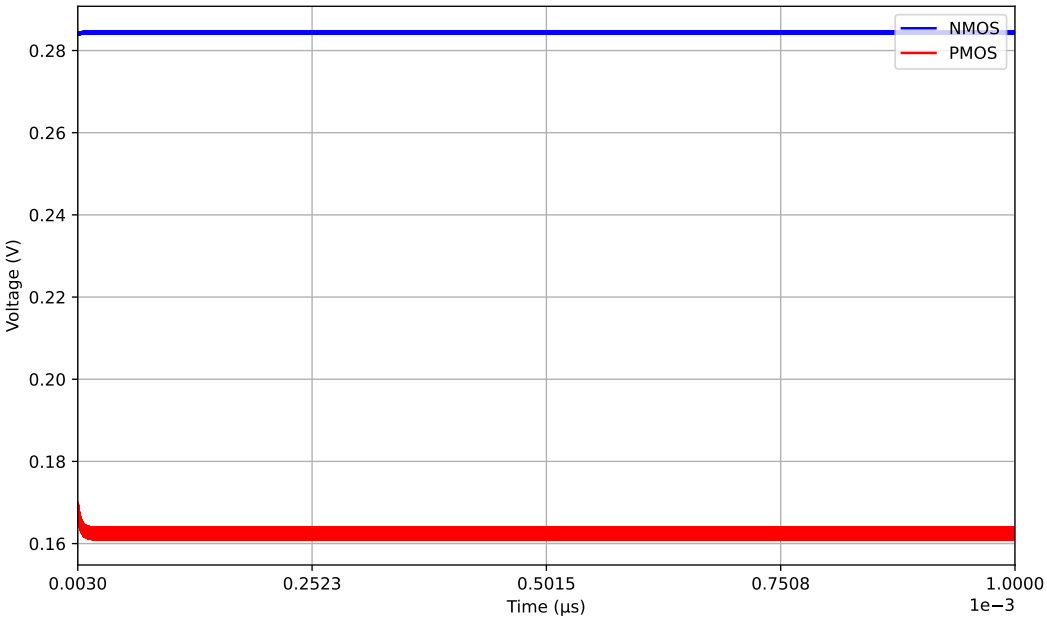
Figure 57 illustrates the transient voltage waveforms corresponding to the control currents derived from the error amplifier and current mirror within the control loop of the Current Starved Ring Oscillator (CSRO).

The signal I_{ctrl} representing the output of the error amplifier, is mirrored and fed into the NMOS transistor of the CSRO to regulate its current and thus control the oscillation frequency. Likewise, the complementary signal $\mathrm{I}_{ctrl,pmos}$ generated by the current mirror, drives the PMOS transistor of the CSRO.

The plotted waveforms demonstrate a stable and complementary behavior between I_{ctrl} and $\mathrm{I}_{ctrl,pmos}$ with voltage levels consistently ranging from approximately 0.16 V to 0.28 V. This differential control ensures balanced current starvation in both NMOS and PMOS branches of the oscillator, optimizing its frequency stability and power consumption.

The smooth transitions and minimal oscillations in both signals support the effective operation of the error amplifier and current mirror circuitry, contributing to

Figure 57 – Control Voltages of NMOS and PMOS Branches from Error Amplifier and Current Mirror in the CSRO.

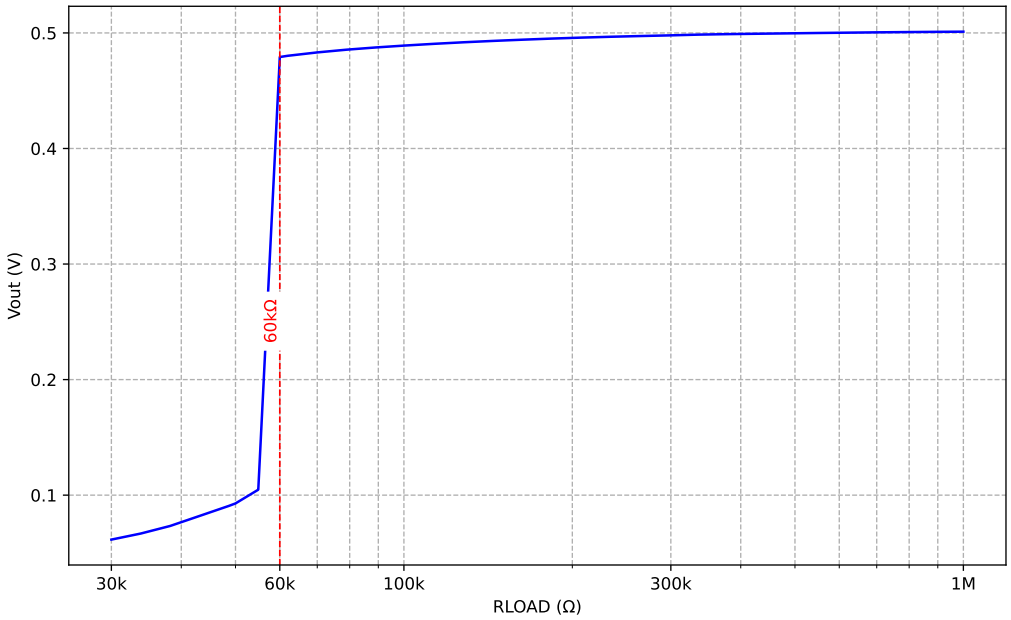


precise frequency control in the CSRO. The control currents respond dynamically to changes in operating conditions, enabling the oscillator to maintain a stable frequency over time.

The operational limits of the regulated converter, particularly concerning load requirements and available power are critical to determining its functional range. Figure 58 illustrates the regulated output voltage (V_{OUT}) as a function of the load resistance (R_{LOAD}) under a fixed illumination condition of 500 lux. The results demonstrate a clear threshold for stable operation, known as the minimum starting load. Specifically, the converter requires a minimum load resistance of 60 kΩ to successfully initiate and maintain the output voltage regulation near its target level (approximately 0.5 V). Below this threshold, the converter is unable to regulate the voltage effectively, as evidenced by the sharp drop in V_{OUT}. This phenomenon typically occurs because the circuit requires a minimum current flow of minimum input power to sustain the internal control and switching mechanisms necessary for regulation.

Figure 59 further characterize the converter's capability by showing the regulated output voltage (V_{OUT}) as a function of the incident illuminance for a specific load. This plot defines the minimum power requirement for the device's functional start-up. The data explicity reveals that the converter requires a minimum illuminance level of 390 lux to transition from the non-regulated state to a stable, regulated output state (around 0.5 V). This minimum illuminance directly correlates to the minimum input power generated

Figure 58 – Regulated converter output voltage as a function of RLOAD for afixed illuminance of 500 lux.



by the photovoltaic cell necessary to overcome the internal power consumption of the converter's control circuitry and deliver the required power to the load. These two boudary conditions - he minimum R_{LOAD} and the minimum illuminance - collectivelly define the stable operational range of the proposed converter circuit.

In Figure 60, the efficiency of the switched-capacitor circuit is shown as a function of illuminance, measured in lux. The graph indicates that the efficiency reaches its maximum value of approximately 65.8% at an illuminance level of around 420 lux. Beyond this point, the efficiency gradually decreases, showing a downward trend as illuminance increases. At the highest measured illuminance of 500 lux, the efficiency attains its minimum value of about 65.1%. This behavior suggests that the switched-capacitor circuit operates most efficiently at moderate illumination intensities, with performance diminishing slightly at higher levels of ambient light. The data underscores the sensitivity of the circuit's efficiency to changes in illuminance, which could be a critical factor in its application in energy harvesting or sensor interfacing under varying lighting conditions.

Table 8 presents the input power (PIN), output power (POUT), and the power loss (PIN - POUT) of the switched-capacitor circuit as functions of illuminance in lux. As illuminance increases from 400 lux to 500 lux, the input power rises steadily from 18.73 μW to 21.89 μW, and the output power correspondingly increases from 12.31 μW to 14.26 μW. Despite this increase in absolute power levels, the difference between input and output power, representing the power loss, also grows from 6.42 μW to 7.63 μW. This

Figure 59 – Regulated converter output voltage as a function of the illuminance.

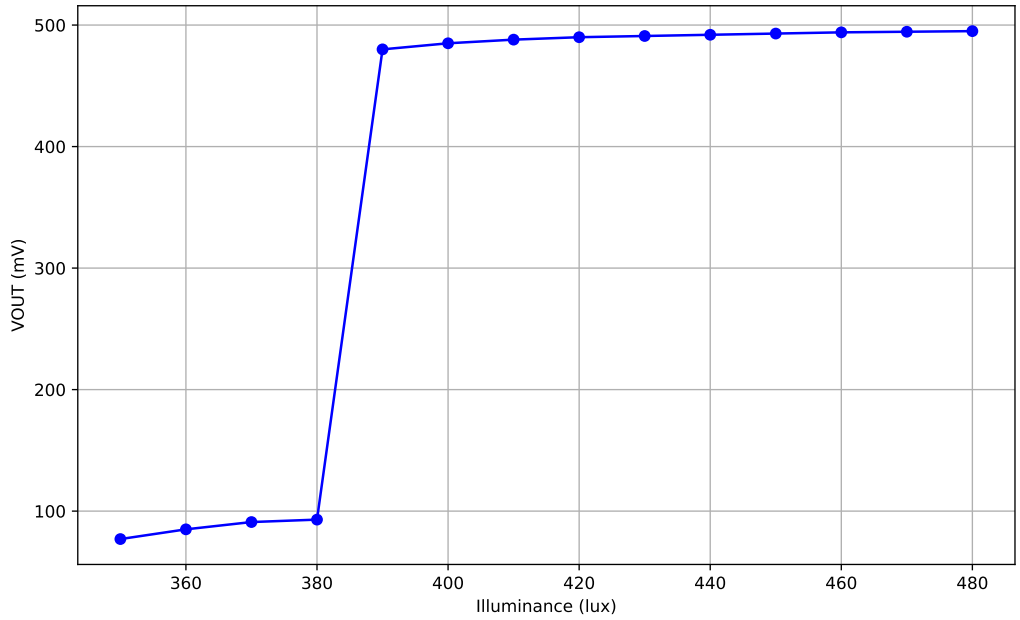
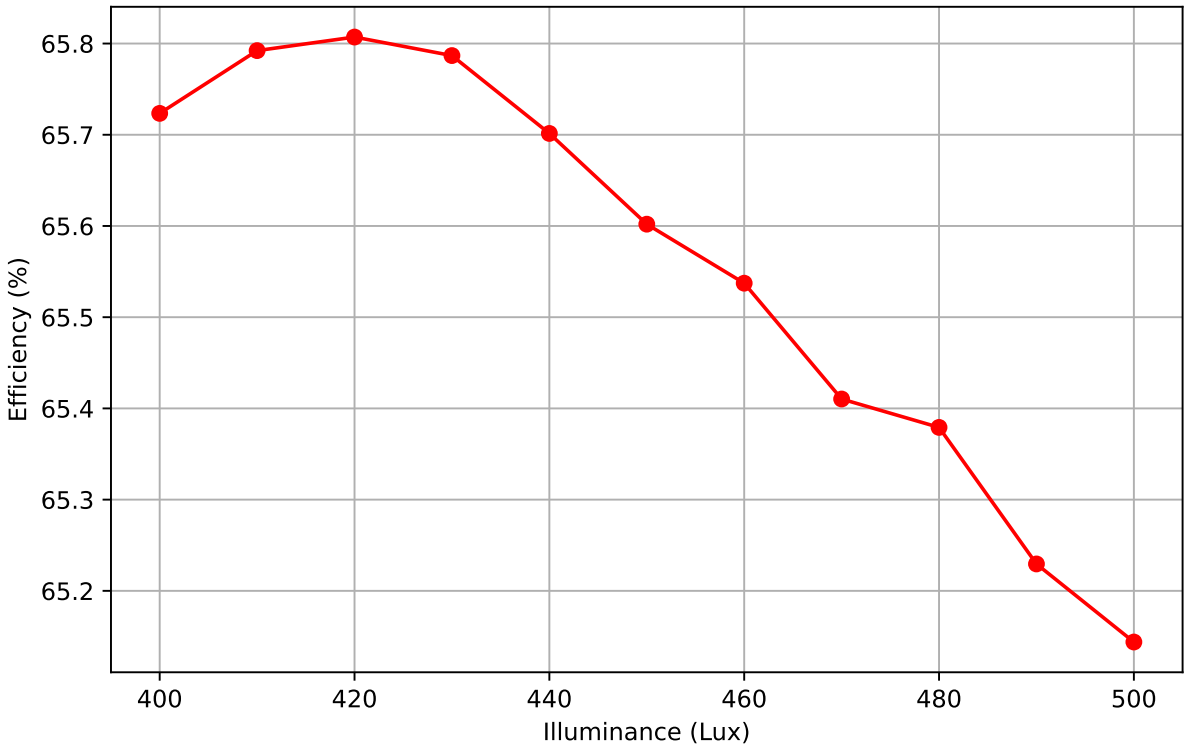


Figure 60 – Efficiency vs Illuminance.



trend is consistent with the efficiency data shown in Figure 60, where efficiency peaks at approximately 65.8% around 420 lux and then gradually declines to about 65.1% at 500

lux. The increase in power loss alongside increasing illuminance explains the reduction in efficiency at higher illumination levels, highlighting the trade-offs in power conversion performance under varying lighting conditions. These results emphasize the importance of optimizing the switched-capacitor design for specific operating environments to maximize energy harvesting efficiency. The data suggest that although the circuit harvests more power with increased light intensity, the efficiency is somewhat compromised due to higher losses, underscoring the trade-off between power availability and conversion efficiency in switched-capacitor circuits under varying lighting conditions.

Table 8 – Input and Output Power as a Function of Illuminance

Lux	PIN (μW)	POUT (μW)	PIN - POUT (μW)
400	18.73	12.31	6.42
410	19.06	12.54	6.52
420	19.39	12.76	6.63
430	19.70	12.96	6.74
440	20.03	13.16	6.87
450	20.35	13.35	7.00
460	20.66	13.54	7.12
470	20.96	13.71	7.25
480	21.23	13.88	7.35
490	21.57	14.07	7.50
500	21.89	14.26	7.63

Table 9 – Comparative performance with other energy harvesting converters.

Reference	**Converter Type**	**Technology**	**Input Voltage (V)**	**Output Voltage (V)**	**Energy Source**
(CHENG et al., 2020)	Redistributable Capacitive Power Converter	180 nm	0.45 – 0.9	1.5	Indoor light
(DUTRA et al., 2023)	Switched-capacitor converter	180 nm	0.2315 – 0.270	0.4	Indoor light
(SILVA; SEVERO; GIRARDI, 2020)	Switched-capacitor converter	180 nm	0.05 – 1.6	0.4	Indoor light
(DEVARAJ et al., 2019)	Switched-capacitor converter	65 nm	0.55	1.8 – 2.5	Piezo and solar
This work	**Switched-capacitor converter**	**65 nm**	**0.297**	**0.48 – 0.50**	**Indoor light**

Source: Author.

6 CONCLUSION

This work has delved into the realm of energy harvesting system and power management, focusing on the development of a switched capacitor converter topology. The proposed components, including the cold-start circuit and the photovoltaic cell characterization, have been meticulously designed to address key aspect of energy harvesting efficiency and performance optimization.

Detailed characterization and modeling of photovoltaic cells under varied indoor lighting conditions provided essential data informing the converter's optimum operational parameters. The 1D2R electrical model parameters were successfully extracted through DC and AC small-signal measurements, validating the PV cell's dynamic response and bandwidth limitations relevant for both energy harvesting and visible light communication (VLC). This dual-use analysis highlighted the trade-offs between maximum power point operation and communication bandwidth, suggesting an effective bias near the MPP to balance energy output and signal fidelity.

Schematic-level simulations of the cold-start system demonstrated its ability to initiate operation at low input voltages (172 mV at 50 lux), with the ring oscillator generating a high-frequency clock (18.7 MHz) and sufficient voltage boosting to power the non-overlapping and bootstrap circuits. This ensured reliable startup and stable operation of the switched-capacitor converter. Subsequent transient simulations refined these results, showing that the photovoltaic (PV) cell delivers a stable output voltage between 0.18 V and 0.28 V, corresponding to a power delivery of approximately 28.09 μW.

The series-parallel switched-capacitor converter achieved a voltage step-up, producing an output voltage ranging from 0.48 V to 0.50 V. This represents a successful multiplication from the PV cell's lower input voltage levels. The control circuit design incorporated a low-power error amplifier operating in weak inversion, a precision current mirror for frequency control of the current-starved ring oscillator (CSRO), and robust clock generation including non-overlapping and bootstrap signals. Simulation results demonstrated that the CSRO operated at a frequency of 16.02 MHz. The non-overlapping clock generation successfully produced two clean clock signals with distinct intervals, preventing simultaneous conduction and ensuring efficient switched-capacitor operation. The bootstrap circuit further boosted the generated clock signals, achieving an amplitude approximately 200 mV above the nominal supply voltage, validating its role in reliable gate driving. The CSRO control loop exhibited complementary behavior between the NMOS and PMOS branches, with control voltages ranging from 0.16 V to 0.28 V. This operation maintained frequency stability and supported efficient power regulation. The series-parallel switched-capacitor converter exhibited a voltage gain of approximately 1.68, given an input from the PV cell of 297 mV under typical indoor lighting (500 lux). Transient simulations confirmed stable output voltage regulation near 500 mV with low ripple, suitable for powering IoT circuits without the need for external inductors, thereby reducing size and

electromagnetic interference.

In Figure 60, the efficiency of the switched-capacitor circuit is shown as a function of illuminance, measured in lux. The graph indicates that the efficiency reaches its maximum value of approximately 65.8% at an illuminance level of around 420 lux. Beyond this point, the efficiency gradually decreases, showing a downward trend as illuminance increases, reaching a minimum of about 65.1% at 500 lux. Table 8 presents the input power (PIN), output power (POUT), and the power loss (PIN - POUT) of the switched-capacitor circuit across illuminance levels from 400 lux to 500 lux. As illuminance increases, both input and output power rise; however, power loss also grows, explaining the observed reduction in efficiency under higher illumination. These findings highlight the sensitivity of the circuit's efficiency to ambient lighting conditions and emphasize the trade-offs between power availability and conversion efficiency in switched-capacitor designs. Such insights are crucial for optimizing energy harvesting systems tailored for varying indoor environments.

The series-parallel switched-capacitor converter exhibited a voltage gain of approximately 1.68, given an input from the PV cell of 297 mV under typical indoor lighting (500 lux). Transient simulations confirmed stable output voltage regulation near 500 mV with low ripple, suitable for powering IoT circuits without the need for external inductors, thereby reducing size and electromagnetic interference.

Overall, the integrated system efficiently transforms ultra-low input voltages from indoor photovoltaic cells into usable supply voltages with precise control and stability, enabling batteryless operation of ultra-low power electronic devices. The design strategy effectively tackles the challenges of low voltage startup, variable illumination conditions, and the trade-offs between power extraction and communication functions in indoor environments.

Future work will focus on physical layout implementation, silicon fabrication, and experimental validation of the prototype chip to further substantiate the architecture's efficacy and robustness in practical IoT applications.

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