

FEDERAL UNIVERSITY OF PAMPA

Luís Felipe Machado Dutra

**INTEGRATED DC-DC CONVERTER FOR PHOTOVOLTAIC ENERGY
HARVESTING TARGETED TO ULTRA-LOW VOLTAGE AND LOW POWER
APPLICATIONS**

**Alegrete/RS
October 2022**

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APPLICATIONS**

Master's Thesis submitted to the Graduate
Program in Electrical Engineering of Federal
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the requirements for the degree of Master in
Electrical Engineering.

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LUÍS FELIPE MACHADO DUTRA

**INTEGRATED DC-DC CONVERTER FOR PHOTOVOLTAIC ENERGY HARVESTING TARGETED
TO
ULTRA-LOW VOLTAGE AND LOW POWER APPLICATIONS**

Dissertação apresentada ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal do Pampa, como requisito parcial para obtenção do Título de Mestre em Engenharia Elétrica.

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*This thesis is dedicated to my parents, Luis Carlos and Neusa. For their love, affection,
support and encouragement through all of my life.*

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" Whatever happens, happens. "
(Keiko Nobumoto)

ABSTRACT

Energy Harvesting is an emerging technology in this century, moreover, it has been applied in many systems, such as batteryless applications to remove the need for batteries. Most of the batteries end up in landfills, endangering the environment with toxic substances. Many types of sources of energy are available for harvesting, such as light, thermal, vibration and electromagnetic energies. Thermal and vibration are not reliable in indoor use, except for industrial applications. Indoor light energy is promising as light is not always available, especially at nighttime, whereas artificial light such as fluorescent light bulbs can be used for energy harvesting for long periods of time. DC-DC converters can be used in numerous applications in ultra-low power systems, especially for applications related to Internet of Things. For integrated-form implementation, switched-capacitor DC-DC converters are superior to its inductive counterparts due to the higher power density of capacitors and easier implementation in CMOS technologies. Transducers, such as photovoltaic cells are non-ideal devices and have finite series resistance, therefore, analytical models of the output resistance of switched-capacitor converters must include the series resistance of the transducer. A new method to model the equivalent output resistance based on the Charge Flow analysis is proposed and includes the effects of the source resistance. An Energy Harvesting system, consisting of a switched-capacitor DC-DC converter is proposed to obtain an output voltage of 400 mV using a photovoltaic cells with indoor-light levels of illuminance. The proposed system is able to provide power to an ultra-low power device between 20 μ W and 40 μ W for a minimum input voltage of 230 mV. The idea of the work is to use an hysteretic control system with comparators and a logic system to adjust the switching frequency and VCR of the converter. This converter was able to obtain a peak efficiency of 81.24% at an input voltage of 260 mV for a 20 μ W load, although it requires three external capacitors.

Keywords: Switched Capacitor. DC-DC converter. Indoor Energy Harvesting. Photovoltaic cells. Electronic Devices. Internet of Things. Ultra-Low Power Circuits.

RESUMO

A colheita de energia é uma tecnologia emergente nesse século, ela vem sendo aplicada em diversos sistemas, como aplicações sem baterias, para remover a necessidade de baterias. A maioria das baterias acaba em aterros sanitários, poluindo o ambiente com substâncias tóxicas. Diversos tipos de fontes de energia estão disponíveis para colheita de energia, como energia luminosa, térmica, vibracional e eletromagnética. A colheita de energia de luz em ambiente fechado é promissora, pois a luz externa não está disponível a todos os momentos, principalmente à noite, onde luzes artificiais, como lâmpadas fluorescentes podem prover a luz para células fotovoltaicas, que são usadas para colheita de energia por longos períodos de tempo. Conversores CC-CC são utilizados em várias aplicações em sistemas de ultra-baixa potência, especialmente em sistemas da Internet das Coisas. Para implementação em circuito integrado, os conversores à capacitor chaveado se sobressaem a sua contraparte baseada em indutores, pois a densidade de potência de capacitores é maior que indutores, além disso, capacitores são dispositivos mais simples de implementar em tecnologias CMOS. Transdutores de energia, como células solares, são dispositivos não-ideais e possuem uma resistência série finita, portanto, modelos analíticos da resistência equivalente de saída devem incluir a resistência série do transdutor. Um novo método para modelar a resistência equivalente de saída, baseada na análise de fluxo de carga é proposto e inclui os efeitos da resistência série. Um sistema de colheita de energia, que consiste de um conversor DC-DC a capacitor-chaveado, é proposto para obter uma tensão de saída de 400 mV usando uma célula fotovoltaica para iluminâncias típicas em ambientes internos. O sistema proposto pode suprir um equipamento de ultra-baixa potência entre $20\ \mu\text{W}$ e $40\ \mu\text{W}$ para uma tensão de entrada de 230 mV. A ideia do trabalho é usar um sistema de controle com histerese usando comparadores e um sistema lógico para ajustar a frequência de chaveamento e o VCR do conversor. Esse conversor consegue obter um pico de eficiência em 81.24% com uma tensão de entrada de 260 mV para uma carga de $20\ \mu\text{W}$, porém, requer três capacitores externos.

Palavras-chave: Capacitor Chaveado, Conversor CC-CC. Colheita de Energia em Ambiente Fechado. Células fotovoltaicas. Dispositivos Eletrônicos. Internet das Coisas. Circuitos de Ultra-Baixa Potência.

LIST OF FIGURES

Figure 1 – Wireless Sensor Network.	17
Figure 2 – Diagram of a typical light-powered energy harvesting system.	18
Figure 3 – Common buck-converter module.	19
Figure 4 – Active-to-sleep duty cycle ratio.	20
Figure 5 – Energy Harvesting diagram.	24
Figure 6 – Propagation of RF energy through space.	25
Figure 7 – Thermoelectric generator.	26
Figure 8 – Tension and compression effects on a piezoelectric material.	27
Figure 9 – Piezoelectric Generator PPA-1014.	28
Figure 10 – Working principle of a photovoltaic cell.	29
Figure 11 – Structure of an hydrogenated amorphous silicon (a-Si:H) PV cell.	30
Figure 12 – Structure of a cadmium-telluride (CdTe) PV cell.	30
Figure 13 – Structure of a copper-indium-gallium-diselenide (CIGS) PV cell.	31
Figure 14 – I-V characteristics of a PV cell.	32
Figure 15 – Simplified electrical model for a PV cell.	32
Figure 16 – iVCR of a DC-DC converter.	33
Figure 17 – Lumped model of the connections between a battery and a chip in a PCB.	34
Figure 18 – Simplified electrical model of a DC-DC Converter.	35
Figure 19 – Charge flow analysis in Doubler topology.	36
Figure 20 – Three-stage dickson topology.	38
Figure 21 – Voltage divider topology.	40
Figure 22 – 1/3 topology.	40
Figure 23 – Ladder topology.	41
Figure 24 – Potential efficiency by using a multi-topology converter.	42
Figure 25 – Multi-topology converter with iVCRs of 2 and 1/3.	42
Figure 26 – Multi-topology converter with iVCRs of 1, 2 and 3.	43
Figure 27 – Transformed-based model of a DC-DC voltage converter with a PV Cell connected at its input.	45
Figure 28 – Doubler with a photovoltaic cell as source.	46
Figure 29 – Symmetric topology with n converters in parallel.	47
Figure 30 – Cross-coupled Doubler.	48
Figure 31 – CMOS Switch.	49
Figure 32 – On-state resistance as function of the voltage across the switch.	49
Figure 33 – Output Equivalent Resistance as a function of the switching frequency for different values of R_s	51
Figure 34 – Output Equivalent Resistance as function of the switching frequency for different values of R_s , using CMOS switches.	52
Figure 35 – Transient voltage for $R_s = 20k\Omega$ and a switching frequency of 61.2 kHz.	52

Figure 36 – Transient voltage for $R_s = 20k\Omega$ and a switching frequency of 30 MHz.	53
Figure 37 – Simplified electrical diagram of an indoor-light energy harvesting system for ULV applications.	55
Figure 38 – Output equivalent resistance in a SC Converter with source resistances R_s of 200 Ω and 2 k Ω	56
Figure 39 – Schematic circuit of the ring-oscillator DCO, showing the CMOS inverter stages, capacitor banks, current-starving transistors and the signal decoder.	57
Figure 40 – Delay cell composed of an inverter, parasitic capacitances and capacitor bank with 9 capacitors and 9 switches, allowing the combination of 16 different load capacitances.	58
Figure 41 – Schematic diagram of the CMOS Inverter.	59
Figure 42 – Propagation delay of a single inverter in function of V_{CTRL} voltage. . .	60
Figure 43 – Schematic diagram of the CMOS Switch.	61
Figure 44 – Resistance in function of the voltage across the switch.	61
Figure 45 – Layout of the DCO.	63
Figure 46 – Comparison of frequency in function of digital code for schematic and post-layout simulations.	64
Figure 47 – Linearity error in frequency for schematic and post-layout simulations.	64
Figure 48 – Power consumption analysis of schematic and post-layout simulations. .	65
Figure 49 – Frequency variation in 0–70°C operating temperatures, and a 500-run Monte-Carlo analysis of standard deviation of the frequency in function of digital code.	65
Figure 50 – A variation of $\pm 10\%$ in supply voltage for V_{CTRL} voltages of 0 mV and 80 mV.	66
Figure 51 – Complete schematic of the proposed cold-start circuit.	68
Figure 52 – Comparison of steady-state output voltage of single, double and triple-stage Dickson converters in function of switch channel width.	70
Figure 53 – Signals $V_{\phi,1}$ and $V_{\phi,2}$ from the bootstrapped inverter with $V_{CLK,1}$ and $V_{CLK,2}$ as input from the non-overlapping clock circuit.	72
Figure 54 – Transient simulation of supply voltage for the non-overlapping circuit $V_{DD,NOV}$ and supply voltage V_{DD} in start-up phases and operation. . .	72
Figure 55 – Steady-state Output Voltage ($V_{DD,OUT}$) for temperatures of 0°C, 27°C and 70°C.	73
Figure 56 – Complete schematic diagram of the Energy Harvester.	75
Figure 57 – Schematic diagram of a doubler/tripler SC converter.	76
Figure 58 – Charge flow of topological states ϕ_1 and ϕ_2 for the SC Converter in Doubler mode.	76
Figure 59 – Charge flow of topological states ϕ_1 and ϕ_2 for the SC Converter in Tripler mode.	77

Figure 60 – On-state resistance of the CMOS switch for the SC Converter.	78
Figure 61 – 5000-run Monte-Carlo analysis of the on-state resistance of the CMOS switch considering mismatch and process effects	78
Figure 62 – Output Equivalent Resistance and optimal frequency for Doubler and Tripler modes.	79
Figure 63 – Frequency and power consumption in function of V_{CTRL}	80
Figure 64 – Doubler/Tripler mode selector with three 2-to-1 multiplexers.	81
Figure 65 – Single-ended differential amplifier.	82
Figure 66 – Steady-state Voltage Conversion Ratio (VCR) in function of a digital code for DCO frequency.	83
Figure 67 – Synchronous 5-bit up/down counter using full-adder and registers. . . .	84
Figure 68 – Logic system to enable registers, detection of stability and under- flow/overflow, and mode selection.	84
Figure 69 – Output voltage of the converter for current loads of 50 μA , 75 μA , and 100 μA with input voltages of 230 mV up to 260 mV.	85
Figure 70 – Transient of converter mode and DCO digital code of the SC Converter for a 50 μA current load.	86
Figure 71 – Transient of converter mode and DCO digital code of the SC Converter for a 75 μA current load.	87
Figure 72 – Transient of converter mode and DCO digital code of the SC Converter for a 100 μA current load.	88
Figure 73 – Efficiency of the complete energy harvesting system.	88
Figure 74 – Transient simulation of an abrupt change in current load.	89
Figure 75 – Pie-chart of power consumption considering a V_{IN} of 250 mV and a 30 μW load.	90
Figure 76 – DCO Individual Test Bench.	100
Figure 77 – DC-DC Converter Individual Test Bench.	101
Figure 78 – Complete Energy Harvesting System Test Bench.	102

LIST OF TABLES

Table 1 – Power density of alternative energy sources.	18
Table 2 – Comparison of MPPT algorithms.	21
Table 3 – Comparison of Energy Harvesters.	43
Table 4 – Comparison results of the proposed method with the transformer-based method and SPICE simulations.	50
Table 5 – Comparison results of the proposed method with the transformer-based method and Spectre simulations, considering the TSMC 180 nm technology.	53
Table 6 – Shunt-capacitor loading combinations.	59
Table 7 – Performance comparison with state-of-the-art oscillators with similar oscillation frequencies.	66
Table 8 – Performance comparison with other micro-power start-up systems for ULV applications.	73
Table 9 – Combination of topological states for the SC Converter.	80
Table 10 – Sizing of components in the multi-topology SC Converter.	81
Table 11 – Sizing of transistors for the differential amplifier.	82
Table 12 – Comparison with state-of-the-art energy harvesters.	91

CONTENTS

1	INTRODUCTION	17
1.1	OBJECTIVES	22
1.2	PUBLICATIONS	22
1.3	ORGANIZATION OF THE WORK	23
2	STATE-OF-THE-ART	24
2.1	ENERGY HARVESTING	24
2.1.1	RF ENERGY HARVESTING	25
2.1.2	THERMAL ENERGY HARVESTING	26
2.1.3	PIEZOELECTRIC ENERGY HARVESTING	27
2.1.4	LIGHT ENERGY HARVESTING	28
2.1.4.1	CHARACTERIZATION OF PV CELLS	31
2.2	SWITCHED-CAPACITOR DC-DC CONVERTERS	33
2.2.1	VOLTAGE CONVERSION RATIO (VCR)	33
2.2.2	EFFICIENCY	34
2.2.3	NOISE	34
2.2.4	ELECTRICAL MODEL OF SC DC-DC CONVERTERS	35
2.3	TOPOLOGIES OF SC DC-DC CONVERTERS	37
2.3.1	STEP-UP SC CONVERTERS	38
2.3.1.1	DICKSON CONVERTER	38
2.3.1.2	PARALLEL-SERIES CONVERTER	39
2.3.2	STEP-DOWN SC CONVERTERS	39
2.3.2.1	SERIES-PARALLEL CONVERTER	39
2.3.2.2	LADDER CONVERTER	41
2.3.3	MULTI-TOPOLOGY CONVERTERS	41
2.4	SC CONVERTERS FOR ENERGY HARVESTERS	43
2.5	CONCLUSION	44
3	MODELING THE EQUIVALENT OUTPUT RESISTANCE $R_{OUT,EQ}$	45
3.1	OUTPUT RESISTANCE CONSIDERING SOURCE RESISTANCE	46
3.1.1	GENERIC METHOD	46
3.1.2	COMPLEMENTARY METHOD FOR SYMMETRIC CONVERTERS	47
3.2	NON-LINEAR SWITCHES	48
3.3	RESULTS	50
3.4	CONCLUSION	54
4	PROPOSED ENERGY HARVESTING SYSTEM	55
4.1	DIGITALLY CONTROLLED OSCILLATOR	55
4.1.1	DESIGN AND SIZING OF COMPONENTS	56

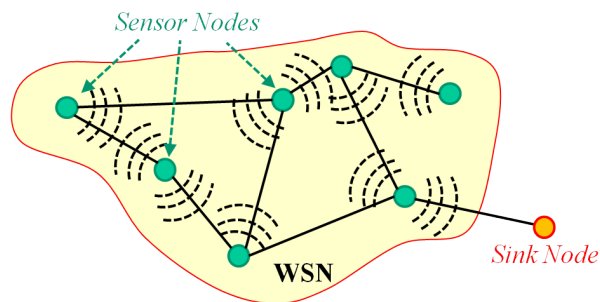
4.1.1.1	CAPACITOR BANK	58
4.1.1.2	CMOS INVERTER AND CURRENT-STARVING TRANSISTOR	59
4.1.1.3	CMOS SWITCH	60
4.1.1.4	DECODER	61
4.1.1.5	CMOS BUFFER	62
4.1.2	RESULTS	62
4.1.3	CONCLUSION	66
4.2	COLD-START SYSTEM	67
4.2.1	PROPOSED COLD-START SYSTEM	68
4.2.2	SIMULATION RESULTS	71
4.2.3	CONCLUSION	73
4.3	A DUAL-MODE SC DC-DC CONVERTER WITH FEEDBACK CONTROL	74
4.3.1	SPECIFICATION AND DESIGN STRATEGIES	74
4.3.2	DESIGN OF A SWITCHED-CAPACITOR DC-DC CONVERTER .	75
4.3.2.1	CALIBRATION OF SWITCHING FREQUENCY	77
4.3.2.2	MULTIPLEXERS	79
4.3.3	CONTROL	80
4.3.3.1	COMPARATORS	80
4.3.3.2	HYSTERETIC LOGIC SYSTEM AND BIDIRECTIONAL COUNTER . .	82
4.4	RESULTS	85
4.5	CONCLUSION	90
5	CONCLUSION	92
5.1	FUTURE WORKS	92
	BIBLIOGRAPHY	93
	APPENDIX A – CHIP TEST BENCH	100
A.1	DCO INDIVIDUAL TEST BENCH	100
A.2	DC-DC CONVERTER INDIVIDUAL TEST BENCH	101
A.3	COMPLETE ENERGY HARVESTING SYSTEM TEST BENCH .	102

1 INTRODUCTION

Internet of Things (IoT) is a term that was first coined in 1999 to refer to the concept of connecting devices to the internet (KRAMP; KRANENBURG; LANGE, 2013). Many gadgets are already part of the world of Internet of Things, such as wearables, sensors, and even medical monitoring devices (CHURCHILL et al., 2020).

Wireless Sensor Network (WSN) is a network with a large number of sensor nodes dispersed in a specific area, responsible for monitoring and storing the physical conditions of the environment, such as temperature and humidity. WSNs can be used in areas of difficult access or hostile areas, where those sensors must sustain themselves for months, or even years, since maintenance can be difficult, or nearly impossible due to the large number of sensor nodes (SHAIKH; ZEADALLY, 2016). The diagram of a Wireless Sensor Network is illustrated in Figure 1.

Figure 1 – Wireless Sensor Network.



Source: From (CORRADINI et al., 2014).

Commonly, batteries are used to attain a larger autonomy for those devices, but batteries have a limited lifespan. The capacity of holding charge and lifespan of the lithium-ion battery gradually deteriorates as the number of charge and discharge cycles increases (HU et al., 2020). The constant need for replacement can pose serious environmental pollution if batteries are improperly disposed of, mainly due to flammable and toxic heavy metals present in batteries, such as cadmium, mercury, lead and lithium (KANG; CHEN; OGUNSEITAN, 2013). According to Chen (2018), less than 5% of the total of discarded lithium-ion batteries are recycled, whereas most of those batteries end up in landfills.

Energy Harvesting is an alternative available to obtain a large autonomy while maintenance-free. Energy can be defined as a "force" carried in the form of matter or waves through a medium, such as water, air, or metals (SOYATA; COPELAND; HEINZELMAN, 2016). In energy harvesting, the goal is to gather the ambient energy, which would otherwise be lost to heat, and transform it into electrical energy through the use of a transducer, for example, a photovoltaic cell. It is easily distinguishable from renewable energies as Energy Harvesting can be defined as the collection of local naturally available energy for local use. Also, it has a characteristic of low power that typically ranges from nanowatts to milliwatts of power (KIZIROGLOU; YEATMAN, 2012).

Table 1 compares the power density in the most common energy sources for Energy Harvesting.

Table 1 – Power density of alternative energy sources.

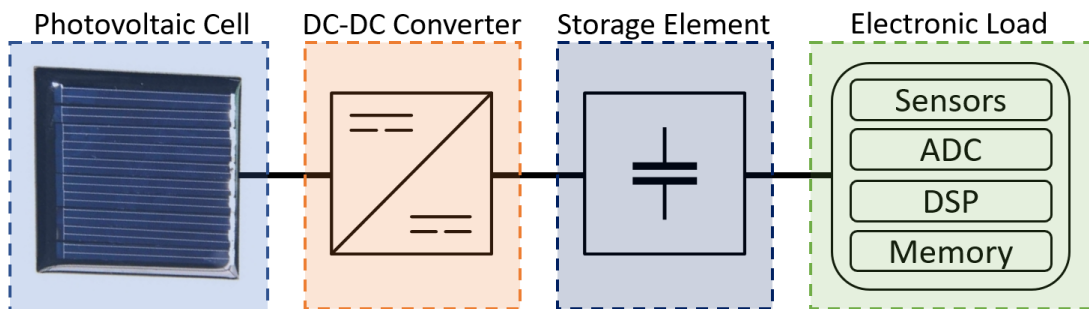
Source	Power Density	Harvesting technology
Light	Indoor: $10 \mu W/cm^2$ Outdoor: $10 mW/cm^2$	Photovoltaic
Vibration	Human: $4 \mu W/cm^2$ Industrial: $100 \mu W/cm^2$	Piezoelectric Electrostatic Electromagnetic
Thermal	Human: $30 \mu W/cm^2$ Industrial: $1-10 mW/cm^2$	Thermoelectric Pyroelectric
RF	GSM: $0.1 \mu W/cm^2$ Wi-Fi: $1 mW/cm^2$	Patch antenna

Source: From (TRAN; CHA; PARK, 2017).

In Table 1, the RF Energy Harvesting is shown to be an option with a high power density and high reliability, but the power output is heavily dependant on the distance from a transmitting device (CHURCHILL et al., 2020). Even though Thermal and Vibration Energy Harvesting are options with high power density, they are not always available, especially in indoor environments (TRAN; CHA; PARK, 2017).

Light is a commonly used ambient energy source in Energy Harvesting. Apart from being renewable energy, light is abundant in nature, and has a very high power density, as evidenced in Table 1. Photovoltaic cells are common transducers for indoor-light and outdoor-light energy harvesters. In Silva, Compassi-Severo and Girardi (2019), a 42x42 mm photovoltaic cell is characterized at an indoor lighting environment with average office illuminance levels. At 470 lux and 700 lux, the power output is measured as $23 \mu W$ and $42 \mu W$, respectively. For those reasons, this work proposes the use of photovoltaic cells to harvest energy from indoor lighting. A typical light-based energy harvesting system using a photovoltaic cell is illustrated in Figure 2.

Figure 2 – Diagram of a typical light-powered energy harvesting system.



Source: Author.

The typical Energy Harvester consists of three key components: a transducer, a voltage converter, and an energy-storing element. Many types of transducers can be used for energy harvesting, for example, photovoltaic (PV) cells, thermoelectric generators (TEGs), and piezoelectric generators (SILVA; SEVERO; GIRARDI, 2020; DEVARAJ et al., 2019; YOON; PARK; YU, 2018). The energy-storing element can be a battery, a capacitor, or a super-capacitor.

DC-DC voltage converters are widely used to produce a regulated voltage from unregulated or non-constant voltage sources, such as the voltage produced by photovoltaic cells. A voltage converter interfaces an unregulated or loosely regulated source to specific voltage rails in an electronic system. Linear converters are very inefficient due to excessive power-loss in heat, also, it only works as a step-down converter. In contrast, the switched-mode DC-DC converters are very versatile and efficient. Switched-mode converters are either inductor-based or capacitor-based. The inductor-based converter is composed of an inductor, a capacitor, and switches, while the capacitor-based converter does not contain any magnetic component, and is only composed of capacitors and switches (Van Breussegeem; STEYAERT, 2013). A common inductor-based buck-converter DC-DC voltage converter module is shown in Figure 3.

Figure 3 – Common buck-converter module.

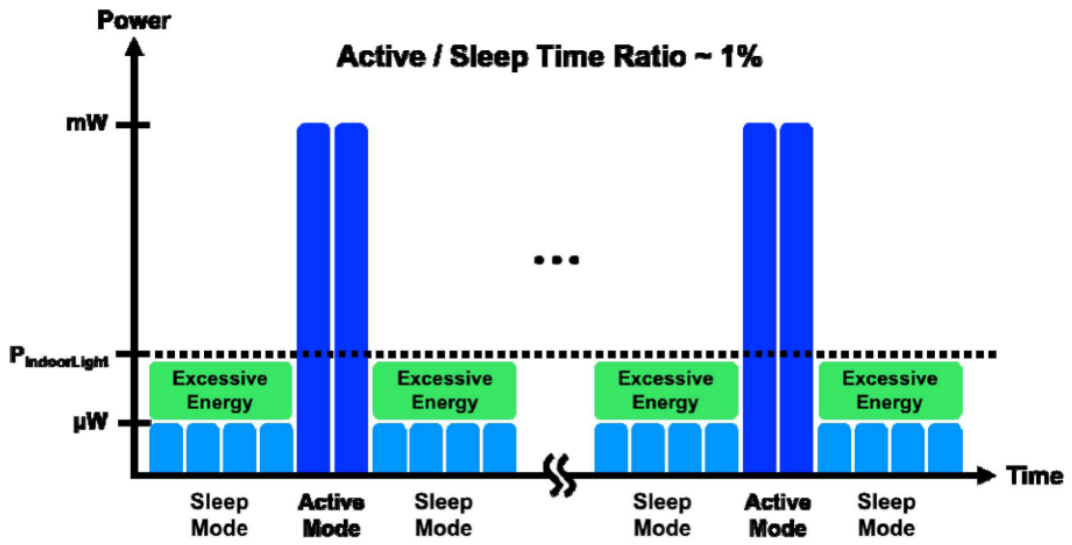


Source: From (DIGIKEY.COM, 2021).

Theoretically, an inductor-based converter provides a near lossless conversion under continuous input-output voltages, while the capacitor-based cannot replicate that accomplishment. The inductor-based converter loses its superiority over capacitor-based converters in integrated form due to the poor quality of integrated inductors. While capacitors are simple and native devices in CMOS technologies, the inductor is a more complex device (Van Breussegeem; STEYAERT, 2013). Small areas are often desired on integrated circuits due to costs, and capacitor-based converters have a greater power density than inductor-based converters (SEEMAN et al., 2010). For those reasons, this work proposes the use of switched-capacitor DC-DC converters.

For certain ultra-low power (ULP) applications (COMPASSI-SEVERO; Van Noije, 2019), the need for batteries can be partially, and even completely removed through the use of a batteryless system. In those systems, capacitors or supercapacitors can be used to replace batteries as the energy storing component. In some applications, such as RF transceivers, a very low active-to-sleep duty cycle ratio is expected. In other words, a power-hungry active mode is operating only for a small fraction of a complete cycle, while the rest of the cycle is spent in a sleep mode to recover the consumed energy (CHENG et al., 2020). This characteristic is illustrated in Figure 4.

Figure 4 – Active-to-sleep duty cycle ratio.



Source: From (CHENG et al., 2020).

The photovoltaic cell is a non-ideal source of energy, and thus, it has a finite internal resistance, therefore, the maximum power transfer theorem must be applied in order to maximize the power transfer. The maximum power transfer theorem, also known as Jacobi's law, states that the maximum power transfer occurs when the resistance of the load is equal the source resistance as viewed from the output terminals (GAIKWAD; LOKHANDE, 2015). A Maximum Power Point Tracking (MPPT) system can be implemented for this. MPPT is a technique that continuously tracks the P-V and I-V characteristics from the non-linear source of energy in order to extract as much power as possible from it. An energy harvester does not require MPPT in order to work, but the technique contributes to a significant increase of 65% to 90% in power transfer (RAGHUNATHAN; CHOU, 2006). Moreover, those techniques contribute to the overall performance of the circuit, since the storage element is always charged at the maximum rate of the energy harvesting system (CARVALHO; PAULINO, 2016). In switched-capacitor DC-DC converters, the switching frequency must be in a range that allows the PV cells to reach the maximum power point (SOUSA, 2017).

MPPT techniques are divided into two distinct categories: true-MPPT and quasi-MPPT. True-MPPT techniques track the actual MPP of a PV cell, independent of external conditions such as light and temperature, and produce very accurate approximations of the MPP. Those techniques rely upon microcontroller computation and may require more sensors and power-hungry circuitry for precise measurements, which is not an ideal solution for ultra-low power applications. Quasi-MPPT techniques obtain an approximation of the MPP of a PV cell. The MPP is not significantly affected by external conditions (light, temperature, and others), therefore, the PV cell can be characterized and the voltage or current of the MPP can be obtained.

Some of the most common MPPT algorithms are compared in Table 2, considering the categories, speed of convergence, implementation complexity and sensed parameters.

Table 2 – Comparison of MPPT algorithms.

MPPT Technique	True MPPT?	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill climbing	Yes	Varies	Low	Voltage and current
Fuzzy logic control	Yes	Fast	High	Varies
Neural network	Yes	Fast	High	Varies
RCC	Yes	Fast	Low	Voltage and current
I_{MPP} and V_{MPP} computation	Yes	N/A	Medium	Irradiance and temperature
Current sweep	Yes	Slow	High	Voltage and current
Fractional V_{OC}	No	Medium	Low	Voltage
Fractional I_{SC}	No	Medium	Medium	Current
DC link capacitor droop control	No	Medium	Low	Voltage
Load I or V maximization	No	Fast	Low	Voltage and current
OCC MPPT	No	Fast	Medium	Current
LRCM	No	N/A	High	Voltage and current

Source: Adapted from (CARVALHO; PAULINO, 2016).

From the true-MPPT techniques presented in Table 2, the Hill Climbing technique has a low implementation complexity, however, it requires a voltage and a current sensor, also a signal processing circuitry. Another option that presents a low implementation complexity is the RCC (ripple correlation control) technique, however, this circuit requires an analog multiplier to obtain the instantaneous power. An analog multiplier has a very high power consumption. The complex and power-hungry circuitry present in true-MPPT techniques is not ideal for implementation in ultra-low power applications.

From the quasi-MPPT techniques presented in Table 2, the DC Link Capacitor Droop technique presents the lowest implementation complexity and only requires a current sensor, however, this method only works when connected to an AC line, and is generally used in DC-AC inverters. Another low complexity option is the FOCV (fractional open-circuit voltage) technique. This technique defines a coefficient k for the MPP, and

this parameter is estimated to be within a range of 0.71-0.78 of the open-circuit voltage. In order to determine the value of k , a prior characterization of the PV cell is required (CARVALHO; PAULINO, 2016). The MPP voltage is defined in Eq. 1.1, where k is the MPP coefficient and V_{OC} is the open-circuit voltage.

$$V_{MPP} = k \cdot V_{OC} \quad (1.1)$$

Moreover, the FOCV technique consumes very little power because the circuitry consists of only a voltage sensor, a comparator, and a reference voltage. Such a low-power implementation is ideal for ULP applications. For those reasons, this work proposes the use of an MPPT system with the FOCV algorithm.

1.1 OBJECTIVES

The main goal of this work is to propose and validate an integrated switched-capacitor DC-DC converter for a batteryless energy harvesting system supplied by a photovoltaic cell with an energy-storing capacitor to remove the need for battery usage in an ultra-low power device. The energy harvesting system will be suitable for ultra-low power applications at indoor and outdoor ambient lighting levels.

The specific goals of this work are: to propose and validate a method to model the equivalent output resistance of switched-capacitor DC-DC converters considering source resistance effects; to characterize photovoltaic cells at a range of lighting at indoor and outdoor ambient lighting for insight about the limitations and electrical characteristics; to propose a switched-capacitor DC-DC converter topology with multiple voltage conversion ratios; to simulate the electrical behavior to validate the proposed topology;

1.2 PUBLICATIONS

Several parts of this Master's dissertation were published in proceedings of events. Chapter 3 was used in two papers for the 2021 and 2022 South Symposium on Microelectronics (SIM) (DUTRA; GIRARDI; COMPASSI-SEVERO, 2021; DUTRA; GIRARDI; COMPASSI-SEVERO, 2022a). The Digitally-Controllable Oscillator was presented in the 2022 Symposium on Integrated Circuits and Systems Design (SBCCI) (DUTRA; GIRARDI; COMPASSI-SEVERO, 2022b), and the proceedings are available on IEEE Xplore. Two papers about PV cell modeling were published in the proceedings of SIM 2022 and in the 2022 36th Symposium on Microelectronics Technology (SBMICRO) (MONTEIRO et al., 2022b; MONTEIRO et al., 2022a). A paper about the cold-start system was submitted to 2023 IEEE Latin American Symposium on Circuits and Systems (LASCAS) and is currently waiting for acceptance. Moreover, an article about the complete energy harvesting system for publication in an international periodic is in its finishing stages.

1.3 ORGANIZATION OF THE WORK

This work is organized as follows: Chapter 2 presents an overview on the different types of sources for energy harvesting, and topologies of DC-DC converters. Chapter 3 proposes an analytical modelling method considering source resistance effects. Chapter 4 proposes an Energy Harvesting system, consisting of a DCO, cold-start system, logic control, and a switched-capacitor DC-DC converter. Chapter 5 draws the conclusion of this dissertation.

2 STATE-OF-THE-ART

This chapter reviews the state-of-the-art works from the literature related to the applications of Energy Harvesting, DC-DC Converters, and MPPT.

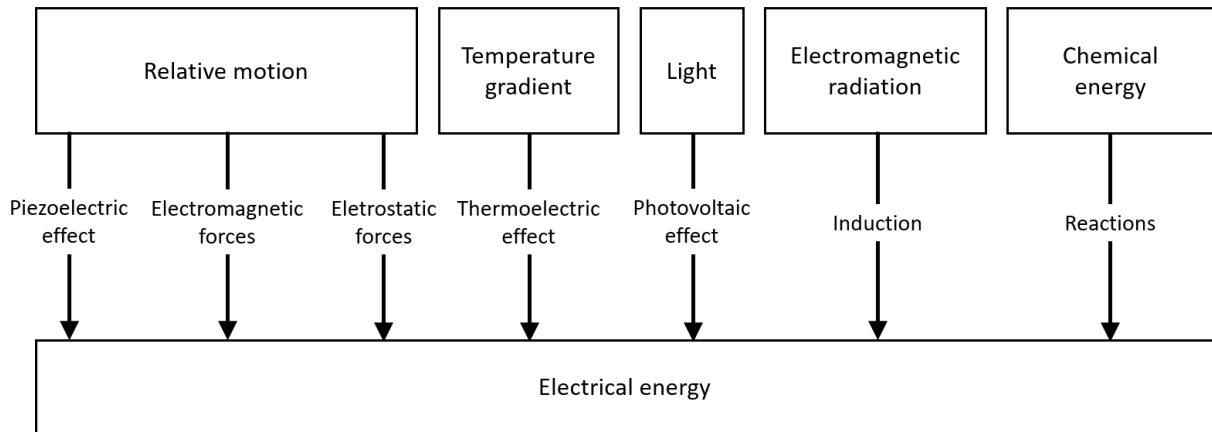
2.1 ENERGY HARVESTING

Energy Harvesting is an important emerging technology in the 21st century. As the name suggests, Energy Harvesting refers to the collection of energy from the environment (KIZIROGLOU; YEATMAN, 2012). Energy can be defined as a force carried in form of matter or waves through a medium, such as water, air, or metals. The goal in Energy Harvesting is to intercept and convert this "force" into electrical energy through a transducer (SOYATA; COPELAND; HEINZELMAN, 2016).

Wireless devices are the main application of Energy Harvesting for low power, although, the application is mainly limited by the availability of ambient energy (KIZIROGLOU; YEATMAN, 2012). Although, there are many low-power applications for energy harvesting, most notably for Internet of Things, such as wearable devices, embedded systems, and remote sensors (CHURCHILL et al., 2020). Energy Harvesting can be used for charging batteries or to store energy into other types of storage, such as capacitors and supercapacitors.

Nowadays, many sources of energy are available for Energy Harvesting, most notably, light, thermal, electromagnetic, and motion-based energy sources. The diagram in Figure 5 depicts some commonly found sources for energy harvesting.

Figure 5 – Energy Harvesting diagram.



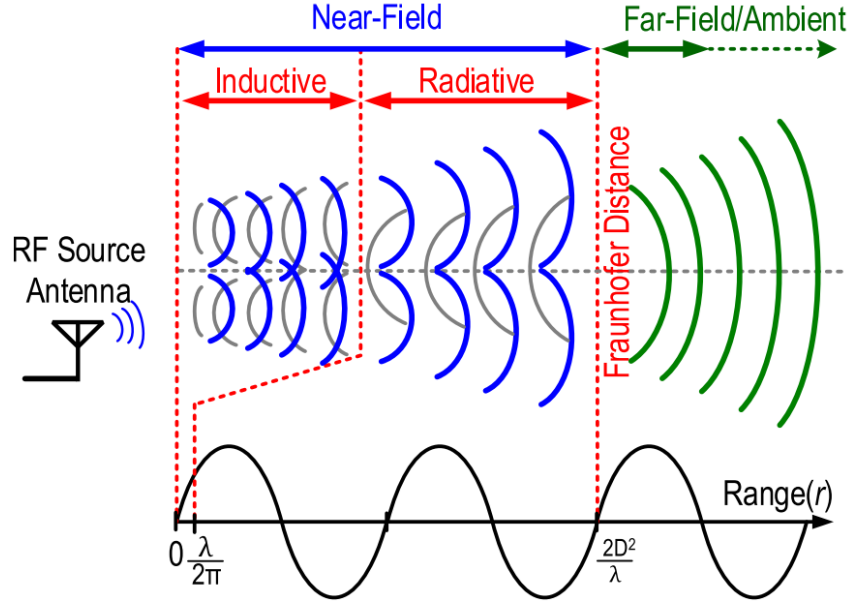
Source: Adapted from (KIZIROGLOU; YEATMAN, 2012).

The following sections explain the most common energy sources found in Energy Harvesters, namely: Light, RF, Thermal and Piezoelectric.

2.1.1 RF ENERGY HARVESTING

Radio Frequency (RF) Energy Harvesting systems are categorized into two types: Near-field and Far-field. The propagation of RF energy through space is illustrated in Figure 6 and shows the operation of each type (CHURCHILL et al., 2020).

Figure 6 – Propagation of RF energy through space.



Source: From (CHURCHILL et al., 2020).

The power density of the Near-Field type is significantly larger when compared to the Far-Field type. The Near-Field type operates through magnetic coupling where the transmitter and receiver are placed in proximity within the Fraunhofer distance. The distance is calculated through Eq. 2.1, where D is the diameter of the antenna and λ is the wavelength of the signal (CHURCHILL et al., 2020).

$$d = \frac{2D^2}{\lambda} \quad (2.1)$$

The propagated wave of electromagnetic radiation consists of an electrical and magnetic components. The system is classified as a far-field when the transmission range of the propagated wave is beyond the Fraunhofer's distance. In the far-field, the electrical and magnetic components have equal magnitude and the power can be predicted through Friss' equation, expressed in Eq. 2.2.

$$P_{RX} = \frac{P_{TX} \cdot G_{TX} \cdot G_{RX} \cdot \lambda^2}{(4\pi \cdot R)^2} \quad (2.2)$$

Where P_{TX} is the transmitted power, G_{TX} is the gain of the transmitter, G_{RX} is the gain of the receiver, and R is the distance between the transmitter and receiver antennas.

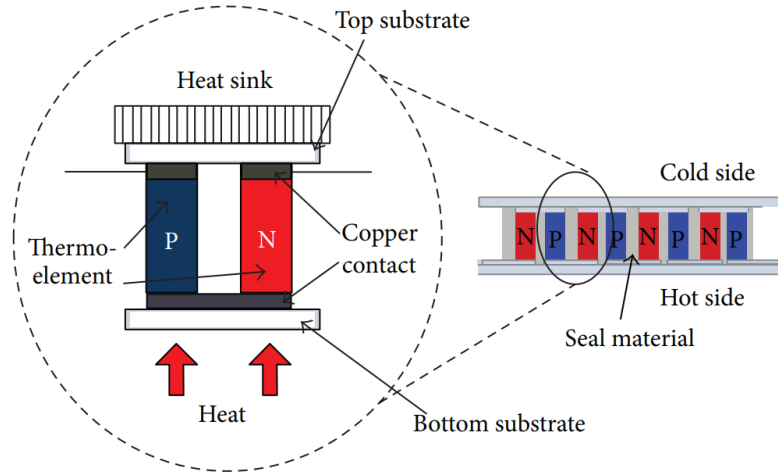
The difference between RF Energy Harvesting and Light Energy Harvesting is that in RF, the source is an intentional electromagnetic radiation from a transmitter, instead of a naturally occurring radiation from the sun. Therefore, the RF radiation can be determined by the transmitter (SOYATA; COPELAND; HEINZELMAN, 2016).

The main advantages of an RF energy harvesting source is the high reliability of far-field RF Energy Harvesting and the need for just a very small transducer, generally just a small antenna (CHURCHILL et al., 2020).

2.1.2 THERMAL ENERGY HARVESTING

In Thermoelectric Energy Harvesting, the Seebeck effect is taken into consideration for the heat conversion to electricity. This effect is illustrated in Figure 7.

Figure 7 – Thermoelectric generator.



Source: From (WANG et al., 2013).

Two different materials, namely P and N, and one of their sides should be at a low temperature (T_1), and the other one at a higher temperature (T_2). An electrical connection between P and N is made at the hot side, and the voltage across those materials is monitored at the cold side. Free moving particles such as electrons, holes and phonons carry a heat flow in the materials due to the difference in temperature between the hot and cold sides ($\Delta T = T_2 - T_1$). Until equilibrium is reached, an electrical field is created to oppose the space charges at the contact of the materials caused by the motion of the charged particles. The voltage across a material is defined by Eq. 2.3, where α is the Seebeck's coefficient, a temperature-dependent parameter for the material (KIZIROGLOU; YEATMAN, 2012).

$$V = \alpha \cdot \Delta T \quad (2.3)$$

The voltage across both materials (thermocouple) is defined by Eq. 2.4

$$V_{thermocouple} = V_P - V_N = (\alpha_P - \alpha_N) \cdot \Delta T \quad (2.4)$$

The series resistance of the thermocouple is the main factor limiting the power output. Also, Seebeck's coefficient typically ranges in hundreds of $\mu V/K$, therefore, in a thermoelectric generator (TEG), either many thermocouples connected in series or structurally-long thermocouples are used in order to increase the output voltage (KIZIROGLOU; YEATMAN, 2012).

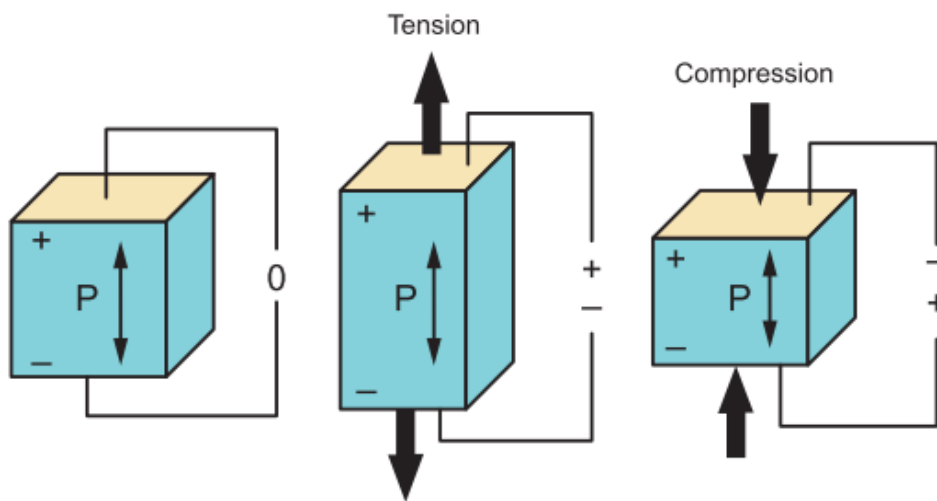
An example of Energy Harvesting through the use of a TEG is seen in Dezyani et al. (2018). In that work, the minimum required input voltage is 60 mV, which is feasible for the majority of the commercially available TEGs. At the minimum input voltage, the power output was measured as $4.5 \mu W$, enough to power a few ultra-low power systems. In Wang et al. (2013), the source of energy is a 50x60 mm TEG that generates a power of 0.2 mW with a $3.5^\circ C$ temperature difference, and a power of 0.95 mW with a $4^\circ C$ temperature difference.

2.1.3 PIEZOELECTRIC ENERGY HARVESTING

Certain materials have an ability to generate electrical charge in response to a mechanical force, this is called the piezoelectric effect. In Energy Harvesting, the piezoelectric effect is used to transform the kinetic energy from vibrations into electrical energy (KIZIROGLOU; YEATMAN, 2012).

Vibration is an inertial motion that causes mechanical stress in a piezoelectric material. When pressure is applied in a piezoelectric material, a change in the polarity of the dipoles is made, thus, an imbalance between two surfaces results in charge separation, which, in turn, generates a voltage on the output (KIZIROGLOU; YEATMAN, 2012; DIAS, 2015). The effects of compression and tension on piezoelectric materials are illustrated in Figure 8.

Figure 8 – Tension and compression effects on a piezoelectric material.



Source: From (DIAS, 2015).

The majority of piezoelectric materials are made of lead zirconate titanate (PZT). Higher sensitivity and operating temperature are characteristic traits of PTZ ceramics. Also, in that ceramic, there is a morphotropic phase boundary at 52% of lead zirconate, therefore, a large number of domain states are available for a vast temperature range (KIZIROGLOU; YEATMAN, 2012). Piezoelectric generators are very attractive as energy sources for Energy Harvesters due to attributes such as the high availability for a large range of temperatures.

Output impedance tends to be high in piezoelectric materials, often exceeding 100 k Ω , therefore, electrical current is limited. Although, those materials are able to generate high voltages (DIAS, 2015). The output voltage is an oscillating signal that must be rectified for use in charge pumps (DEVARAJ et al., 2019).

In Devaraj et al. (2019), a piezoelectric generator PPA-1014 from MIDE Engineering Solutions (2021) is used as an energy source for an Energy Harvester. This transducer is shown in Figure 9.

Figure 9 – Piezoelectric Generator PPA-1014.



Source: From (DIGIKEY.COM, 2021).

It generates a voltage of 1.6 V at vibrations with a frequency of 66 Hz, relatively close to its resonant frequency. At the maximum power point, the series resistance of the piezoelectric generator is 125 k Ω . And according to (MIDE Engineering Solutions, 2021), the transducer is capable of generating up to 400 μ W of power.

2.1.4 LIGHT ENERGY HARVESTING

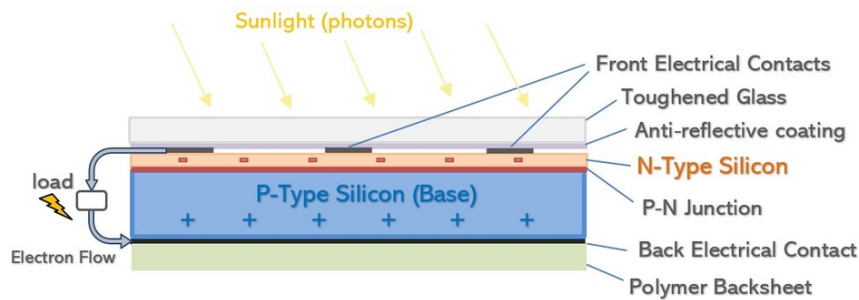
The photovoltaic effect was first observed in 1839 by french scientist Edmond Becquerel. The first solar cell was created in 1883 by Charles Fritts. It was made of selenium and a layer of transparent gold coating, but had a very poor power conversion efficiency (PCE) of 0.05%. The era of photovoltaics finally began in 1954, when D. Chapin, G. Pearson, and C. Fuller successfully fabricated a solar cell made of silicon, with a PCE

of 5.7% (CARVALHO; PAULINO, 2016). For comparison, by 2020, solar cells can reach up to 47.1% of PCE under certain conditions (GEISZ et al., 2020).

Silicon-based photovoltaic cells have remained almost unchanged since 1954 (CARVALHO; PAULINO, 2016). In 2020, crystalline silicon dominates the market of photovoltaics with approximately 90% of usage (ZENDEHDEL; Yaghoobi Nia; YAGHOUBINIA, 2020). This type of cell is constituted of a P-N junction, where the n-type silicon is a thin layer, highly doped with phosphorus. The n-type silicon sits upon a p-type substrate lightly doped with boron (SOUSA, 2017; CARVALHO; PAULINO, 2016).

As photons from a light source are absorbed by free-electrons of the n-junction of the PV cell, an electron-hole pair is created. Electrons make a current flow between the positive and negative layers of the photovoltaic cell, thus, generating a voltage. The incident irradiance has photons with a great variety of energy levels, however, only photons with an energy level above the band gap energy can mobilize free electrons (ABDELHADY; ABD-ELHADY; FOUAD, 2017; SOUSA, 2017). The working principle is illustrated in Figure 10.

Figure 10 – Working principle of a photovoltaic cell.



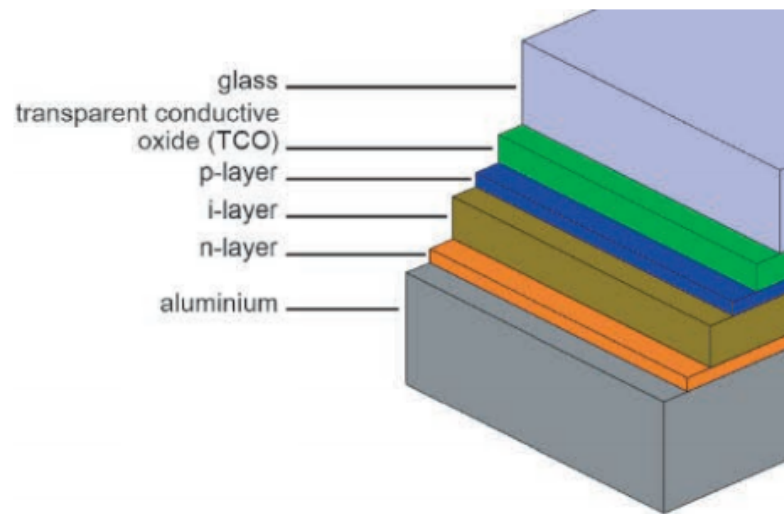
Source: From (SVARC, 2021).

Apart from the wafer-based PV cells explained above, there are also thin-film PV cells. These cells consist of layers of semiconductors deposited into plastic, glass, or metal substrates. Generally, the fabrication of thin-film PV cells is through additive processes, which contributes to a reduction in material usage and fabrication costs. Some commercially available technologies of thin-film cells are: hydrogenated-amorphous-silicon (a-Si:H), cadmium-telluride (CdTe), and copper-iridium-gallium-diselenide (CIGS) (ZENDEHDEL; Yaghoobi Nia; YAGHOUBINIA, 2020).

Hydrogenated amorphous silicon (a-Si:H) technology offers higher absorption than crystalline-silicon, but according to Shah et al. (2004), the band gap voltage of 1.7–1.8 eV is not well-matched in the solar spectrum. Those cells can be flexible, weigh very little, and are suited for low-power applications. However, their share on the market has been diminishing due to the light-induced degradation of the Staebler-Wronski effect, and lower efficiency in comparison to other thin-film technologies (ZENDEHDEL; Yaghoobi Nia;

YAGHOUBINIA, 2020). The structure of the a-Si:H cell is illustrated in Figure 11.

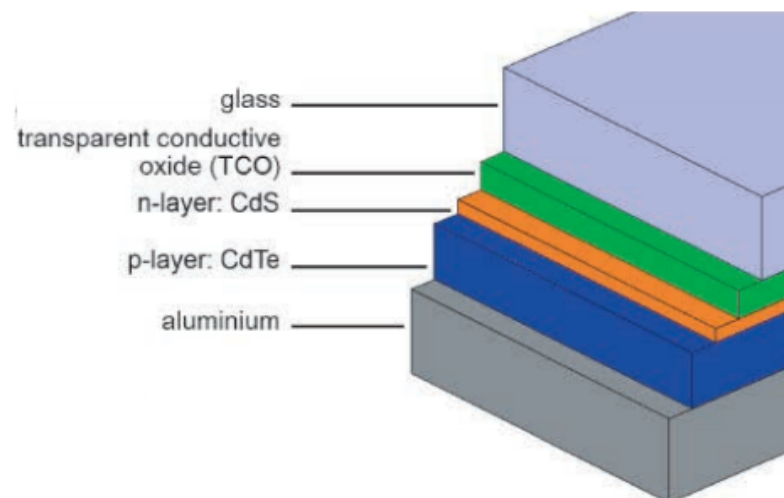
Figure 11 – Structure of an hydrogenated amorphous silicon (a-Si:H) PV cell.



Source: From (BRADSHAW; REUTER; HAMACHER, 2013)

Cadmium-telluride (CdTe) is the most suited composite for Solar Energy Harvesting purposes due to the strong absorption in the solar spectrum and low band gap voltage of 1.45 eV. In 2016, Solar First Inc. was able to reach a PCE of 22.1% in a small lab-scale PV cell (MILLER; PETERS; SHIVAM, 2020). The main concerns about this technology are the toxicity of the cadmium, and the geological scarceness of tellurium on Earth's crust (ZENDEHDEL; Yaghoobi Nia; YAGHOUBINIA, 2020). The structure of the CdTe cell is illustrated in Figure 12.

Figure 12 – Structure of a cadmium-telluride (CdTe) PV cell.

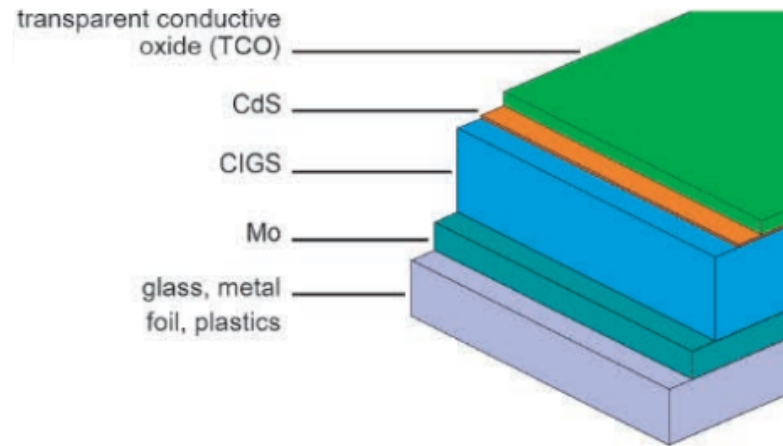


Source: From (BRADSHAW; REUTER; HAMACHER, 2013)

Copper-indium-gallium-diselenide (CIGS) is a technology suited for building-integrated PV applications. Also, CIGS is suitable for space applications due to its

property of high radiation resistivity. But, this technology has challenges such as: low open-circuit voltage, high variability of physical properties, geological scarceness of indium for large-scale fabrication. CIGS-based have a band gap voltage of 1.1–1.2 eV, and are 10 to 100 times more efficient at absorbing sunlight than silicon-based cells, which allows structures with a thickness of a few microns (ZENDEHDEL; Yaghoobi Nia; YAGHOUBINIA, 2020). The structure of the CIGS cell is illustrated in Figure 13.

Figure 13 – Structure of a copper-indium-gallium-diselenide (CIGS) PV cell.



Source: From (BRADSHAW; REUTER; HAMACHER, 2013)

There are also emerging technologies for thin-film PV cells, not yet available commercially as of 2021, such as: copper-zinc-tin-sulfide (CZTS), perovskite solar cells (PSCs), organic photovoltaics (OPV), dye-sensitized solar cells (DSCs), and colloidal quantum dot photovoltaics (QDPV). Despite intense research and development, those technologies are not mature enough for a progression to industrial production and commercialization (ZENDEHDEL; Yaghoobi Nia; YAGHOUBINIA, 2020).

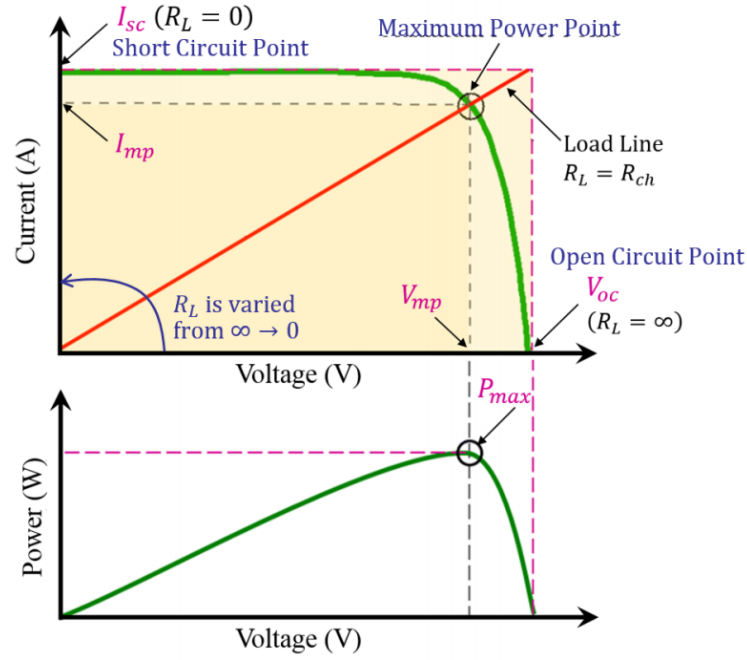
2.1.4.1 CHARACTERIZATION OF PV CELLS

The performance of a photovoltaic cell is mainly dependant on three parameters found in the I-V curve: the short-circuit current (I_{SC}), the open-circuit voltage (V_{OC}), and the maximum power point (V_{MPP}).

The short-circuit current I_{SC} is the current generated with a load impedance of 0 Ω , it is also the current at 0 V. The open-circuit voltage V_{OC} is the voltage at an infinitely high resistance, and the effective current is equal to 0 A. The maximum power point is the point at the I-V curve where the maximum power is reached, and generally, it is between 70% to 80% of V_{OC} . The I-V and P-V curves of a generic PV Cell are illustrated in Figure 14.

The electrical model of a PV cell is effectively a diode with a reverse-biased current source controlled by the flow of electrons due to the light incidence, also resistive losses are

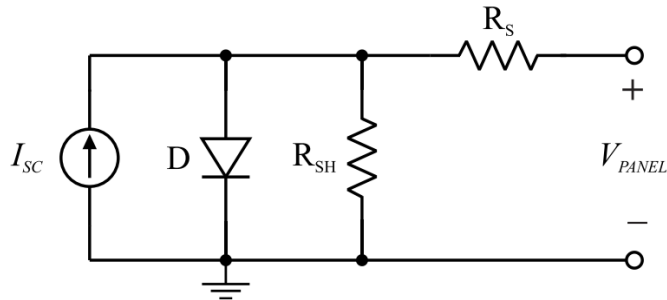
Figure 14 – I-V characteristics of a PV cell.



Source: From (DAS, 2016).

present due to the intrinsic construction of the PV cell. This electrical model is illustrated in Figure 15.

Figure 15 – Simplified electrical model for a PV cell.



Source: From (ZAMPARETTE, 2017).

In Silva (2020) and Monteiro et al. (2022a), the electrical model from Figure 15 is used in order to emulate a real photovoltaic cell in SPICE-based simulators such as Spectre, Hspice, and others. Many techniques can be implemented in order to obtain the parameters for the electrical model, such as approximations using Bisection, Newton-Raphson, or other similar methods, as demonstrated in Rasheed and Shihab (2019).

2.2 SWITCHED-CAPACITOR DC-DC CONVERTERS

As previously explained in Chapter 1, DC-DC voltage converters are widely used to produce a regulated voltage from unregulated or non-constant voltage sources, such as harvested energy from photovoltaic cells, TEGs, and piezoelectric generators. Thus, the voltage converter interfaces the unregulated source to voltage rails in an electronic system that requires a certain voltage (Van Breussegeem; STEYAERT, 2013).

There are two types of switched-mode converters: switched-inductor and switched-capacitor. In this chapter, the switched-capacitor DC-DC converter will be predominantly discussed, because it is best suited for integrated implementation.

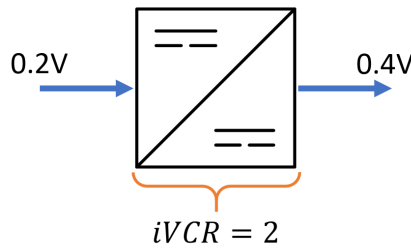
Switched-capacitor DC-DC converters have an extensive list of applications, from System-on-Chip (SoC) to energy harvesting applications. Regardless of the application, the function of a DC-DC voltage converter is to convert a DC voltage to another DC voltage. In Energy Harvesters, voltage converters are used to convert the unregulated voltage generated from a transducer to a regulated output voltage. This case is exemplified in Silva (2020), Zamparette (2017), and Devaraj et al. (2019).

The most important static characteristics found in DC-DC voltage converters are: voltage conversion ratio (VCR), efficiency and noise (Van Breussegeem; STEYAERT, 2013).

2.2.1 VOLTAGE CONVERSION RATIO (VCR)

Each DC-DC converter topology has a fixed ideal voltage conversion ratio (iVCR). The iVCR considers a theoretical efficiency of 100%, but it is unfeasible in real applications due to ohmic losses in the converter. The voltage conversion considering the iVCR is illustrated in Figure 16 (Van Breussegeem; STEYAERT, 2013).

Figure 16 – iVCR of a DC-DC converter.



Source: Author.

The actual VCR of a converter is dependant on the efficiency of the converter and is obtained by the ratio of output voltage and input voltage, as defined in Eq. 2.5 (Van Breussegeem; STEYAERT, 2013).

$$VCR = \frac{V_{OUT}}{V_{IN}} \quad (2.5)$$

The output voltage is defined as the multiplication of the input voltage and the VCR, given by:

$$V_{OUT} = V_{IN} \cdot VCR \quad (2.6)$$

If $VCR > 1$, it is called a step-up converter, otherwise, if $VCR < 1$, it is a step-down converter.

2.2.2 EFFICIENCY

The efficiency η is a ratio between the output power and the input power, as defined in Eq. 2.7.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{LOSS} + P_{OUT}} \quad (2.7)$$

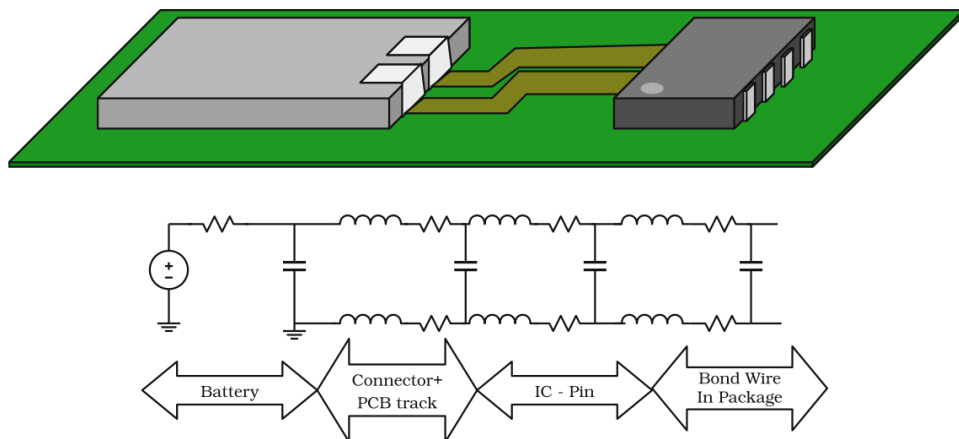
There are no power losses in DC-DC converters with ideal components, but real components introduce resistive loads, and the electrical power is partially lost into heat, hence the power loss. Although, there are many more parameters to be analyzed.

2.2.3 NOISE

Noise can be introduced by the path taken from the source to the load. Most voltage sources have an output impedance that varies in regards to the energy density. Every electrical device can be modeled into an RLC circuit due to its parasitic elements (resistance, capacitance, inductance).

As an example, the connection of a battery connected to an integrated chip is illustrated in Figure 17.

Figure 17 – Lumped model of the connections between a battery and a chip in a PCB.



Source: From (Van Breusseger; STEYAERT, 2013).

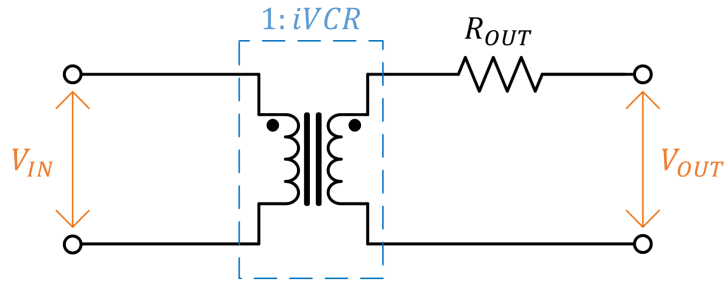
Parasitic elements from every device in the path from the source to the chip are illustrated in the lumped model. The source is modeled as an ideal voltage source with variable resistance, as explained before. Even the PCB tracks, the pins of the integrated

chip, the internal bond-wiring in the chip package introduce those RLC elements. If a varying current flows through that circuit, the voltage becomes the sum of a DC component and an AC signal, whereas the latter is called the input noise. Similarly, at the output of a DC-DC converter, non-zero impedance and pulsating currents introduce noise.

2.2.4 ELECTRICAL MODEL OF SC DC-DC CONVERTERS

The switched-capacitor DC-DC voltage converter can be modelled as a transformer with an ideal conversion ratio and an output resistance, as illustrated in Figure 18.

Figure 18 – Simplified electrical model of a DC-DC Converter.



Source: Author.

The losses are represented by the output resistance R_{OUT} . Those losses are attributed to conduction losses, and losses from the charging and discharging of capacitors. The output resistance can be dominated by capacitance or resistance, through the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL), respectively. Both the SSL and FSL resistances can be obtained through the Charge Flow Analysis (SEEMAN, 2006).

The charge flow analysis can be used to identify individual quantities of charge flowing in each switch and capacitor present in the SC converter (SEEMAN, 2006; Van Breussegem; STEYAERT, 2013).

The analysis is performed for each operation state (phase) using Kirchhoff's current law (KCL) to obtain the normalized charge multipliers a_i^j , as shown in Eq. 2.8, in which $q_i^{(j)}$ is the charge flow in component i during state j and q_{out} is the charge delivered to the output.

$$a_i^{(j)} = \frac{q_i^{(j)}}{q_{out}} \quad (2.8)$$

Due to the principle of electric charge conservation, the sum of all individual charges flowing in each component should be equal to zero. The Charge Flow Analysis is divided into two modes: slow and fast switching limits (SEEMAN, 2006).

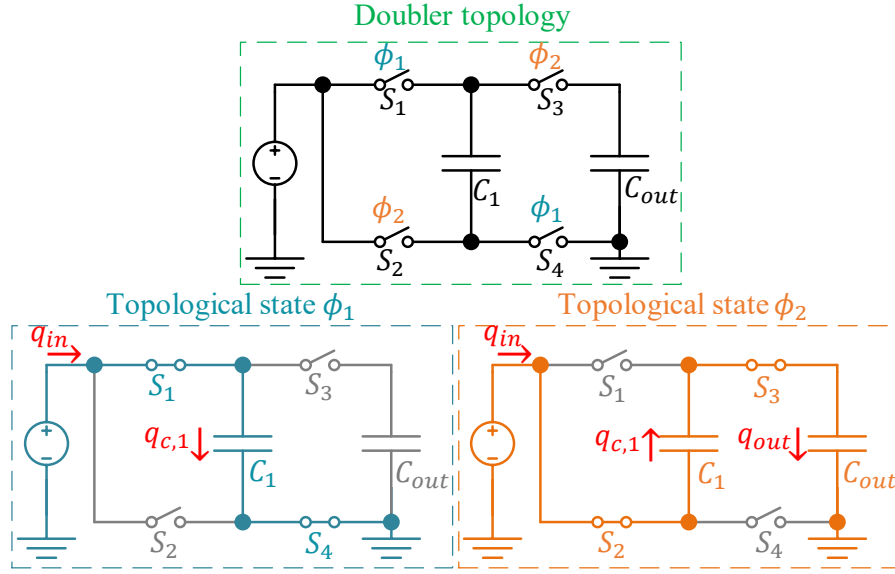
The Slow Switching Limit (SSL) occurs when the switching frequency is sufficiently slow that the charge in each flying capacitor fully equilibrates during each state. Due to

this, finite resistances from the switches and capacitors are ignored, because they are not large enough to prevent the capacitor from fully charging (SEEMAN, 2006).

The Fast Switching Limit (FSL) is the opposite of SSL, since the on-state resistances from switches are large enough that flying-capacitors can not approach equilibrium during a switch period (Van Breussegeem; STEYAERT, 2013).

As an example of Charge Flow Analysis, consider the generic SC doubler topology shown in Figure 19.

Figure 19 – Charge flow analysis in Doubler topology.



Source: Author.

In the topological state ϕ_1 , the charge q_{in} flows from the source to the fly capacitor C_1 . In state ϕ_2 , C_1 is connected in series with the input voltage and the charge $q_{c,1}$ flows from the fly capacitor C_1 to the buffer capacitor C_{load} .

In SSL mode, the resistances from all components are ignored during the extraction of capacitor charge multiplier vectors.

The vectors are given by Eq. 2.9, where the components $a_{out}^{(j)}$, $a_{in}^{(j)}$ and $a_{c,1}^{(j)}$ are the charge multipliers in the state j for output, input and C_1 , respectively.

$$a_c^{(j)} = \begin{bmatrix} a_{out}^{(j)} & a_{c,1}^{(j)} & a_{in}^{(j)} \end{bmatrix} \quad (2.9)$$

Based on Eq. 2.10 and Eq. 2.8, it is possible to obtain the ideal converter VCR (iVCR), as shown in Eq. 2.11 (Van Breussegeem; STEYAERT, 2013).

$$a_c^{(1)} = [0, 1, 1], \quad a_c^{(2)} = [1, -1, 1] \quad (2.10)$$

$$iVCR = \frac{q_{in}}{q_{out}} = a_{in}^{(1)} + a_{in}^{(2)} = 2 \quad (2.11)$$

The Slow Switching Limit converter output resistance is given by Eq. 2.12, where n is the number of charge-transfer capacitors, f_{sw} is the switching frequency, C_i is the capacitor i , and $a_{c,i}$ is the charge flow in the capacitor i .

$$R_{SSL} = \sum_{i=1}^n \frac{(a_{c,i})^2}{C_i \cdot f_{sw}} = \frac{1}{C_1 f_{sw}} \quad (2.12)$$

In FSL mode, switch charge multiplier vectors are obtained according to the charge flowing through the switches. The vectors are given by Eq. 2.13, where $a_{r,i}^{(j)}$ is the charge flow during state j for the switch i . It results in Eq. 2.14 for the analyzed doubler converter.

$$a_r^{(j)} = [a_{r,1}^{(j)}, a_{r,2}^{(j)}, a_{r,3}^{(j)}, a_{r,4}^{(j)}] \quad (2.13)$$

$$a_r^{(1)} = [1, 0, 0, 1], \quad a_r^{(2)} = [0, 1, 1, 0] \quad (2.14)$$

The Fast Switching Limit resistance is given by Eq. 2.15, where n is the number of switches, D_i is the duty cycle in switch i , $a_{r,i}$ is the charge flow multiplier in switch i , and R_i is the on-state resistance in switch i .

$$R_{FSL} = \sum_{i=1}^n \frac{(a_{r,i})^2 \cdot R_i}{D_i} = \frac{4R_{on}}{D} \quad (2.15)$$

Switches are assumed to have equal resistances and duty-cycles in Eq. 2.15, therefore R_{on} is the on-state resistance of a single switch.

An exact value for output equivalent resistance may be difficult to obtain for certain topologies (MAKSIMOVIC; DHAR, 1999; SEEMAN, 2006). An approximation for the output equivalent resistance of a SC Converter is given by Eq. 2.16 (SEEMAN; SANDERS, 2006).

$$R_{out} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} = \sqrt{\frac{1}{C_1^2 f_{sw}^2} + \frac{16R_{on}^2}{D^2}} \quad (2.16)$$

2.3 TOPOLOGIES OF SC DC-DC CONVERTERS

The topology of a switched-capacitor converter describes the structure and interconnection of the components in a converter through a circuit's netlist or a schematic diagram. Switched-capacitor DC-DC converters have different topological states where the components are interconnected differently (Van Breussegeem; STEYAERT, 2013).

Topologies of SC converters can be divided into two groups: step-up converters and step-down converters (Van Breussegeem; STEYAERT, 2013). A multi-topology converter is able to incorporate both step-up and step-down converters in a single SC converter, as demonstrated by Silva (2020).

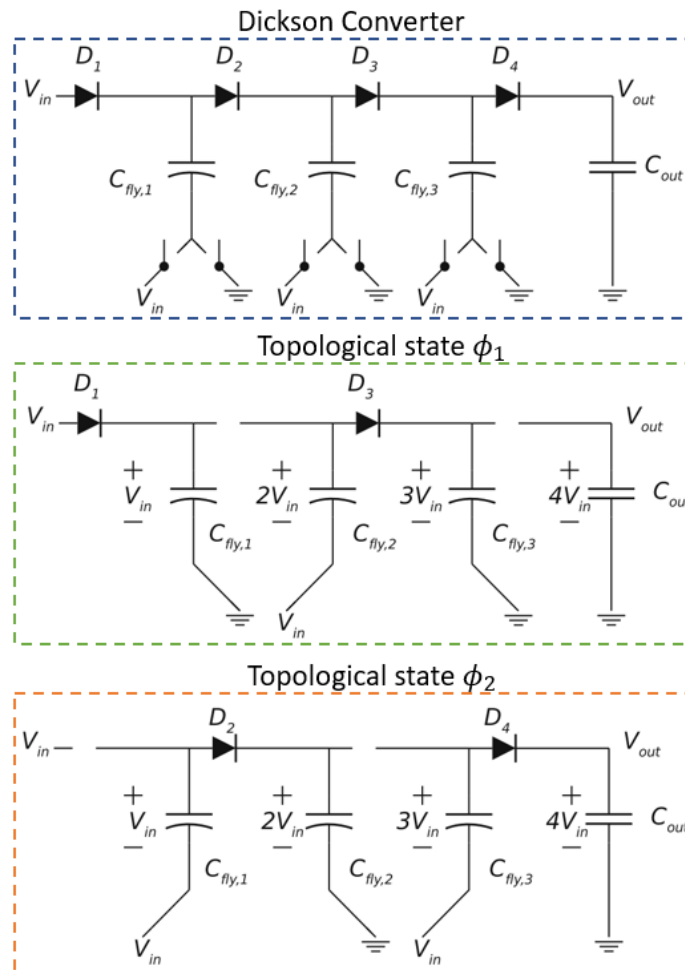
2.3.1 STEP-UP SC CONVERTERS

Step-up converters have an ideal voltage conversion ratio ($iVCR$) higher than one, and many topologies fall under this category, such as parallel-series converters and Dickson converters.

2.3.1.1 DICKSON CONVERTER

The Dickson Converter was introduced from the need for generation of high voltages on integrated circuits. It originates from the Greinacher/Cockcroft–Walton Multipliers, both are AC/DC converters that have a series connection of capacitors. The Greinacher converter proved to be very sensitive to large parasitic capacitances to the substrate. The Dickson Converter consists of capacitors in a parallel configuration as opposed to the Greinacher Multiplier. It has a lower input impedance and is less sensitive to parasitic elements. A Dickson Converter is illustrated in Figure 20 (Van Breussegem; STEYAERT, 2013).

Figure 20 – Three-stage dickson topology.



Source: Adapted from (Van Breussegem; STEYAERT, 2013).

In the first topological state ϕ_1 , the odd-numbered diodes D_1 and D_2 conduct and transfer charges in the direction of the load. In the second topological state ϕ_2 , the even-numbered diodes conduct but the odd-numbered diodes block (Van Breussegeem; STEYAERT, 2013).

In Chouhan and Halonen (2014) and Ballo, Grasso and Palumbo (2020), Dickson converters are implemented with diode-connected transistors, instead of diodes, also biasing techniques are used in order to decrease threshold voltages.

2.3.1.2 PARALLEL-SERIES CONVERTER

Many topologies of step-up converters found in the literature are parallel-series converters. Basically, in the first topological state of a parallel-series converter, the capacitors are in parallel and are charged by the input voltage. On the second topological state, the capacitors are in series and are discharged. The iVCR of converters based on this method is equal to $(n + 1)$, where n is the number of flying capacitors (Van Breussegeem; STEYAERT, 2013). A few topologies are developed through this method, such as the voltage doubler and voltage tripler.

The Voltage Doubler is a very common switched-capacitor converter based on the parallel-series technique, and it has an ideal voltage conversion ratio (iVCR) of two. One of the advantages of this converter over the Dickson converter is that an exponential increase is obtained by cascading multiple stages of voltage doublers, in contrast to the linear increase found in the Dickson topology (Van Breussegeem; STEYAERT, 2013; STARZYK; JAN; QIU, 2001). The voltage doubler consists of a single flying capacitor, although, more than one flying capacitor may be needed in some applications, especially in multi-topology converters such as (SILVA, 2020). In Section 2.2.4, the topological phases of the voltage doubler are explained.

The Voltage Tripler is also based on the parallel-series technique, and has an ideal voltage conversion ratio (iVCR) of three. It has the same working principle as the doubler, but requires a minimum of two capacitors.

2.3.2 STEP-DOWN SC CONVERTERS

Step-down converters have an ideal voltage conversion ratio (*iVCR*) lower than one, and many topologies fall under this category, such as series-parallel and ladder converters.

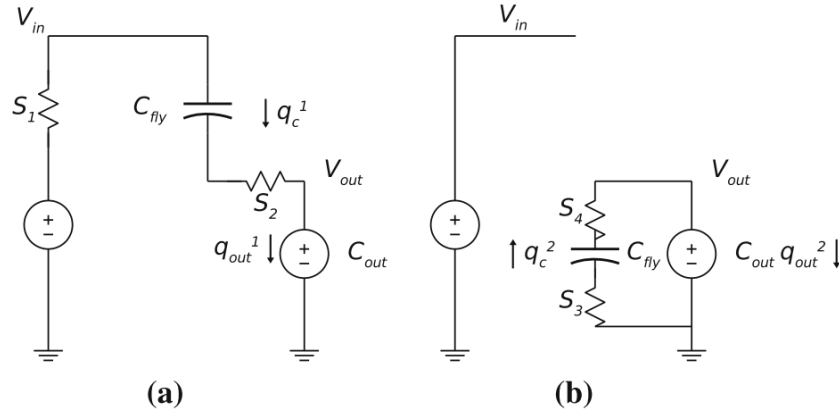
2.3.2.1 SERIES-PARALLEL CONVERTER

The series-parallel converter is the counterpart to the parallel-series converter. At the first topological state, the capacitors are in series and are charged by the input voltage. At the second topological state, the capacitors are in parallel and are connected to the

output. The iVCR of those converters are defined as $1/(n + 1)$, where n is the number of flying capacitors (Van Brussegeem; STEYAERT, 2013).

The Voltage Divider is a type of series-parallel converter that has an iVCR of $1/2$. As in the voltage doubler topology, the voltage divider can also be cascaded to obtain an exponential decrease in voltage. As illustrated in Figure 21, this SC converter requires a minimum of one flying capacitor, and four switches (Van Brussegeem; STEYAERT, 2013).

Figure 21 – Voltage divider topology.

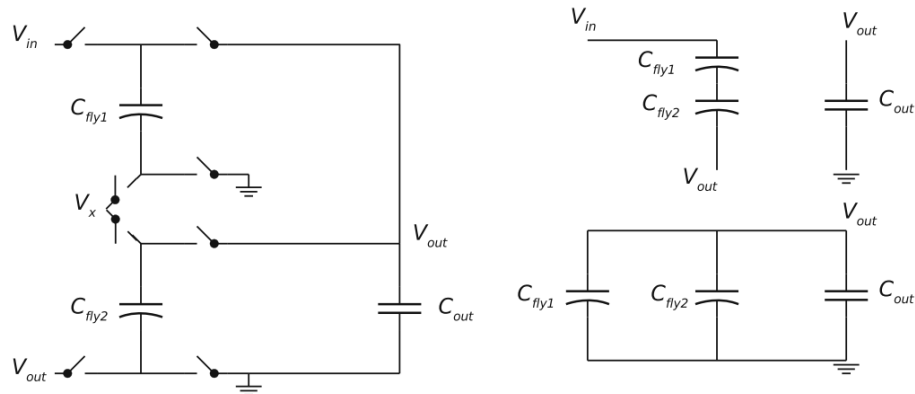


Source: Adapted from (Van Brussegeem; STEYAERT, 2013).

In the first topological state ϕ_1 , switches S_1 and S_2 are closed and the capacitor C_{fly} is put in series with the input source and is charged. In the second topological state ϕ_2 , switches S_3 and S_4 are closed, and the capacitor C_{fly} is in parallel with the output, and ideally delivers $1/2$ of the voltage at the input. This converter is used in many energy harvesters, such as in Silva, Severo and Girardi (2020),

An $1/3$ converter can deliver an iVCR equal to $1/3$. As illustrated in Figure 22, this SC converter requires a minimum of two flying capacitors, and six switches (Van Brussegeem; STEYAERT, 2013).

Figure 22 – $1/3$ topology.



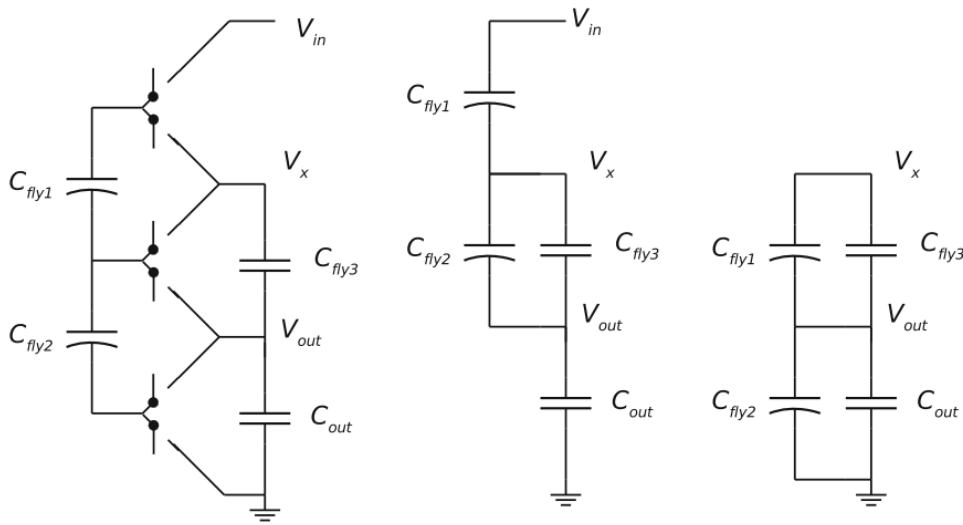
Source: Adapted from (Van Brussegeem; STEYAERT, 2013).

This converter is incorporated into a multiple topology converter with multiple VCRs in Devaraj et al. (2019) for application in an Energy Harvester.

2.3.2.2 LADDER CONVERTER

The ladder converter consists of two strings of capacitors in series that "slides" the connections of the flying capacitors on each topological state. This converter has an $iVCR$ equal to $2/(n + 3)$, where n is the number of flying capacitors (Van Brussegeem; STEYAERT, 2013). The ladder converter is illustrated in Figure 23.

Figure 23 – Ladder topology.



Source: From (Van Brussegeem; STEYAERT, 2013).

The first topological state charges the flying capacitors with the input voltage, and the second topological state discharges the capacitors in direction of the load.

This converter is considered a multiple-output converter because a different DC voltage can be obtained from several nodes. Although, the output resistance is severely impacted by any external loading on those nodes (Van Brussegeem; STEYAERT, 2013).

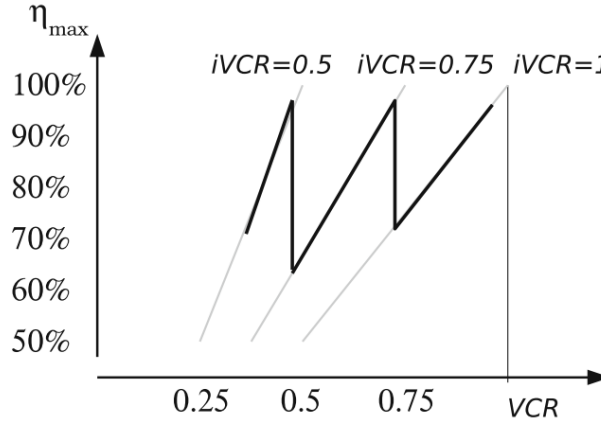
2.3.3 MULTI-TOPOLOGY CONVERTERS

Topologies of switched-capacitor converters have static $iVCR$, a specification that limits the input-output range of the conversion and efficiency. Multiple topologies can be combined into a single converter with selectable modes, for more flexibility with $iVCR$ s and a broader input-output range of conversion (Van Brussegeem; STEYAERT, 2013). Another advantage is that the topologies can share flying capacitors to reduce silicon area.

The efficiency of a converter topology drops if the input or output voltage values cause the VCR to differ from the $iVCR$. Multi-topology converters can improve this by a combination of multiple conversion ratios. Figure 24 illustrates a graph showing the

efficiency as a function of the VCR of a multi-topology converter with iVCRs of 0.5, 0.75, and 1. It is observed that, in all of the topologies that compose the converter, the efficiency drops significantly when the VCR deviates from the iVCR. The advantage of the multi-topology approach is that more iVCRs can be included, and thus, the converter can maintain high efficiency.

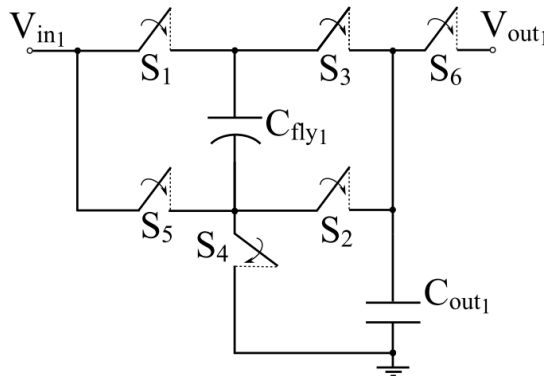
Figure 24 – Potential efficiency by using a multi-topology converter.



Source: From (Van Breussegem; STEYAERT, 2013).

One of the proposed building blocks in Silva (2020) is a Doubler/Divider converter, a multi-topology converter that can either double or divide the input voltage, depending on the selected mode. The converter contains a single flying capacitor that is shared between both topologies. Also, another multi-topology converter called Adder/Subtractor is also proposed and follows the same logic. The Doubler/Divider converter is illustrated in Figure 25.

Figure 25 – Multi-topology converter with iVCRs of 2 and 1/3.

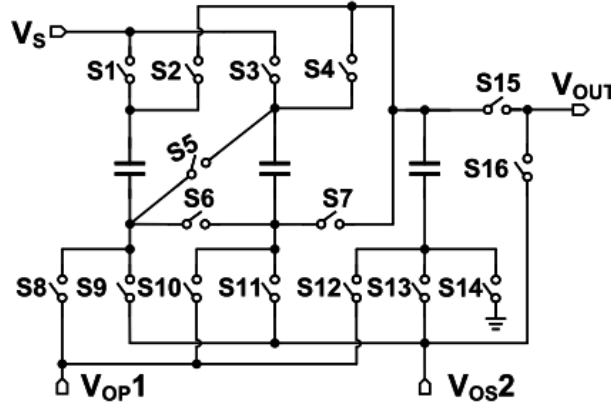


Source: From (SILVA, 2020).

Devaraj et al. (2019) proposes a multi-topology converter with integer values iVCRs of 1, 2, and 3. This converter can bypass the input to the output (for a unitary

iVCR), double and triple the input voltage, depending on the selected mode. Another multi-topology converter with fractional values of $1/3$ and $2/3$ is also proposed and follows the same logic. The integer converter is illustrated in Figure 26.

Figure 26 – Multi-topology converter with iVCRs of 1, 2 and 3.



Source: From (DEVARAJ et al., 2019).

2.4 SC CONVERTERS FOR ENERGY HARVESTERS

A few state-of-the-art DC-DC converters for application in Energy Harvesters are compared in Table 3.

Table 3 – Comparison of Energy Harvesters.

	Converter Type	Number of VCRs	Peak Efficiency	Input Voltage (V)	Output Voltage (V)	Energy Source	Area (mm^2)
(SILVA, 2020)	Up/down	19	90.78%	0.05–1.6	0.4	Indoor Light	0.414
(DEVARAJ et al., 2019)	Up/down	11	74.6%	0.55	1.8–2.5	Piezo/Light	0.47
(YI et al., 2018)	Up	1	45%	0.15–0.2	0.87	Thermal/Light	0.032
(CHENG et al., 2020)	Up	3	68.5%	0.45–0.9	1.5	Indoor Light	1.69

Source: Author.

Silva (2020) presents a multi-topology converter with 19 different iVCRs, from $1/2$ up to 8. The converter contains two strings of stages of Doubler/Dividers to increase the conversion ratio, and an Adder/Subtractor to add or subtract the two strings of converters into a single voltage.

Devaraj et al. (2019) presents a multi-topology converter with 11 iVCRs, from $1/3$ to $11/3$. This converter is designed for multiple inputs, in this case for a piezoelectric generator and a photovoltaic panel. Each source has its converter block that contains two multi-topology converters, one for integer values of 1, 2 and 3, and one for fractional values of $1/3$ and $2/3$. It also has an adder topology in order to sum the fractional and integer converters to obtain a new iVCR.

Yi et al. (2018) presents a simple three-stage Dickson charge-pump achieving a 1:10 conversion ratio. In this case, a differential bootstrapped ring-oscillator VCO, capable of increasing the voltage swing of switches' driving signal from $-V_{IN}$ to $2V_{IN}$.

Cheng et al. (2020) presents a redistributable SC converter for batteryless IoT devices. It is composed of 16 charge-pump submodules with iVCRs of 1.5 and 2, and a low-dropout regulator (LDO) to trim excess voltage. The submodules redistribute in two stages according to the operating mode (sleep and active modes).

2.5 CONCLUSION

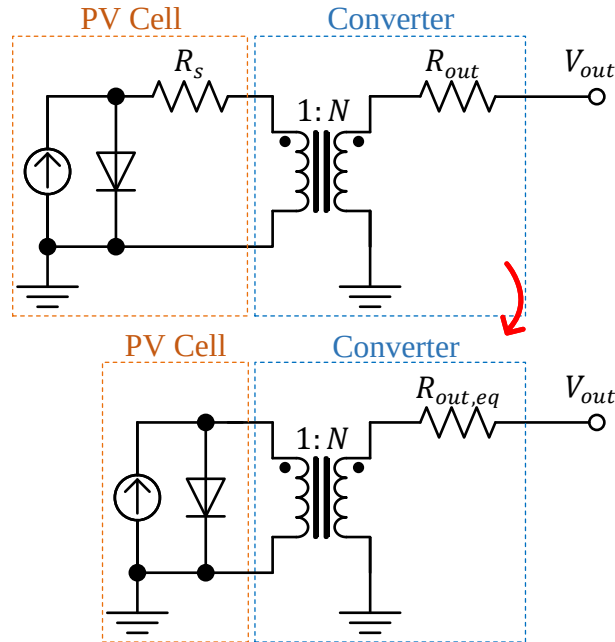
This chapter presents a literature review about the works related to sources of energy suitable for energy harvesting. A comparative analysis between the sources of energy shows that light and thermal energy harvesting are the most dense power-wise, but suffer from availability issues. RF harvesting is reliable but heavily dependant on the distance from the transmitter. Thus, indoor-light harvesting is seen as the suitable approach for low-power applications in an indoor environment, and will work as long as there is an artificial light. Also, this chapter presents an overview about switched-capacitor DC-DC converters, and explains the electrical modelling of the Equivalent Output Resistance through the Charge Flow Analysis. Topologies of SC converters are also presented, from step-up and step-down converters to multi-topology converters. This chapter also presents a comparison between the state-of-the-art DC-DC converters for energy harvesting applications.

3 MODELLING THE EQUIVALENT OUTPUT RESISTANCE

DC-DC voltage converters are widely used for power management of Internet of Things (IoT) devices (GUTIERREZ, 2017). One of the applications is for energy harvesting, in which it is necessary to convert the generated voltage to a regulated output. Energy sources in Energy Harvesting applications are not ideal devices, therefore, a finite series resistance is present in photovoltaic cells, thermoelectric generators (TEGs), and similar transducers. The most common energy sources used in ultra-low power Energy Harvesters are small-sized photovoltaic (PV) cells (SILVA, 2020).

Figure 27 illustrates a generic DC-DC voltage converter with a PV cell connected at the input. The simplified equivalent circuit of a PV cell consists of a current source, a diode, and a series resistance (R_s). The electrical characteristics of the PV cell are dynamically changed according to the illuminance level (SILVA, 2020; MONTEIRO et al., 2022a). As an example, R_s can vary from 2 k Ω to 2.8 k Ω when the illuminance changes from 700 lux to 400 lux in a 20.2 cm² commercial PV cell, as demonstrated in Silva (2020). The generic voltage converter can be modeled using the analogy with an ideal transformer and an output resistance (R_{out}) (SEEMAN, 2006). The transformer voltage ratio (1:N) is equivalent to the converter Voltage Conversion Rate (VCR) (Van Breussegem; STEYAERT, 2013).

Figure 27 – Transformed-based model of a DC-DC voltage converter with a PV Cell connected at its input.



Source: Author.

The R_s resistance in Figure 27 is equivalent to an impedance of $N^2 \cdot R_s$ in series with R_{out} at the secondary due to the transformer (TR) impedance conversion effect. It results in the equivalent output resistance ($R_{out,eq}$) given by:

$$R_{out,eq} = R_{out} + N^2 R_s \quad (3.1)$$

It shows that $R_{out,eq}$ is highly affected by the series resistance present at the converter input, mainly for higher values of VCR. The effects of impedance conversion can be even worse in cascaded converter stages (GUTIERREZ, 2017).

Switched-Capacitor (SC) DC-DC converter topologies are preferred for fully integrated implementation since capacitors are easier to be integrated in CMOS process when compared to inductors. There are some state-of-the-art techniques present in the literature to model SC converters (SEEMAN, 2006; SEEMAN, 2009; Van Breussege; STEYAERT, 2013). The charge flow analysis along with Slow Switching Limit (SSL) and Fast Switching Limit (FSL) are methods that present accurate results (SEEMAN, 2006). However, these methods do not consider the effects of the series input resistance R_s . Additionally, the application of Eq. 3.1 to include the effects of R_s in SC DC-DC converters can present reduced accuracy when higher values of R_s are considered.

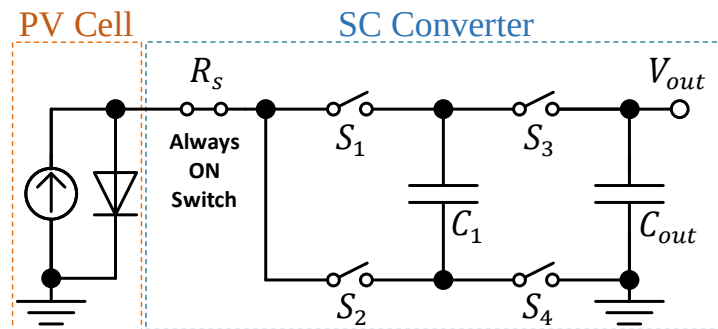
3.1 OUTPUT RESISTANCE CONSIDERING SOURCE RESISTANCE

Section 2.2.4 presented the charge flow analysis to obtain the output resistance of SC converts, considering SSL and FSL. The effects of the input series resistance (R_s) could be analyzed using Eq. 3.1 with the values of R_{out} and N (equal to iVRC) obtained with Eq. 2.11 and Eq. 2.16, respectively. This section presents a more accurate method by considering R_s during the FSL evaluation.

3.1.1 GENERIC METHOD

The proposed generic method is based on considering the source R_s resistance as an always-on switch. It is illustrated in Figure 28, where a photovoltaic cell is connected to the input of the doubler SC converter.

Figure 28 – Doubler with a photovoltaic cell as source.



Source: Author.

The SSL is not affected by the resistances, so R_{SSL} remains equal to Eq. 2.12. The FSL should be analyzed again, by including the charge q_{in} flowing through R_s in both the converter states. Thus, Eq. 2.13 becomes Eq. 3.2, in which $a_{r,R_s}^{(j)}$ is the charge multiplier of R_s .

$$a_{r,eq}^{(j)} = \left[a_{r,R_s}^{(j)}, a_{r,1}^{(j)}, a_{r,2}^{(j)}, a_{r,3}^{(j)}, a_{r,4}^{(j)} \right] \quad (3.2)$$

The FSL resistance could be evaluated by employing Eq. 3.2 in Eq. 2.15, resulting in Eq. 3.3.

$$R_{FSL} = \left(\frac{2R_s + 4R_{on}}{D} \right) \quad (3.3)$$

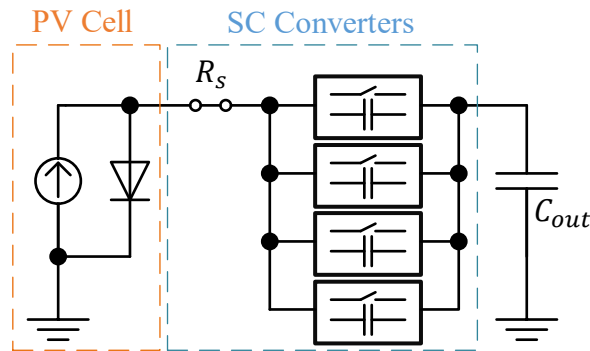
The output equivalent resistance of a SC converter, including the source resistance R_s is given by Eq. 3.4.

$$R_{out,eq} \approx \sqrt{\left(\frac{1}{C_1 f_{sw}} \right)^2 + \left(\frac{2R_s + 4R_{on}}{D} \right)^2} \quad (3.4)$$

3.1.2 COMPLEMENTARY METHOD FOR SYMMETRIC CONVERTERS

Symmetric SC Converters have the benefit of presenting a lower output resistance (MAKSIMOVIC; DHAR, 1999; YING; KI; CHAN, 2003; WANG; YU, 2010). They consist of n converters connected in parallel, as Figure 29 illustrates. Each converter has the same topology and component values but can operate in opposite states (phases).

Figure 29 – Symmetric topology with n converters in parallel.

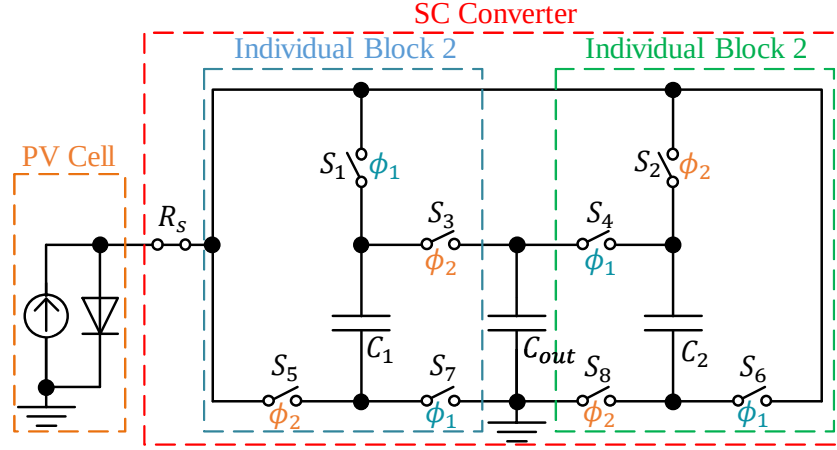


Source: Author.

The generic method, proposed in the last section, can be applied in symmetric SC converters, but the analysis is complex due to the number of elements. Therefore, a complementary method is presented for symmetric topologies.

As an example for a symmetric converter, a cross-coupled doubler is illustrated in Figure 30.

Figure 30 – Cross-coupled Doubler.



Source: Author.

It has two doubler topologies in parallel, therefore, $n = 2$. The source resistance R_s is shared by the individual blocks and is considered as a parallel resistance. Thus, the individual block series resistances ($R_{s,IndividualBlock}$) can be considered as n times R_s , as shown in Eq. 3.5.

$$R_{s,IndividualBlock} = nR_s \quad (3.5)$$

The Generic Method is applied for the individual block to obtain the output equivalent resistance. The output equivalent resistance for the complete block is obtained by dividing the output equivalent resistance for the individual block by n , as shown in Eq. 3.6.

$$R_{out,eq} = \frac{R_{out,IndividualBlock}}{n} \quad (3.6)$$

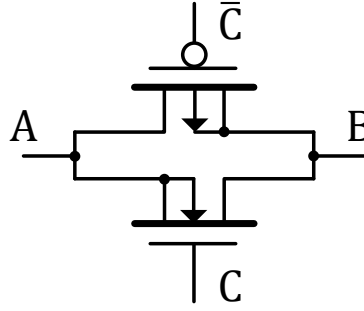
This method can be used for symmetric converters that consider a source resistance. Although, it assumes that all individual blocks are equal, otherwise it does not apply.

3.2 NON-LINEAR SWITCHES

Ideal switches with low on-state resistances were used in previous sections, but a practical use, MOSFETs can be implemented as switches. There are a few topologies of MOSFET-based switches, such as monolithic switches (P-channel and N-channel MOS Switches) and Transmission Gates (CMOS Switches) (ALLEN; HOLBERG, 2002).

Transmission Gates are composed of N-channel and P-channel MOSFETs in parallel, as illustrated in Figure 31. If the bulk is connected to ground, the threshold voltage (V_T) of the transistors will change, as the voltage between source and bulk (V_{SB}) increases. Therefore, to keep the V_T constant, the bulk of both transistors has to be connected to its source terminal. At layout level, a deep n-well is necessary to isolate the bulk of the NMOS transistor from the p-type substrate.

Figure 31 – CMOS Switch.



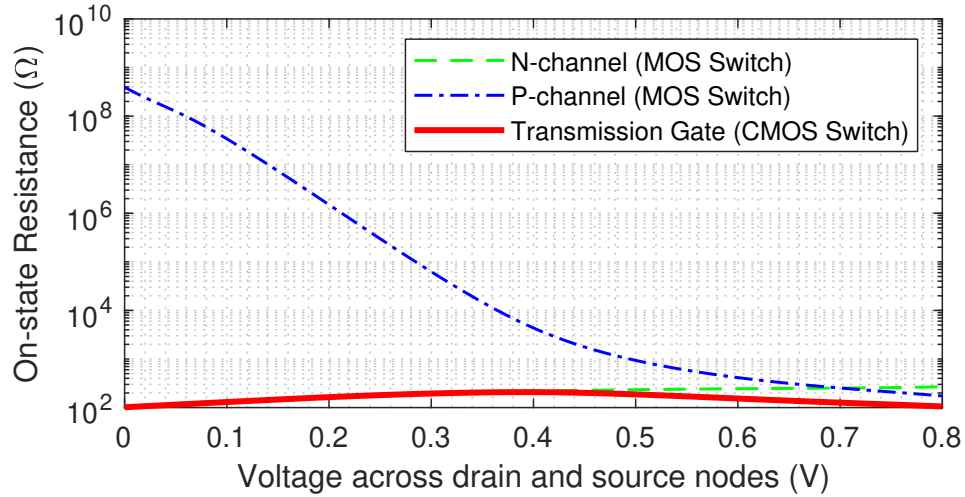
Source: Author.

P-channel MOSFET have inferior carrier mobility (μ_p) than its N-channel counterpart (μ_n), therefore, to compensate the current, the width of the P-channel MOSFET is increased by a factor of 2.7 for the TSMC 180nm technology.

TSMC 180nm technology has an operating voltage up to 1.8 V. Although, for Ultra-Low Voltage purposes, this voltage (V_{DD}) is dropped to 800 mV. To reduce the distortion due to the low V_{DD} , the CMOS switches use with a total of 8 fingers with $W_n = 2 \mu m$ and $W_p = 5.4 \mu m$, and $L = 180 nm$.

Figure 32 shows the resistance as function of the voltage across the A and B nodes, and compares monolithic NMOS, PMOS and a CMOS switch.

Figure 32 – On-state resistance as function of the voltage across the switch.



Source: Author.

To properly model the CMOS switches into the SC Converter, the R_{on} is equal to the on-state resistance when $V_{DS} = V_{CR} \cdot V_{in}$. As shown in Figure 32, the on-state resistance of CMOS switch varies less than monolithic switches due to the parallel implementation of both NMOS and PMOS transistors, effectively decreasing the resistance (ALLEN; HOLBERG, 2002).

The maximum efficiency for a SC Converter is achieved when the Slow Switching Limit and Fast Switching Limit resistances tend to be equal (SILVA, 2020).

The optimal frequency for a given capacitance can be obtained through Eq. 3.7.

$$f_{sw,optimal} = \frac{1}{C_{fly} \cdot R_{FSL}} = \frac{1}{C_{fly} \cdot (4R_s + 8R_{on})} \quad (3.7)$$

3.3 RESULTS

Both methods proposed in the Section 3.1 are compared to the transformer-based model shown in Eq. 3.1. We use SPICE electrical simulation as a golden model for evaluating the quality of the analytical methods. Simulations were performed using a resistive switch model with on-state resistance equal to 100 Ω . Flying-capacitors and buffer-capacitors are 200 pF and 10 nF, respectively. The analysis was executed for R_s equal to 200 Ω , 2 k Ω , and 20 k Ω .

Table 4 shows the obtained results for $R_{out,eq}$ at $f_{sw} = 5$ MHz, for the voltage doubler of Figure 28 and the cross-coupled doubler of Figure 30. Additionally, to validate the method with $VCR < 1$, an SC divider topology presented in Van Breussegem and Steyaert (2013) is also used.

Table 4 – Comparison results of the proposed method with the transformer-based method and SPICE simulations.

Topology ^a	RS ^b (k Ω)	OER ^c (k Ω)			Error		SSL	FSL
		Our	TBM	SS	Our	TBM		
CCDOU	0.2	1.296	1.432	1.280	1.25%	10.66%	29%	71%
	2	8.414	8.632	8.480	0.78%	1.77%	6%	94%
	20	80.401	80.632	80.500	0.12%	0.16%	1%	99%
DOU	0.2	1.876	2.065	1.825	2.74%	11.64%	38%	62%
	2	8.854	9.265	8.865	0.12%	4.32%	10%	90%
	20	80.805	81.265	81.100	0.36%	0.20%	1%	99%
DIV	0.2	0.387	0.366	0.367	5.26%	0.18%	45%	55%
	2	1.224	0.816	1.260	2.88%	54.35%	17%	83%
	20	10.202	5.316	10.400	1.93%	95.62%	2%	98%

^a CCDOU: Cross-coupled Doubler; DOU: Doubler; DIV: Divider.

^b RS: Source Resistance.

^c OER: Output Equivalent Resistance; TBM: TR-Based Method; SS: SPICE Simulation.

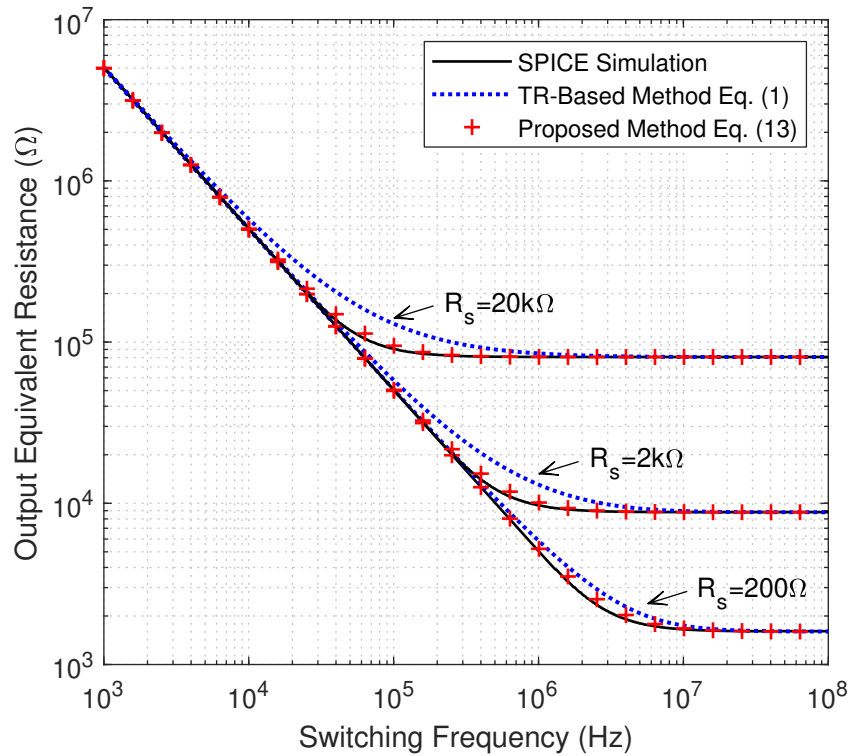
Source: Author.

The maximum error of our proposed method is 1.25%, 2.74%, and 5.26% for the cross-coupled, doubler, and divider topologies, respectively. In contrast, the transformer-based method presents maximum errors of 10.66%, 11.64%, 95.62% for the same topologies. These results show the high precision of the proposed method. Further comparisons show that the error increases in both methods as the percentage of SSL resistance is increased, although our method has a relatively smaller increase. It should also be noted that the

transformer-based method does not model topologies where the source resistance is isolated from the SC converter in any topological state – for example, the divider topology, where the error becomes apparent at higher resistances.

Figure 33 shows a comparison results of the evaluation of $R_{out,eq}$ for the doubler converter, considering the switching frequency variation from 1 kHz to 100 MHz. As can be seen, our proposed method presented results very close to the simulation results in all frequencies for all analyzed values of R_s . Small deviation occurs at the corners due to the limitations of the approximation where SSL tends to be equal to the FSL resistances (Van Breussegeem; STEYAERT, 2013). The transformed-based method presented good accuracy for small and large frequencies, but a higher error at medium frequencies.

Figure 33 – Output Equivalent Resistance as a function of the switching frequency for different values of R_s .

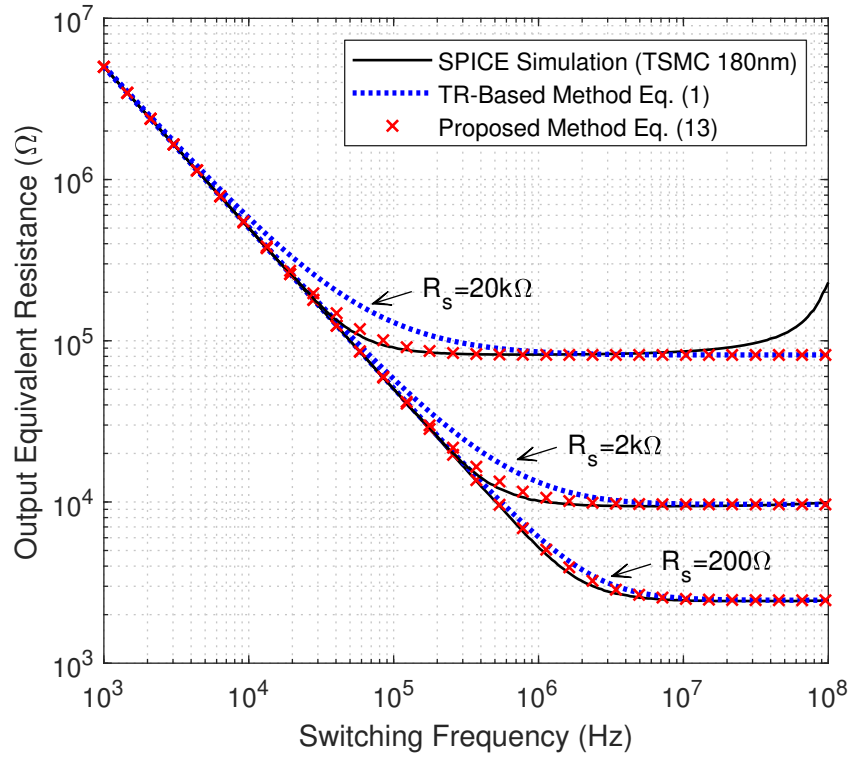


Source: Author.

Figure 34 shows a comparison between the proposed method, the transformer-based method and the resistance obtained through the time constant (τ). The graph proves that the time constant method is valid for a large range of frequencies, although, at very high frequencies, with high resistance, the accuracy drops significantly due to a voltage drop. The voltage drop is present because the control voltage (V_G) supplied to the transistors is 800 mV, as explained in Section 3.2, and makes the transistors slower.

The proposed method models the Output Equivalent Resistance very well, there is a slight increase in error due to the CMOS switches, but it stays within a 10% margin of

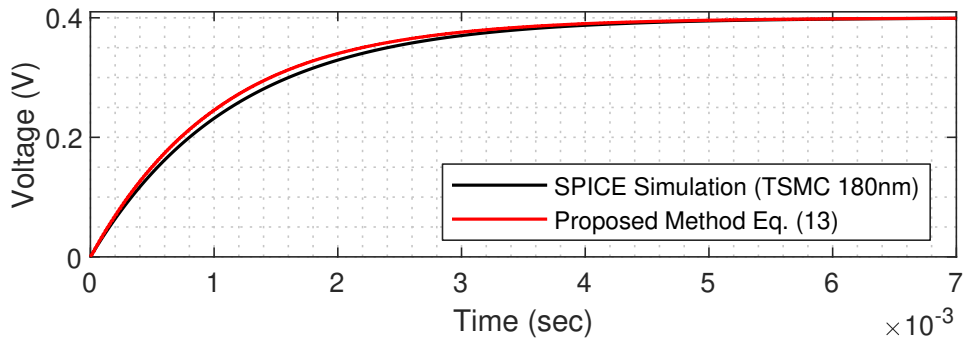
Figure 34 – Output Equivalent Resistance as function of the switching frequency for different values of R_s , using CMOS switches.



Source: Author.

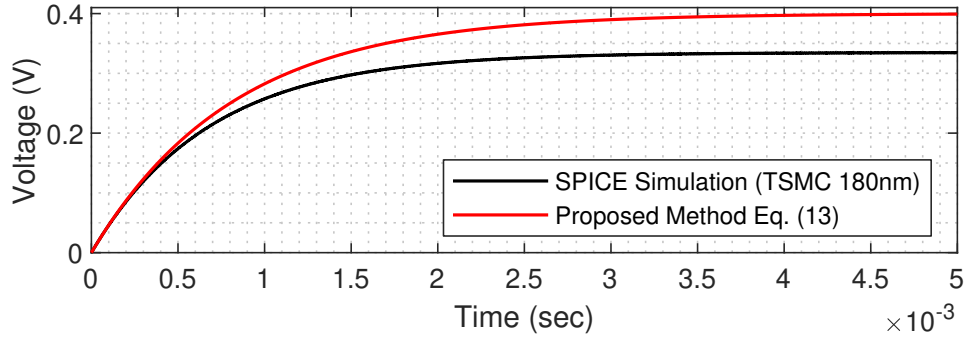
error. The error reaches its peak when $R_{SSL} = R_{FSL}$. It reaches an error of 9.52%, while the TR-based method reached an error of 50.38% in an equal situation.

Figure 35 – Transient voltage for $R_s = 20k\Omega$ and a switching frequency of 61.2 kHz.



Source: Author.

Due to parasitic capacitances in the MOSFETs and low V_{DD} voltage of 800 mV, voltage drops are present at very high frequencies in SC Converters with high resistance, this happens due to parasitic capacitances on the switch MOSFETs and the lower control voltage of 800 mV, therefore, limiting the transistor maximum frequency. This is evidenced in Figure 35 and Figure 36. The latter shows a voltage doubler with a significant voltage

Figure 36 – Transient voltage for $R_s = 20k\Omega$ and a switching frequency of 30 MHz.

Source: Author.

drop on the output with f_{sw} of 30 MHz, while the former is also a voltage doubler with f_{sw} of 61.2 kHz, the optimal frequency for maximum efficiency, calculated through Eq. 3.7. Both SPICE simulations were conducted with a source resistance (R_s) of 20 k Ω .

Table 5 compares three different SC Converters using CMOS switches at their optimal frequency. As expected, the error increases as more parasitic capacitances are inserted into the circuit.

Table 5 – Comparison results of the proposed method with the transformer-based method and Spectre simulations, considering the TSMC 180 nm technology.

Topology ^a	Frequency (MHz)	RS ^b	OER ^c (k Ω)			Error	
			Our	TBM	SS	Our	TBM
CCDOU	1.535	0.2	2.302	2.626	2.136	7.21%	18.67%
	0.283	2	12.48	16.86	11.56	7.37%	31.46%
	0.031	20	114.3	160.8	106.8	6.56%	33.60%
DOU	2.059	0.2	3.473	3.738	3.202	7.80%	14.36%
	0.297	2	13.66	24.91	12.36	9.52%	50.38%
	0.021	20	115.5	240.8	104.9	9.18%	56.44%
DIV	2.593	0.2	0.727	0.595	0.955	23.87%	37.66%
	0.206	2	2	4.22	2.27	11.89%	46.21%
	0.031	20	15.73	41.33	16.67	11.64%	59.67%

^a CCDOU: Cross-coupled Doubler; DOU: Doubler; DIV: Divider.

^b RS: Source Resistance.

^c OER: Output Equivalent Resistance; TBM: TR-Based Method; SS: SPICE Simulation.

Source: Author.

The SC converters remains with an error of less than 10%, except for the divider topology that has a significant error of 23.87% with a low source resistance. This is not a problem if the control voltage V_{DD} is increased from 0.8 V to 1 V. That will decrease the error to 0%, 7.15% and 11.6%, for source resistances of 200 Ω , 2 k Ω and 20 k Ω , respectively.

3.4 CONCLUSION

This chapter proposed a method to model the output equivalent resistance of Switched-Capacitor DC-DC Converters, considering the effects of the source resistance.

The proposed method considers the source resistance as an always-on switch in the Charge Flow Analysis. It makes this method very precise in comparison to the transformer-base method and can also be easily applied in symmetric parallel SC converters.

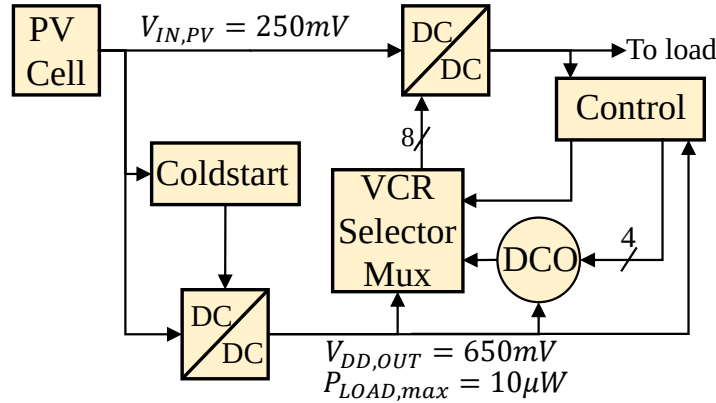
The proposed method was compared to SPICE simulations and presented high accuracy for all analyzed range of switching frequencies (1 kHz to 100 MHz) with different values of source resistances. The maximum errors obtained were 1.25%, 2.74%, and 5.26% for the cross-coupled doubler, doubler, and divider topologies, respectively. The transformer-based method presented errors of 10.66%, 11.64%, and 95.62% for the same topologies.

The proposed method was tested with CMOS switches based on the TSMC 180nm technology. As expected, errors increased as parasitic capacitances were inserted into the circuit. An optimal switching frequency can be adjusted for maximum efficiency when the SSL and FSL resistances are equal. The maximum errors for doubler topologies were less than 10%, although, the divider topology had an error of 23.87% for a low V_{DD} , although, this error can be decreased to less than 1% by increasing V_{DD} to 1 V.

4 PROPOSED ENERGY HARVESTING SYSTEM

This chapter proposes several components of the energy harvesting system, including: a dual-VCR switched-capacitor DC-DC converter with a power output of $20 \mu\text{W}$, with an output voltage of 400 mV for PV cell under low light conditions; a low-power digitally-controlled oscillator with a four-bit control and a frequency range of 0.3 MHz to 5 MHz ; an ultra-low voltage cold-start system to self-start the system. A simplified electrical diagram of the Energy Harvesting system is illustrated in Figure 37.

Figure 37 – Simplified electrical diagram of an indoor-light energy harvesting system for ULV applications.



Source: Author.

4.1 DIGITALLY CONTROLLED OSCILLATOR

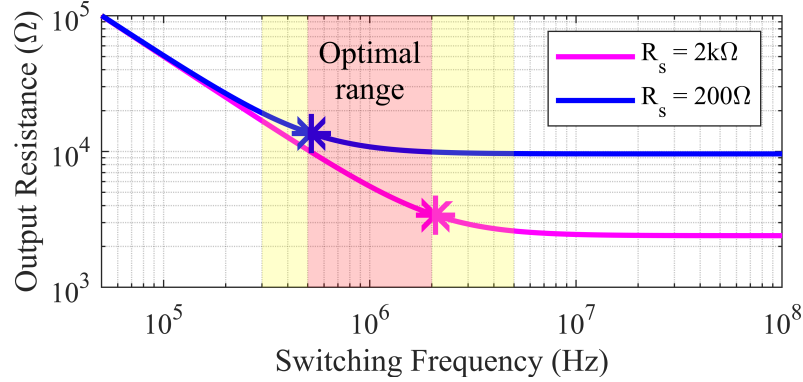
The energy conversion efficiency is one of the main design specification of SC DC-DC converters. According to Silva (2020), the SC DC-DC converter reaches its peak efficiency for a given optimal switching frequency $f_{sw,opt}$. This frequency is determined by the region where the converter equivalent output resistance reaches the Fast Switching Limit (FSL) resistance (SILVA, 2020). It can be estimated through Eq. 4.1, where k is a topological constant, C_{fly} is the flying-capacitance and R_{FSL} is the FSL resistance.

$$f_{sw,opt} = \frac{k}{C_{fly} \cdot R_{FSL}} \quad (4.1)$$

According to Dutra, Girardi and Compassi-Severo (2021), R_{FSL} is a function of switches resistance and input source series resistance (R_s). Figure 38 shows a typical simulation of the output resistance of a SC voltage doubler, for the scenarios where R_s is equal to 200Ω and $2 \text{ k}\Omega$. As shown, in this case, the optimal frequency is found at the range from 500 kHz to 2 MHz .

Consequently, the ability to control the switching frequency (f_{sw}) is an important feature for energy harvesting applications. It can be done by an external signal in analog or digital domain or by means of integrated oscillators. Digitally-Controlled Oscillators

Figure 38 – Output equivalent resistance in a SC Converter with source resistances R_s of $200\ \Omega$ and $2\ \text{k}\Omega$.



Source: Author

(DCOs) are better suited for energy harvester feedback systems, providing precise control and low complexity.

4.1.1 DESIGN AND SIZING OF COMPONENTS

The ring oscillator is among the simplest types of oscillators, and consists of an odd number of cascaded inverters in a closed loop configuration. The outputs of the inverters oscillate from logic high to logic low and vice versa due to the feedback path. The signal is provided at any node in the cascade of inverters (SUNAR; MARTIN; STINSON, 2007). Since there is no stable operation due to the odd number of stages, the oscillation frequency f_{osc} is dependant on the number of stages N and the propagation delay t_p of each inverter (RABAEY; CHANDRAKASAN; NIKOLIC, 2003). The f_{osc} frequency is given by Eq. 4.2.

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_p} \quad (4.2)$$

The propagation delay is given by Eq. 4.3, where C_L is the sum of capacitances connected to the output of the CMOS inverter, such as the output capacitance, input capacitance of next stage and wire capacitance. The $R_{eq,n}$ and $R_{eq,p}$ resistances are the on-state resistance of NMOS and PMOS transistors of the CMOS inverter.

$$t_p = 0.69 \cdot C_L \cdot \left(\frac{R_{eq,n} + R_{eq,p}}{2} \right) \quad (4.3)$$

Based on Eq. 4.2 and 4.3, the oscillation frequency can be adjusted by changing the output capacitance and the on-stage resistance of the CMOS transistors.

The oscillating frequency is heavily dependant on propagation delay. Therefore, any factor that modifies the propagation delay can be used to modify the frequency (RABAEY; CHANDRAKASAN; NIKOLIC, 2003).

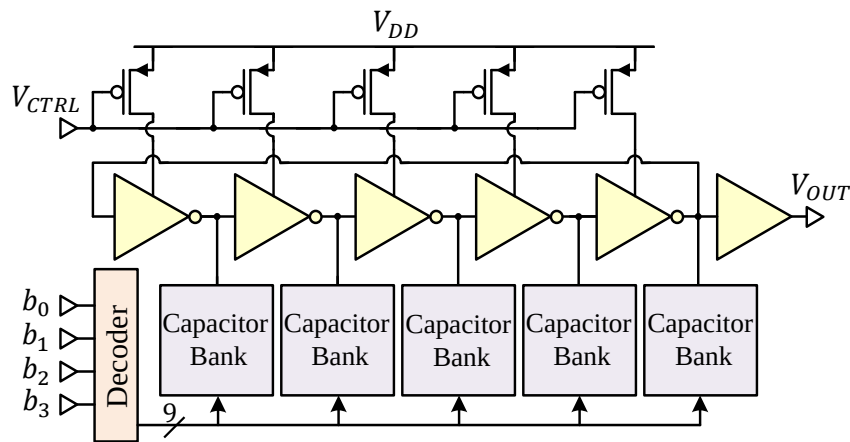
Without modifications on the circuit, a ring-oscillator has a fixed frequency, as there is no way to change the oscillating frequency. The control the oscillation frequency of a ring oscillator can be performed by changing the load of each stage or by changing the circuit supply voltage. In both cases, the inverters propagation delay are modified, resulting in a variation in the oscillation frequency.

One of the simplest ways to control the frequency is to add a current-starving transistor to limit the current passing through the inverters. The current-starved inverters have a limited discharging current for the load capacitance of the gate. By varying the V_{GS} voltage on the current starving transistors, the frequency varies (RABAEY; CHANDRAKASAN; NIKOLIC, 2003). Although, without a closed-loop control, the resulting oscillating frequency is non-linear.

The strategy used in this work is to control the frequency through a configurable capacitive load. Shunt capacitors are switched on and off to modify the capacitive load in each oscillator stage, which leads to a modification in the propagation delay, and consequently in the oscillating frequency (ZHAO; Yong-bin Kim, 2008).

To decrease the power consumption of the circuit, a current-starving PMOS transistor is used. This transistor also provides a coarse adjust in the oscillating frequency, which is useful to avoid the need for larger capacitances, although a reference voltage of around 90 mV is needed to bias the transistor and bring the frequency down to 5 MHz. A transistor with channel width of $1.5 \mu\text{m}$ and channel length of $0.18 \mu\text{m}$ is obtained by adjusting the sizes for low power consumption, and to coarsely adjust the maximum and minimum frequencies. The proposed digitally-controlled ring oscillator is depicted in Figure 39.

Figure 39 – Schematic circuit of the ring-oscillator DCO, showing the CMOS inverter stages, capacitor banks, current-starving transistors and the signal decoder.

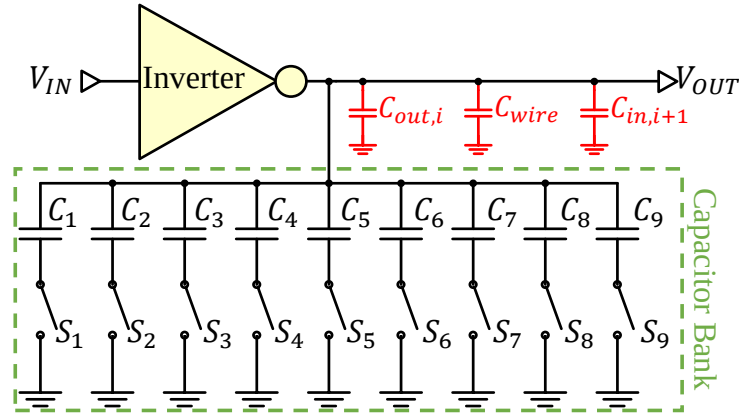


Source: Author

4.1.1.1 CAPACITOR BANK

The Capacitor Bank, shown in Figure 40, is part of the Delay Cell, and is the most important part of the proposed DCO. It is composed of nine capacitors and nine switches. Each capacitor has its top plate connected to the output of the inverter, and the bottom plate connected to a CMOS switch. The switches are controlled by 9 digital control signals decoded from the 4-bit input word. When a switch is closed, the capacitor negative node is connected to ground, contributing to the overall delay capacitance. Otherwise the capacitor has a floating node and does not sum to the total equivalent capacitance.

Figure 40 – Delay cell composed of an inverter, parasitic capacitances and capacitor bank with 9 capacitors and 9 switches, allowing the combination of 16 different load capacitances.



Source: Author

The oscillation frequency does not vary linearly with the capacitive load, as shown in Eq. 4.2. The nine capacitors are combined in order to select an equivalent capacitance which results in a different oscillation frequency. The proposed strategy is to use a reconfigurable capacitor bank with values that can be combined to raise quadratically, in order to output a linear frequency. The lowest code holds the most capacitance, and sets the lowest frequency in the DCO, whereas the highest frequency holds a small amount of frequency. Capacitors of 2.64 pF, 1.5 pF, 600 fF, 300 fF, 150 fF, 150 fF, 60 fF, 30 fF and 30 fF are used to obtain the equivalent capacitance. They are implemented with 2 fF/ μm^2 MIM capacitors from TSMC 180 nm technology. Table 6 shows the combination of capacitors for each digital input code.

The equivalent output capacitance is composed of the intrinsic MOSFET capacitances ($C_{out,i}$), the wire capacitance (C_{wire}) and the input capacitance of the next stage ($C_{in,i+1}$). It affects the propagation delay, which is an issue when the capacitor bank is configured to a small value.

Table 6 – Shunt-capacitor loading combinations.

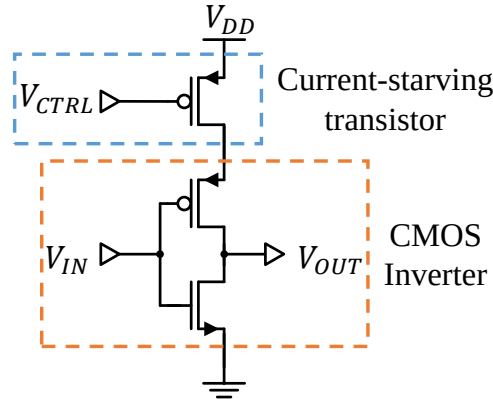
Digital Code	C_1 (fF)	C_2 (fF)	C_3 (fF)	C_4 (fF)	C_5 (fF)	C_6 (fF)	C_7 (fF)	C_8 (fF)	C_9 (fF)	C_{sum} (fF)
0	300	2640	1500	600	150	150	60	30	30	5460
1	300	-	1500	600	150	150	-	-	-	2700
2	300	-	1500	-	-	-	-	-	-	1800
3	300	-	-	600	150	150	60	30	30	1320
4	300	-	-	600	-	150	-	-	-	1050
5	-	-	-	600	-	150	60	30	30	870
6	-	-	-	600	-	150	-	-	-	750
7	-	-	-	600	-	-	-	-	30	630
8	300	-	-	-	-	150	60	30	30	570
9	300	-	-	-	-	150	60	-	-	510
10	300	-	-	-	-	150	-	-	-	450
11	300	-	-	-	-	-	60	30	30	420
12	300	-	-	-	-	-	60	-	30	390
13	300	-	-	-	-	-	-	30	30	360
14	300	-	-	-	-	-	-	-	30	330
15	300	-	-	-	-	-	-	-	-	300

Source: Author.

4.1.1.2 CMOS INVERTER AND CURRENT-STARVING TRANSISTOR

The CMOS inverter is composed of a nominal voltage-threshold (standard transistor) PMOS and an NMOS transistor in the configuration illustrated in Figure 41. The PMOS transistor has a lower carrier mobility than its NMOS counterpart, therefore, to compensate for this, the channel width (W_P) has to be increased by a factor of 3.5. This factor is for a supply voltage V_{DD} of 700 mV.

Figure 41 – Schematic diagram of the CMOS Inverter.

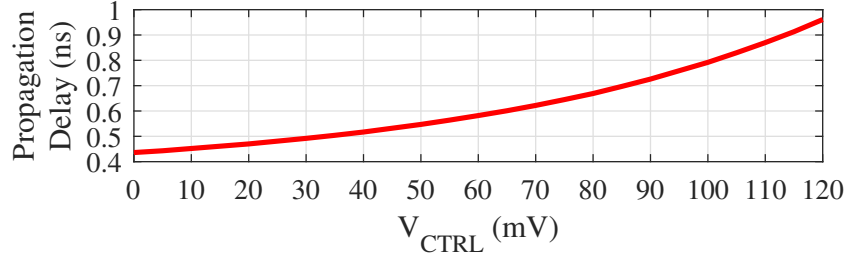


Source: Author

Both transistors have the minimum channel length of $0.18 \mu\text{m}$, whereas the channel

width of the NMOS transistor is $0.3 \mu\text{m}$ and the PMOS is $1.05 \mu\text{m}$. The inverter is directly connected to a current-starving transistor, and the propagation delay in function of the calibration voltage is shown in Figure 42.

Figure 42 – Propagation delay of a single inverter in function of V_{CTRL} voltage.



Source: Author

As shown in Figure 39, a current-starving PMOS transistor is connected to the V_{DD} pin of the CMOS Inverter, and the propagation delay can be adjusted through an external calibration voltage V_{CTRL} that changes the on-resistance of the transistor, as shown in Eq. 4.3. The high-to-low propagation delay is constant, at a steady 103 ps, but the low-to-high propagation delay increases exponentially in response to V_{CTRL} . This transistor has channel width and length of $2 \mu\text{m}$ and $0.18 \mu\text{m}$, respectively. At a calibration voltage V_{CTRL} of 90 mV, the total propagation delay is 726 ps, and at 20 mV, it is 470 ps.

The propagation delay is given by Eq. 4.3, and, as the current-starving is asymmetrical, only the low-to-high delay is affected and can be included in the equation. Also, parasitic capacitances, such as the gate voltage of the next stage must be taken into consideration.

The complete equation for propagation delay including parasitic capacitances is given by Eq. 4.4.

$$t_p(V_{DD}, V_{CTRL}) = 0.69 \cdot (C_{sum} + C_{wire} + C_{out,i} + C_{in,i+1}) \cdot \left(\frac{R_{eq,N} + R_{eq,P}(V_{CTRL})}{2} \right) \quad (4.4)$$

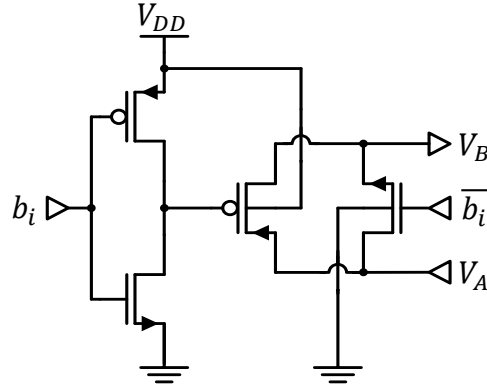
4.1.1.3 CMOS SWITCH

The CMOS switch is composed of an NMOS transistor in parallel with a PMOS transistor. The schematic diagram of the switch is shown in Figure 43, and includes a CMOS inverter to invert the clock signal V_{CLK} for the PMOS transistor.

The NMOS and PMOS transistors have a W/L ratio of $0.3/0.18 \mu\text{m}$ and $1.05/0.18 \mu\text{m}$, respectively. exactly the same as in the designed CMOS inverter for easier placement in the stick diagram of the layout. The on-state resistance of the CMOS switch in function of the voltage across the switch is shown in Figure 60.

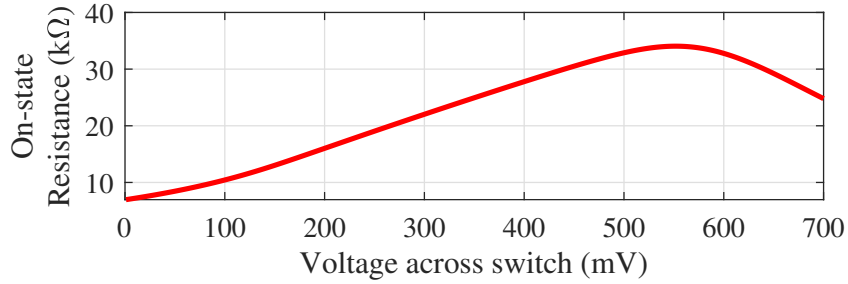
The switch on-state resistance spans from $7 \text{ k}\Omega$ to $34 \text{ k}\Omega$, and can be further linearized through the increase of the channel width of the PMOS transistor.

Figure 43 – Schematic diagram of the CMOS Switch.



Source: Author

Figure 44 – Resistance in function of the voltage across the switch.



Source: Author

4.1.1.4 DECODER

The decoder is a block that converts the four-bit input signal to the nine signals that control the capacitor-loading switches. The truth table can be obtained using Table 6, and based on that, the decoder was implemented using full-custom static logic gates. The logic synthesis was performed with the objective to reduce the decoder silicon area. The solutions for the truth table are shown from Eq. 4.5 to Eq. 4.13 for switches S_1 to S_9 , respectively.

$$S_1 = b_0 + \overline{b_1} + \overline{b_2} + \overline{b_3} \quad (4.5)$$

$$S_2 = \overline{b_0} + \overline{b_1} \cdot \overline{b_2} + \overline{b_3} \quad (4.6)$$

$$S_3 = \overline{b_0} + \overline{b_1} \cdot \overline{b_2} \cdot \overline{b_3} \quad (4.7)$$

$$S_4 = \overline{b_0} + \overline{b_1} + \overline{b_2} + \overline{b_3} \quad (4.8)$$

$$S_5 = \overline{b_0} + \overline{b_1} \cdot (\overline{b_2} + \overline{b_3}) \quad (4.9)$$

$$S_6 = \overline{b_0} + \overline{b_2} + \overline{b_1} + \overline{b_3} \quad (4.10)$$

$$S_7 = (b_3 + \overline{b_2}) \cdot (\overline{b_1} + \overline{b_2}) \cdot (b_0 + \overline{b_1} + \overline{b_3}) \cdot (b_0 + b_1 + b_2 + \overline{b_3}) \cdot (\overline{b_0} \cdot \overline{b_1} \cdot \overline{b_2}) \quad (4.11)$$

$$S_8 = b_1 \cdot \overline{b_2} \cdot b_3 + \overline{b_1} \cdot b_2 \cdot b_3 + \overline{b_1} + \overline{b_2} + \overline{b_3} \quad (4.12)$$

$$S_9 = b_0 \cdot b_1 \cdot \overline{b_3} + \overline{b_0} \cdot b_1 \cdot b_2 + b_1 \cdot \overline{b_2} \cdot b_3 + \overline{b_1} \cdot b_2 \cdot b_3 + \overline{b_1} + \overline{b_2} + \overline{b_3} \quad (4.13)$$

4.1.1.5 CMOS BUFFER

The buffer is composed of two inverters, where the small inverter is the same as the CMOS inverter used in the Ring Oscillator.

To obtain the sizing of the second inverter, a fan-out of 75 gates is considered and simulated to obtain a sizing factor. For a factor of four, there is an insignificant variation with load and no load. Therefore, the channel width (W) of the transistors in the second inverter should be four times larger than in the first.

To maintain a compact layout, the transistors are divided into four fingers.

4.1.2 RESULTS

Figure 45 shows the complete layout of the DCO. It occupies an area of $258 \mu\text{m} \times 135 \mu\text{m}$, and consists of the ring-oscillator and a decoder.

A comparison between schematic and post-layout for the frequency in function of a code is shown in Figure 46.

The linearity error for schematic and post-layout simulations is shown in Figure 47, and considers the ideal frequencies as reference. The Root Mean Square Error (RMSE) of the frequency for schematic simulation is 20.4 kHz with $V_{CTRL} = 90\text{mV}$. For post-layout simulations, the RMSE is 265.3 kHz for $V_{CTRL} = 90\text{mV}$, and 45.7 kHz for the calibrated $V_{CTRL} = 20 \text{ mV}$.

The effects of the parasitic capacitances are clearly depicted. These effects can be compensated by adjusting the reference voltage V_{CTRL} from 90 mV to 20 mV. As shown in Figure 48, this action slightly increases the power consumption, but it stays within the $5 \mu\text{W}$ limit.

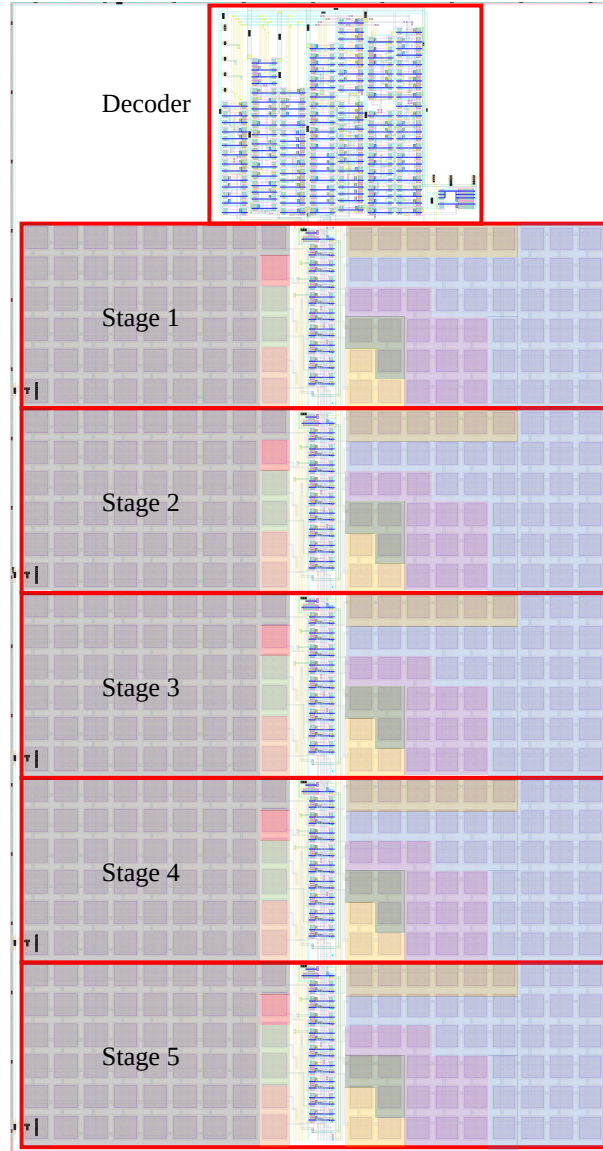
The propagation delay considering the parasitic capacitances is given by Eq. 4.4. The frequency can be modelled through Eq. 4.14 by considering the propagation delay from the inverters and the capacitance added by both the load capacitors and the parasitic capacitances.

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_p(V_{DD}, V_{CTRL})} \quad (4.14)$$

The power consumption is among the most important parameters to be measured in a DCO. Figure 48 shows the power consumption of the DCO in function of a digital code for the schematic and post-layout simulations.

The post-layout simulation shows a lower power consumption with the same adjustment as in the schematic simulation ($V_{CTRL} = 90 \text{ mV}$), but the decreased consumption is due to the decreased frequency, that drops to 3 MHz. The adjustment from 90 mV to 20 mV increases the power consumption and barely stays within the $5 \mu\text{W}$ limit. A 500-run Monte Carlo analysis of frequency in function of the digital code is shown in Figure 49.

Figure 45 – Layout of the DCO.



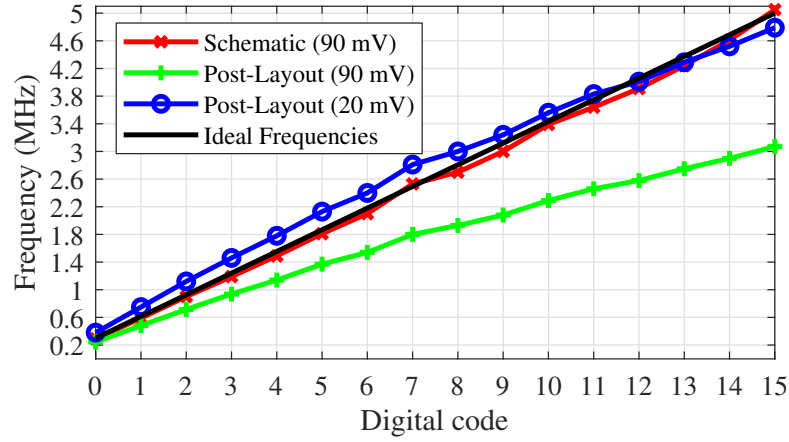
Source: Author

It considers the extracted parasitic components of the layout, and also process variation and mismatch effects. Also, in the same figure, the frequency is simulated for different operating temperatures of 0–70°C, and it is seen that the calibration can be used to correct the frequency in a cold or hot ambient.

A total of 18.8% of frequencies at code 15 were below 4 MHz, which points to a significant variation in frequency due to process and mismatch effects. To compensate for those effects, the frequency must be calibrated through the reference voltage V_{CTRL} .

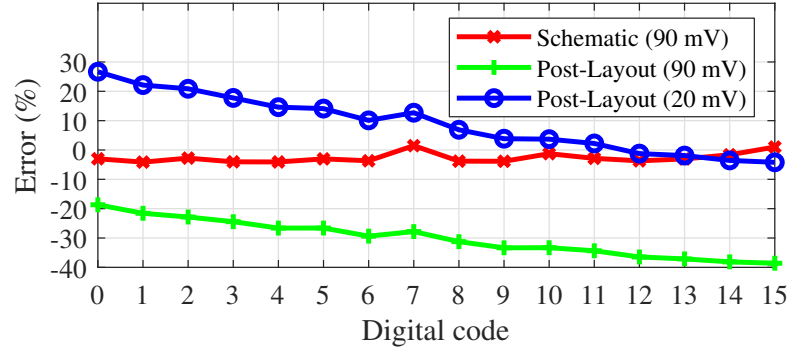
Supply voltage variation is an important factor to consider, as it has a significant impact on the propagation delay of the DCO. In Figure 50, a graph shows the value at the default 700 mV supply voltage and the variation in frequency at $\pm 10\%$ of V_{DD} . If the supply voltage drops 10% under its nominal voltage of 700 mV, the frequency can

Figure 46 – Comparison of frequency in function of digital code for schematic and post-layout simulations.



Source: Author

Figure 47 – Linearity error in frequency for schematic and post-layout simulations.



Source: Author

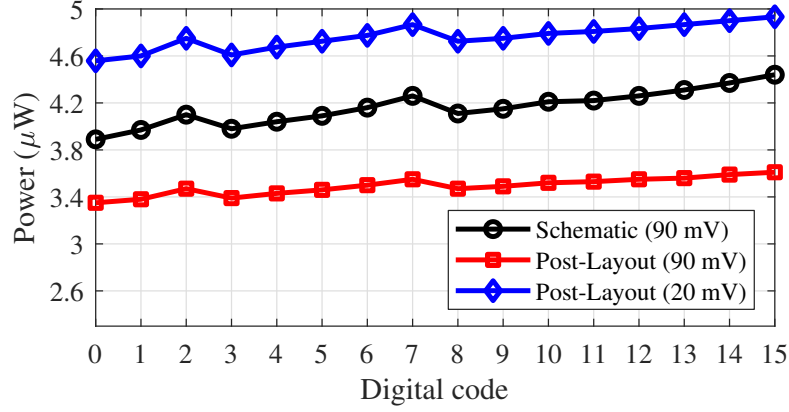
be compensated by decreasing V_{CTRL} from 80 mV to 0 mV. So, the designed DCO works inside the desired frequency range even for a variation of 10% in the nominal supply voltage.

Considering an offset frequency of 100 kHz, the phase noise for codes 1 and 15 are -117 dBc/Hz and -96 dBc/Hz, respectively. The Figure of Merit (FoM) from Eq. 4.15 considers the power and phase noise of the oscillator whilst the FoM from Eq. 4.16 considers the power per frequency. $\mathcal{L}$ is the phase noise at an offset frequency Δf , f_{osc} is the central frequency and P is the output power. The obtained FoM from Eq. 4.15 is 152.8 dBc/Hz for both codes 1 and 15. The power per frequency is 15.33 μ W/MHz and 0.98 μ W/MHz for codes 1 and 15.

Few designs of DCOs are found in the literature with such specific frequency range, therefore, a comparison with oscillators in similar frequencies is made in Table 7.

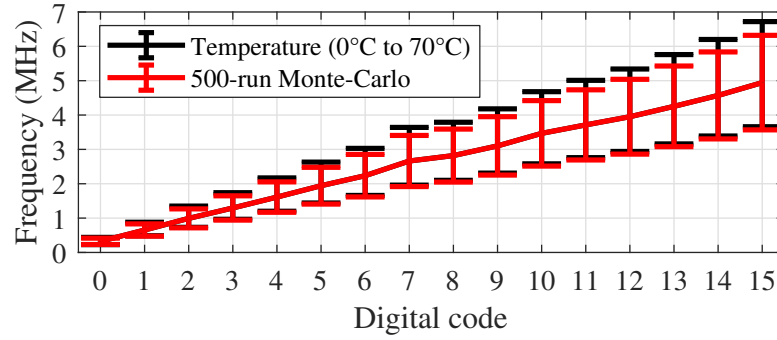
$$FoM_1 = |\mathcal{L}(\Delta f) + 20 \cdot \log_{10}\left(\frac{\Delta f}{f_{osc}}\right) + 10 \cdot \log_{10}\left(\frac{P}{1mW}\right)| \quad (4.15)$$

Figure 48 – Power consumption analysis of schematic and post-layout simulations.



Source: Author

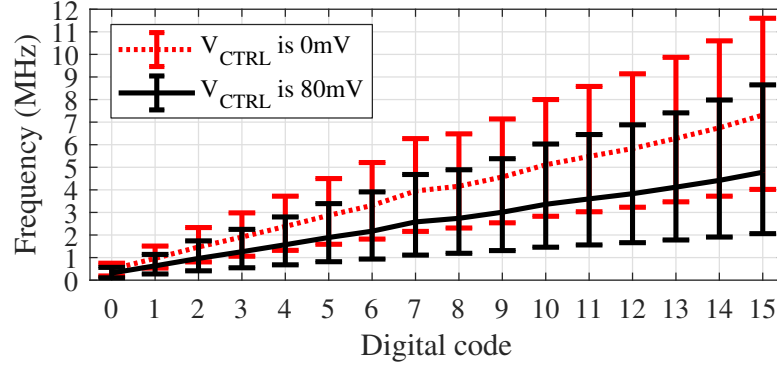
Figure 49 – Frequency variation in 0–70°C operating temperatures, and a 500-run Monte-Carlo analysis of standard deviation of the frequency in function of digital code.



Source: Author

$$FoM_2 = \frac{P}{f_{osc}} \quad (4.16)$$

Relaxation oscillators are used in Lu and Liao (2019), Koo et al. (2019), and Zhou, Goh and Gao (2020). An implementation for low-power wearables and sensors is seen in Lu and Liao (2019), and relies on self-threshold tracking and swing-boosting techniques to maintain a stable frequency with low noise, although, most of its power is consumed by the charge and discharge of the RC circuit. An implementation for implantable diagnostic devices is seen in Koo et al. (2019), and relies on voltage swing compensation for robust 1/f noise dampening. In Zhou, Goh and Gao (2020), an implementation for sensor interface applications is used, and implements switched-capacitor converters to boost the voltage swing. The DCO in Dabas and Kumar (2016) relies on the use of arrays of current-starving transistors controlled digitally to adjust the propagation delay of inverters for a ring oscillator. Other approach is seen in Jeon, Moon and Ahn (2009), where the propagation delay is modified through the combination of inverters in parallel. Also, each inverter has

Figure 50 – A variation of $\pm 10\%$ in supply voltage for V_{CTRL} voltages of 0 mV and 80 mV.

Source: Author

Table 7 – Performance comparison with state-of-the-art oscillators with similar oscillation frequencies.

	JSSC'19 ^a	TCAS-I'19 ^b	TCAS-II'20 ^c	This work
Technology (nm)	180	180	65	180
Measurement	Measured	Measured	Measured	Post-Layout
Frequency (MHz)	8.2	0.4449	3	0.3–5
Supply Voltage (V)	0.75	1.2	1	0.7
Power (μW)	46.3	21.3	17.3	4.6–4.9
Area (mm^2)	0.028	0.058	0.044	0.0348
Application	Low-power wearable and sensors	Implantable diagnostic devices	Sensor interfacing	Energy harvesting
Phase noise (dBc/Hz)	-109 @100kHz	-103.02 @10kHz	-114 @100kHz	-117@100kHz ^d -96@100kHz ^e
FoM ₁ (dBc/Hz)	168.8 @100kHz	152.7 @10kHz	161 @100kHz	152.8 @100kHz
FoM ₂ ($\mu\text{W}/\text{MHz}$)	5.6	47.8	5.7	15.33–0.98

^a Lu and Liao (2019);^b Koo et al. (2019);^c Zhou, Goh and Gao (2020);^d Code 1, considering $f_{osc} = 0.3$ MHz;^e Code 15, considering $f_{osc} = 5$ MHz.

Source: Author.

current-starving transistors and capacitors for fine-tuning.

4.1.3 CONCLUSION

This subsection presented a 0.3–5 MHz Digitally-Controlled Ring-Oscillator controlled by a four-bit digital word. The purpose of the DCO is to generate a variable frequency for a switched-capacitor DC-DC converter of an Energy Harvester. The layout occupies an area of 0.0348 mm^2 not considering pads. Monte-Carlo analysis in the highest

frequency (code 15), 18.2% of frequencies were below 4 MHz at the highest frequency (code 15), thus, a calibration can be made through an external signal V_{CTRL} to compensate for operating temperature, a $\pm 10\%$ supply voltage variation, and also for process variation and mismatch effects. The maximum output power is $4.9 \mu\text{W}$, considering V_{CTRL} of 20 mV on the post-layout simulation to achieve 5 MHz. The achieved FoM is 152.8 dBc/Hz at an offset frequency of 100 kHz, and the power per frequency is $15.33 \mu\text{W}/\text{MHz}$ and $0.98 \mu\text{W}/\text{MHz}$ for codes 1 and 15.

4.2 COLD-START SYSTEM

Harvesting a small amount of energy from the environment to supply electronic circuits is a promising alternative for dealing with the increasing number of Internet-of-Things (IoT) devices. This energy can be stored in batteries or be immediately consumed in battery-less devices. In the context of integrated circuits, the output power is typically in the range of nanowatts to milliwatts (KIZIROGLOU; YEATMAN, 2012), which requires the use of power-efficient and advanced design techniques for the development of ultra low-power circuits.

Most energy harvesting systems are composed of an energy transducer (e.g. photovoltaic cells, thermoelectric generators, or antennas), a voltage converter and a feedback control circuit. The voltage level generated by the transducer is not constant and depends on external factors. Because of that, a voltage converter (known as DC-DC converter) is employed to convert the non-constant DC voltage generated by the transducer to an adequate and constant operational level.

Most implementations of DC-DC converters use switched-capacitor (SC) or switched-inductor (SI) approaches. Both SC and SI converters require a switching frequency to oscillate between topological states (Van Breussegem; STEYAERT, 2013). Since the generation of the switching frequency is dependent on the DC-DC converter output voltage, a problem arises when the output level is so low that the clock generation circuit is not able to oscillate and drive the control circuits. In this condition, some type of auxiliary cold-starting system is necessary.

Several implementations of cold-start circuits have been proposed in the literature (BOSE; ANAND; JOHNSTON, 2018; CAO et al., 2019). In general, they are composed of a low-voltage oscillator, a clock boost and a multi-stage charge pump circuit. According to the number of stages used in the charge pump it is possible to multiply the input voltage to the desired voltage level, e.g. 0.75 V in (BOSE; ANAND; JOHNSTON, 2018). After the start-up time, the converter system reaches steady state operation and the converter output voltage can be used to supply the entire control system by removing the cold-start system from the operation.

However, in the implementation of DC-DC converters for ultra-low voltage (ULV) applications, the converter output voltage is in the range from 0.4 to 0.5 V (SILVA, 2020).

This voltage level could not be enough to supply the clock generation system since higher switching frequency (MHz range) and voltage swing are needed to drive the switches and to reduce the converter equivalent output resistance. Thus, the cold-start circuit needs to remain in operation even after the converter system reaches steady state operation, to supply the entire control system with the higher supply voltage.

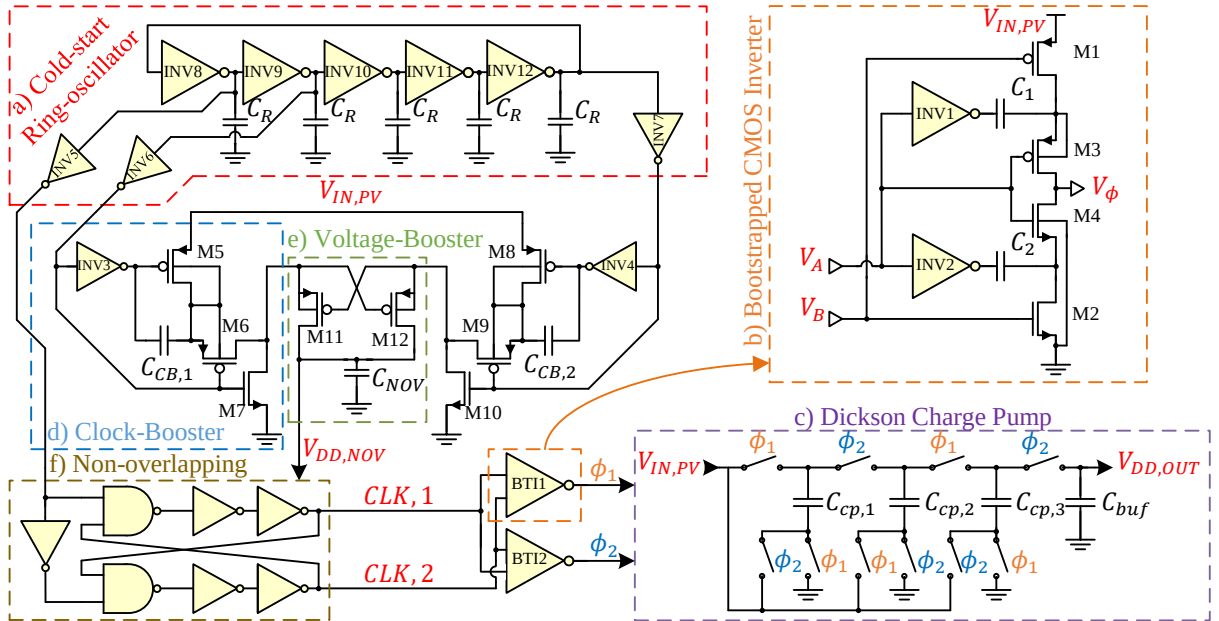
In this context, a cold-start system is required to be applied to an indoor-light energy-harvesting ULV device, as shown in Figure 37. A voltage level of around 650 mV must be provided by the cold-start circuit for the digitally-controlled oscillator (DCO) and main DC-DC converter, which is the minimum supply voltage required to drive the main DCO (DUTRA; GIRARDI; COMPASSI-SEVERO, 2022b) and switches for selecting the correct voltage conversion ratio (VCR) in a multi-topology SC converter. The circuit is implemented in a typical 180-nm CMOS technology node.

4.2.1 PROPOSED COLD-START SYSTEM

The proposed integrated cold-start system is developed in the context of a complete DC-DC SC converter aimed to harvest energy from indoor light with the use of small-size photovoltaic (PV) cells and to supply an ULV application.

The cold-start system has to provide a power of 10 μW , whereas 4.9 μW is for the DCO (operating at 5 MHz) and 2.0 μW for the multiplexers, as shown in Figure 37. The remaining power is used as safety margin considering switching and parasitic losses in the main converter operation.

Figure 51 – Complete schematic of the proposed cold-start circuit.



Source: Author.

Figure 51 shows the complete schematic-level implementation of the proposed cold-

start system. The main block is the Dickson charge pump (c), which quadruples the voltage provided by the PV cell ($V_{IN,PV}$) and generates the cold-start output voltage $V_{DD,OUT}$ that supplies the main converter. The generation of ϕ_1 and ϕ_2 signals are performed by a ring oscillator (a), followed by a clock-booster (d), a voltage-boost (e), a non-overlapping clock circuit (f) and two bootstrapped CMOS inverters (b).

A simple Dickson SC charge pump circuit boosts the voltage generated by the PV cell ($V_{IN,PV}$) to the minimum output voltage level ($V_{DD,OUT}$) required for starting the main DC-DC converter. Considering a minimum $V_{IN,PV} = 250 \text{ mV}$, it is necessary to use a voltage conversion ratio (VCR) of 2.8 to boost this voltage to $V_{DD,OUT} = 650 \text{ mV}$, which is the minimum required voltage level to turn on the DCO that generates the clock for the main converter in the target application. The Dickson charge pump is composed of 3 capacitors and 10 switches, controlled by signals ϕ_1 and ϕ_2 , as depicted in the block (c) of Figure 51. The output supply voltage $V_{DD,OUT}$ can be estimated through Eq. 4.17, where N is the voltage conversion ratio, I_L is the current load on the converter, f_{osc} is the oscillation frequency, and C_{fly} is the flying-capacitance (Van Breussegeem; STEYAERT, 2013).

$$V_{OUT} = V_{IN,PV} \cdot N \cdot \left(V_{IN,PV} - \frac{I_L}{f_{osc} \cdot C_{cp}} \right) \quad (4.17)$$

The switches are implemented with transmission gates using low- V_T transistors. Figure 52 shows the electrical simulation of the steady-state output voltage for single, dual and triple-stage Dickson topologies as a function of the switches NMOS transistor channel width (W_N) for an input voltage of 250 mV operating at 10 MHz. Channel width of PMOS switches (W_P) was fixed in $1.25 \cdot W_N$ and all channel lengths were set to the minimum (250 nm and 300 nm for PMOS and NMOS, respectively). It can be seen in Figure 52 that only the triple-stage Dickson is able to reach a $V_{DD,OUT}$ of 650 mV. A higher number of stages could increase the output voltage by a considerable margin, but the impedance of the Dickson converter increases exponentially with the number of stages (Van Breussegeem; STEYAERT, 2013). Considering the results of Figure 52, we choose a CMOS transmission gate switch with $W_N = 20 \text{ } \mu\text{m}$ and $W_P = 25 \text{ } \mu\text{m}$ as ideal to reach the highest charge pump steady-state output voltage.

Signals ϕ_1 and ϕ_2 , which control the switches in the Dickson charge pump, must be generated from the voltage $V_{IN,PV}$. A ring-oscillator, shown in Figure 51 (box (a)), can be used as a cold-start solution as it self-starts from small supply voltages (BOSE; ANAND; JOHNSTON, 2018). It can be used to provide the necessary oscillation frequency for the charge pump.

Low- V_T transistors are also used to implement the inverters INV8 to INV12 that compose the ring oscillator in order to deal with low supply voltages. They are sized with a W/L ratio of $30 \text{ } \mu\text{m} / 0.3 \text{ } \mu\text{m}$ and $20 \text{ } \mu\text{m} / 0.25 \text{ } \mu\text{m}$, for NMOS and PMOS, respectively. The NMOS transistor width is larger to compensate for a large fall time due to the gate

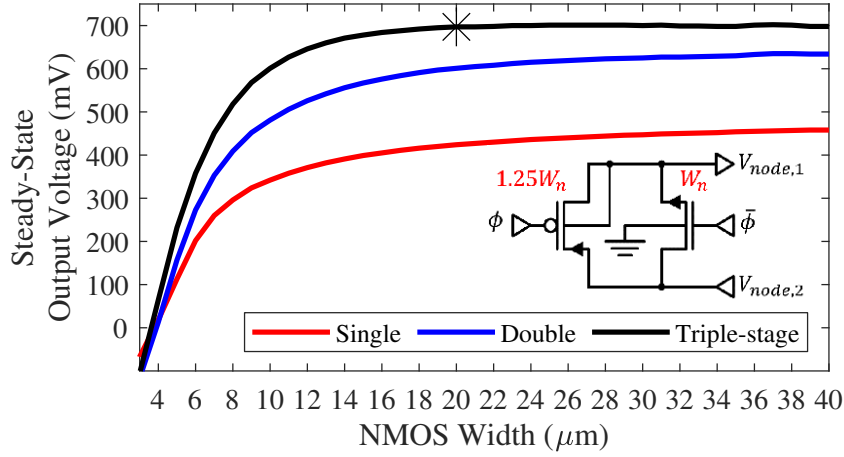


Figure 52 – Comparison of steady-state output voltage of single, double and triple-stage Dickson converters in function of switch channel width.

Source: Author.

voltage being lower than the threshold voltage of the low- V_T transistor.

Oscillation frequency f_{osc} is calculated through Eq. 4.18, where N is the number of stages, C_{RO} is the load capacitance, and $R_{eq,N}$ and $R_{eq,P}$ are equivalent series resistance of transistors that compose the inverters.

$$f_{osc} = \frac{1}{0.69 \cdot N \cdot C_{RO} \cdot (R_{eq,N} + R_{eq,P})} \quad (4.18)$$

A 100 fF MiM capacitor is used as buffer capacitor (C_R in Figure 51) to limit the oscillation frequency to 10 MHz.

Inverters INV6 and INV7 are used for signals phased 180° from each other, as shown in Figure 51 (box (a)). The inverters are connected to different nodes of the ring-oscillator, and both have the same W/L dimensions of 14/0.3 and 17.5/0.25 for NMOS and PMOS, respectively.

The three-stage Dickson rectifier provides a high output voltage, although its impedance is higher and can not sustain high loads. The output voltage is required to be around 650 mV, therefore, to decrease the impedance in CMOS switches and reduce the voltage drop without increasing transistors sizes, the voltage swing of the clock signal needs to be increased. The bootstrapped inverter (BTI), shown in Figure 51, box (b), can be used to obtain a higher voltage swing. It was originally intended to be used on a differential ring-oscillator (YI et al., 2018), therefore, signals with a slightly higher amplitude are required. To fix this problem, two clock-boost circuits (box (d) in Figure 51) are implemented to pump charge into C_{NOV} through a pair of cross-coupled transistors (box (e) in Figure 51) to obtain a higher voltage in $V_{DD,NOV}$. This voltage is used to power the non-overlapping clock circuit (block (f) in Figure 51). PMOS transistors M11 and M12 from the Voltage-Booster have a W/L ratio of 10 μm / 0.25 μm .

In the Clock-Booster circuit, the transistors in inverters INV3 and INV4 have a W/L ratio of $5 \mu\text{m} / 0.35 \mu\text{m}$ and $20 \mu\text{m} / 0.25 \mu\text{m}$ for NMOS and PMOS transistors, respectively. Both M5, M6, M8 and M9 have a size of $20 \mu\text{m} / 0.25 \mu\text{m}$, and M7 and M10 have a size of $5 \mu\text{m} / 0.25 \mu\text{m}$.

The non-overlapping clock generator, shown in Figure 51, box (f), is a circuit composed of logic gates to insert a delay between the signals to avoid short circuits in circumstances where both phases are conducting. Ideally, this circuit should be used before the charge pump, but the signals are swing-boosted. Thus, the non-overlapping circuit is used before the BT inverters. This circuit has two delay stages and all NMOS and PMOS transistors in the logic gates are sized as $0.5 \mu\text{m} / 0.3 \mu\text{m}$ and $1 \mu\text{m} / 0.25 \mu\text{m}$, respectively. There is a time instant in which both non-overlapped signals are low. Since the topology of the BT inverter outputs a high signal when both input signals are low, it generates a boosted overlapped signal. In order to fix this problem, an overlapped signal can be provided to the BT inverter by adding an inverter to the outputs of the non-overlapping circuit, thus generating non-overlapped signals at the output.

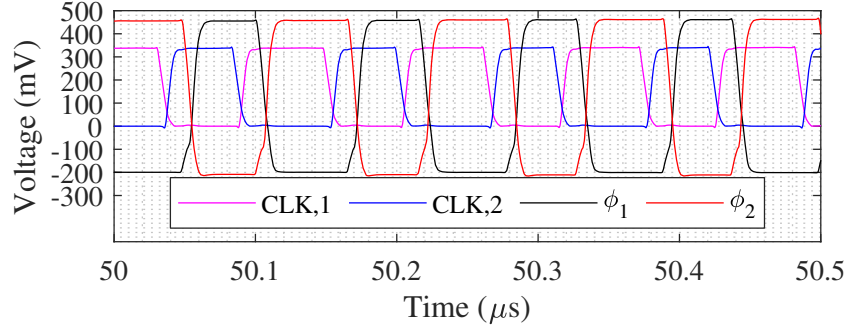
Typical clock boosting techniques can increase the amplitude of the signal. The work in Yi et al. (2018) proposes a triple amplification, providing a voltage swing from $-V_{IN}$ to $2V_{IN}$. The adapted topology is illustrated in Figure 51, box (b). Inverters INV1 and INV2 are used to charge the capacitors C_1 and C_2 to $V_{IN,PV}$. When signal V_A is high and V_B is low, INV1 and INV2 output a low signal, but only M1 is conducting and V_{C1} charges to $V_{IN,PV}$. Thus, M3 has a source terminal in $V_{IN,PV} + V_{C1}$ and the output signal is $2 \cdot V_{IN,PV}$. When the signals invert and V_A is low and V_B is high, INV1 and INV2 provide a high logic-level signal, M2 is conducting and V_{C2} charges to $V_{IN,PV}$. Thus, the source terminal of M4 is $0 - V_{C2}$ and the output signal is $-V_{IN,PV}$.

4.2.2 SIMULATION RESULTS

The proposed cold-start circuit was simulated at schematic-level with Spectre circuit simulator with typical and corner parameters and different temperatures. The simulation of phase signals ϕ_1 and ϕ_2 is presented in Figure 53 at steady-state. Considering an input voltage $V_{IN,PV}$ of 250 mV, the non-overlapped signals $V_{CLK,1}$ and $V_{CLK,2}$ are boosted to an amplitude of 330 mV by the Voltage-Booster circuit, and those signals are used as input for the bootstrapped inverters. The outputs of the bootstrapped inverters provide signals ϕ_1 and ϕ_2 with an amplitude ranging from -200 mV to 450 mV.

Figure 54 presents the transient schematic-level simulation of the supply voltage provided to the non-overlapping circuit ($V_{DD,NOV}$) considering an input voltage of 250 mV. The circuit requires only $30.76 \mu\text{s}$ for $V_{DD,OUT}$ to reach 700 mV without load. In the *Start-up Phase 1*, the charge pump charges to its maximum voltage without any load attached to its output signal. In this phase, the charge-pump reaches a voltage of 700 mV. In the *Start-up Phase 2*, a load of $10 \mu\text{W}$ is switched-on for supplying power to all sub-circuits,

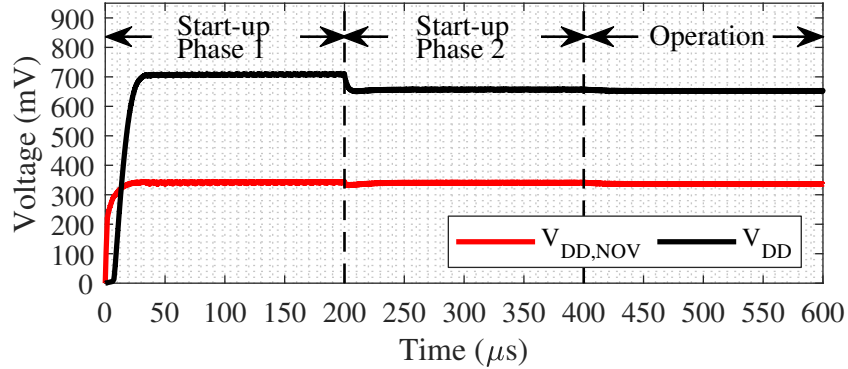
Figure 53 – Signals $V_{\phi,1}$ and $V_{\phi,2}$ from the bootstrapped inverter with $V_{CLK,1}$ and $V_{CLK,2}$ as input from the non-overlapping clock circuit.



Source: Author.

such as the DCO, the main switched-capacitor converter multiplexers, and logic control circuits, but the load of the main converter is not switched-on. The supply voltage drops to 650 mV in this phase. In the *Operation* phase, a load of 50 μA is switched on at the output of the main converter, and no significant voltage drop in $V_{DD,OUT}$ is noticed.

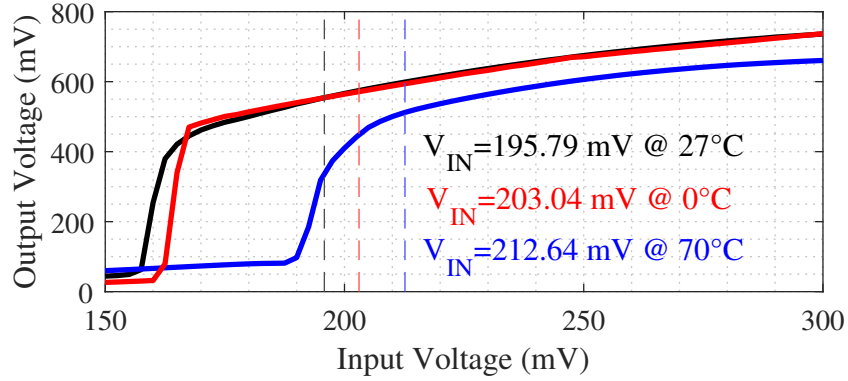
Figure 54 – Transient simulation of supply voltage for the non-overlapping circuit $V_{DD,NOV}$ and supply voltage V_{DD} in start-up phases and operation.



Source: Author.

Figure 55 presents the variation of the output voltage $V_{DD,OUT}$ in function of the input voltage $V_{IN,PV}$ for temperatures of 0°C, 27°C and 70°C, considering a schematic simulation. The minimum $V_{IN,PV}$ in which the main DC-DC converter achieves the target output voltage of 400 mV is 195.79 mV. It represents a $V_{DD,OUT}$ of 625.7 mV generated by the cold-start circuit. The variation in temperature affects the on-state resistance of the CMOS switches in the Dickson charge-pump. Considering an energy harvesting system supplied by a 20 mm x 40 mm crystalline silicon PV cell, it is possible to notice that the proposed cold-start system is able to operate with a minimum illuminance around 800 lux (MONTEIRO et al., 2022a), which is a typical illuminance level provided for an indoor office room.

Figure 55 – Steady-state Output Voltage ($V_{DD,OUT}$) for temperatures of 0°C, 27°C and 70°C.



Source: Author.

Table 8 shows a comparison of the proposed cold-start circuit with related works. Our circuit requires a higher minimum input voltage (195.79 mV) among the compared works. On the other hand, it provides the lowest start-up time and the highest output power level while it requires no external components since we used an 100-pF integrated output filtering capacitor.

Table 8 – Performance comparison with other micro-power start-up systems for ULV applications.

Specification	(YIN et al., 2018) ¹	(MACHADO et al., 2014) ²	(BOSE et al., 2018)	This work
Technology	28 nm	130 nm	180 nm	180 nm
Topology	RO-CP	LRO-CP	RO-CP	RO-CP
$V_{in_{min}}$	200 mV	108 mV	57 mV	195.79 mV
V_{out}	900 mV	1 V	720 mV	625.7 mV
P_{out}	2 μ W	5 μ W	3.5 nW	10 μW
Start-up time	400 μ s	-	135 ms	30.7 μs

RO: Ring Oscillator, LRO: Inductive Ring Oscillator, CP: Charge Pump

(*) Considering only the main micro-power manager.

(**) Considering the maximum output power.

Source: Author.

4.2.3 CONCLUSION

This subsection presented a cold-start circuit applied to an indoor-light energy harvesting DC-DC converter which provides a 625.7 mV output voltage from a minimum input voltage of 195.79 mV generated by a photovoltaic cell. The proposed circuit is designed in a 180-nm CMOS process and provides a start-up time of 30.7 μ s. The total

start-up power is $10\ \mu\text{W}$. The implementation is fully-integrated, and the circuit was successfully tested in a DC-DC converter able to provide an output voltage of 400 mV. The results are similar to other works in the state-of-the-art.

4.3 A DUAL-MODE SC DC-DC CONVERTER WITH FEEDBACK CONTROL

This section proposes a multi-topology switched-capacitor DC-DC Converter with doubler and tripler modes. The objective of this converter is to obtain a 400 mV minimum output voltage with $20\ \mu\text{W}$ output power for a 250 mV input voltage. It features a feedback control that checks the output voltage through two comparators that send signals to a up-down counter that changes the switching frequency of the DCO in order to obtain an output voltage closer to the desired 400 mV output voltage.

4.3.1 SPECIFICATION AND DESIGN STRATEGIES

In order to provide power to an hypothetical ultra-low power (ULP) and ultra-low voltage (ULV) batteryless IoT device, a minimum voltage of 400 mV and a load of $30\ \mu\text{W}$ are considered, as those are typical values for ULP energy harvesters. Thus, the objective of this DC-DC voltage converter is to maintain a continuous load for an undetermined time while outputting a minimum voltage of 400 mV. That load could very well be the internal resistance of a battery, or, in a batteryless system, as an external capacitor.

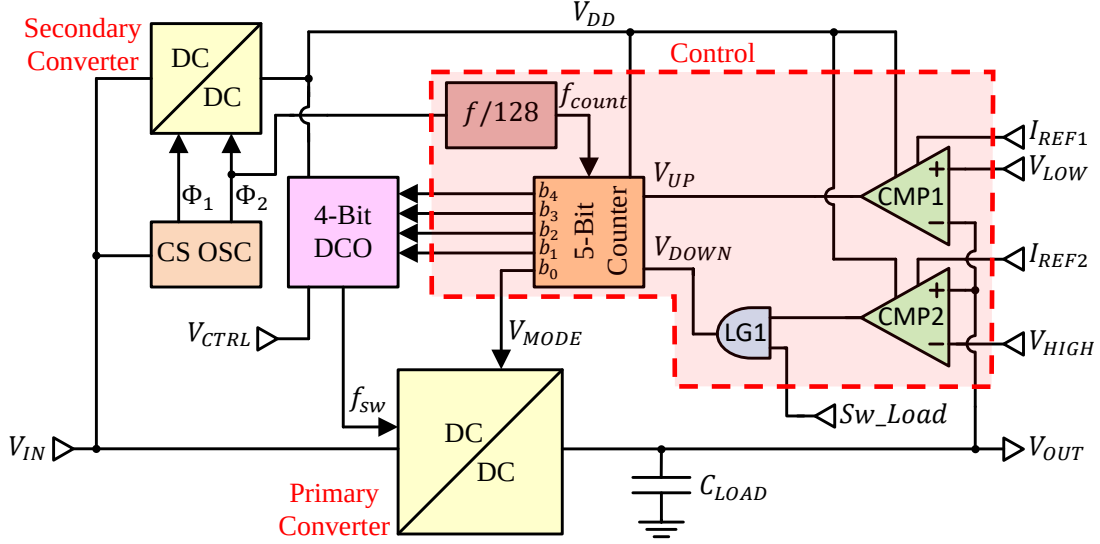
DC-DC converters are widely used to produce regulated voltages from unregulated or non-constant voltage sources, such as photovoltaic cells. Aside from only working in step-down mode, linear converters are very inefficient due to excessive power-loss to heat. In contrast, switched-mode DC-DC converters are versatile and efficient, and are divided into two categories: capacitor-based and inductor-based (Van Breussege; STEYAERT, 2013). Switched-capacitor converters are favorable for integrated implementation due to the capacitor inherent higher energy-density in comparison to inductors (KESARWANI; SANGWAN; STAUTH, 2015).

Generally, the load for those systems consists of a large capacitor, although it makes it easier to estimate the resistance, it is hard to estimate the efficiency of the system in those circumstances due to the capacitor having a low impedance when discharged and a high impedance when charged. Batteryless systems are not constant as it switches between a power-hungry active-mode for a small period of time, and a sleep-mode to charge the capacitor back for a longer period of time. This idea is not evidenced in other works, but the idea is that a certain fixed value can be used for that matter, but the system can supply a larger amount of power in the “active mode” when the capacitor is charged, but a smaller power in the “sleep-mode” as it requires of a longer period of time to charge the capacitor.

The complete schematic diagram is illustrated in Figure 56, it consists of a primary

and secondary converter, a cold-start oscillator, a 4-bit Digitally-Controlled Oscillator, and a control system that consists of a 5-bit synchronous up/down counter and two comparators..

Figure 56 – Complete schematic diagram of the Energy Harvester.



Source: Author.

The output of the secondary converter is the supply voltage V_{DD} for all sub-circuitry in the energy harvesting system, it should generate a voltage above 600 mV to be able to drive the switches in the primary SC converter.

4.3.2 DESIGN OF A SWITCHED-CAPACITOR DC-DC CONVERTER

Switched-capacitor converters of any topology are composed of switches, flying-capacitors (also known as charge-transfer capacitors), and a buffer capacitor (Van Breussegeem; STEYAERT, 2013). This type of converter operates in topological states, for example, charges the flying-capacitors on the first state, and discharges on the second state.

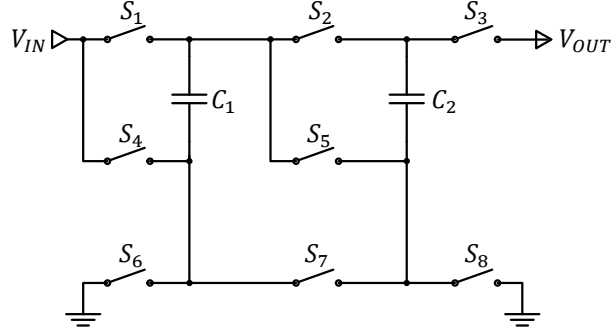
As previously stated, the main SC Converter is required to have an output voltage of 400 mV and output power of 30 μ W, which are very typical values for ULV and ULP energy harvesters.

A multi-topology converter can be used to obtain several voltage conversion ratios (VCRs) (SILVA; SEVERO; GIRARDI, 2020). A single-stage and two-stage Dickson, or a series-parallel doubler and tripler could be used to obtain VCRs of 2 and 3, respectively. Although, the output equivalent resistance of the Dickson converter increases exponentially with the number of stages (Van Breussegeem; STEYAERT, 2013).

A dual-mode SC converter is illustrated in Figure 57, with eight CMOS switches and two flying-capacitors.

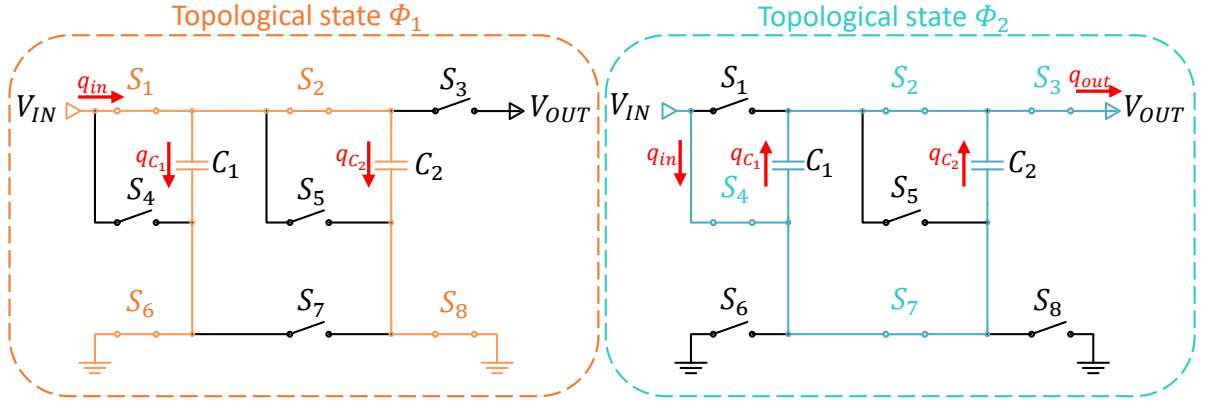
In the topological state ϕ_1 for Doubler mode, switches S_1 , S_2 , S_6 and S_8 are closed. Therefore, flying-capacitors C_1 and C_2 are put in parallel configuration with the voltage

Figure 57 – Schematic diagram of a doubler/tripler SC converter.



Source: Author.

source V_{IN} . In the topological state ϕ_2 for Doubler mode, switches S_2 , S_3 , S_4 and S_7 are closed. Therefore, flying-capacitors C_1 and C_2 are put in parallel configuration between themselves, and then put in series with the voltage source V_{IN} , and outputs the sum of voltages between the voltage input V_{IN} and the capacitors voltage V_C . The charge flow is illustrated in Figure 58.

Figure 58 – Charge flow of topological states ϕ_1 and ϕ_2 for the SC Converter in Doubler mode.

Source: Author.

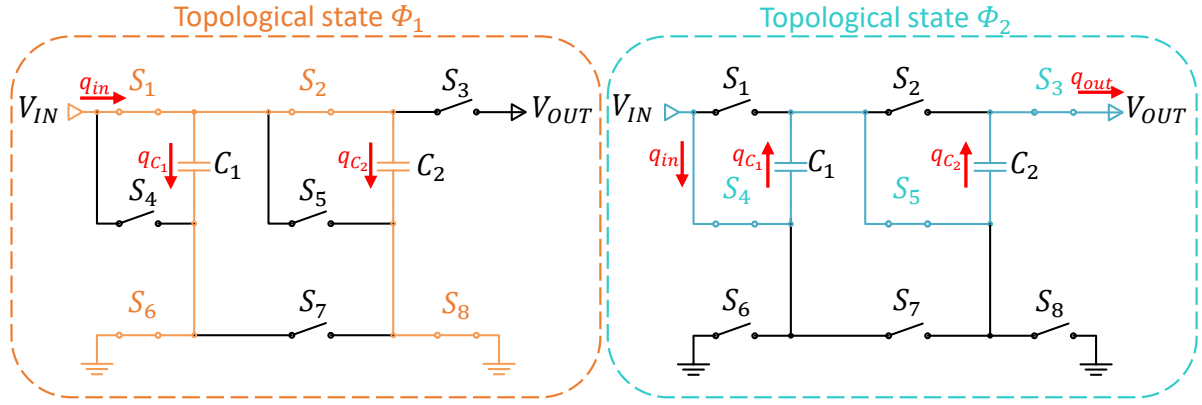
The charge multipliers for the Doubler mode can be extracted by applying the Charge Flow Analysis on the SC converter, then applied into the SSL and FSL equations to obtain the Output Equivalent Resistance, as shown in Eq. 4.19.

$$R_{out,2x} = \sqrt{\left(\frac{0.5}{f_{sw} \cdot C_1}\right)^2 + (4R_s + 8.5R_{on})^2} \quad (4.19)$$

Considering the topology for the Doubler mode, and through the use of the Charge Flow Analysis, the Equivalent Output Resistance of the SC Converter can be obtained through the SSL and FSL resistances.

In the topological state ϕ_1 for Tripler mode, switches S_1 , S_2 , S_6 and S_8 are closed. Therefore, flying-capacitors C_1 and C_2 are put in parallel configuration with the voltage source V_{IN} . In the topological state ϕ_2 for Tripler mode, switches S_3 , S_4 and S_5 are closed, and flying-capacitor C_1 is put in series with the voltage source V_{IN} . Thus, the output voltage is the sum of voltages between the voltage input V_{IN} and the capacitors voltage V_C . The charge flow is illustrated in Figure 59.

Figure 59 – Charge flow of topological states ϕ_1 and ϕ_2 for the SC Converter in Tripler mode.



Source: Author.

Similarly, the charge multipliers for the Tripler mode can be extracted through the Charge Flow Analysis and applied into Eq. 2.12 and Eq. 2.15 to obtain the Output Equivalent Resistance, as given by Eq. 4.20.

$$R_{out,3x} = \sqrt{\left(\frac{2}{f_{sw} \cdot C_1}\right)^2 + (8R_s + 14R_{on})^2} \quad (4.20)$$

Figure 60 shows the resistance of a CMOS switch using medium-VT transistors with W/L ratio of 5/0.25 and 17.5/0.3 for NMOS and PMOS transistors, respectively, also using 10 fingers each.

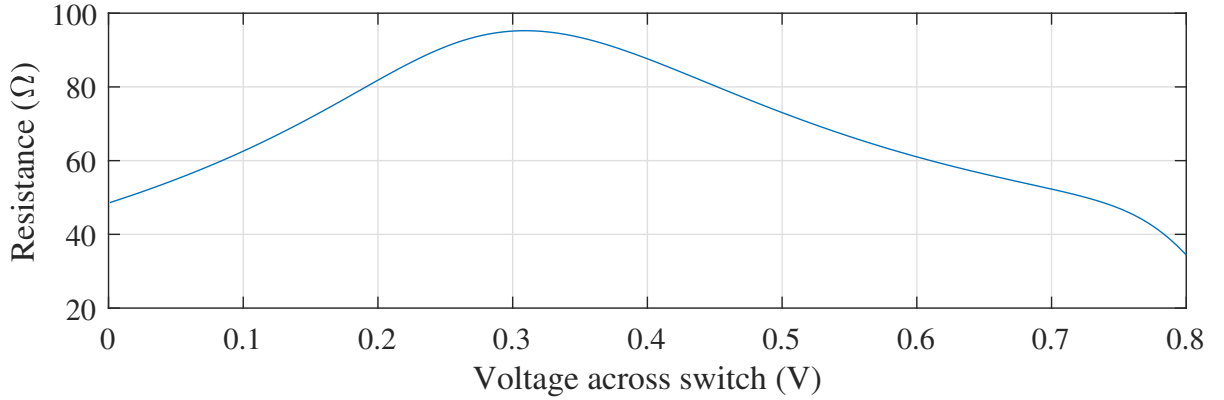
Figure 61 shows the histogram of the on-state resistance of the CMOS switch considering a 5000-run Monte-Carlo analysis with mismatch and process effects. The obtained mean resistance is 76.8 Ω , with a standard deviation of 8.2 Ω .

4.3.2.1 CALIBRATION OF SWITCHING FREQUENCY

As explained by Silva (2020), the optimal frequency is obtained when the SSL and FSL resistances tend to be equal. The optimal frequency $f_{optimal}$ for a SC Converter with the defined specifications is given by Eq. 4.21.

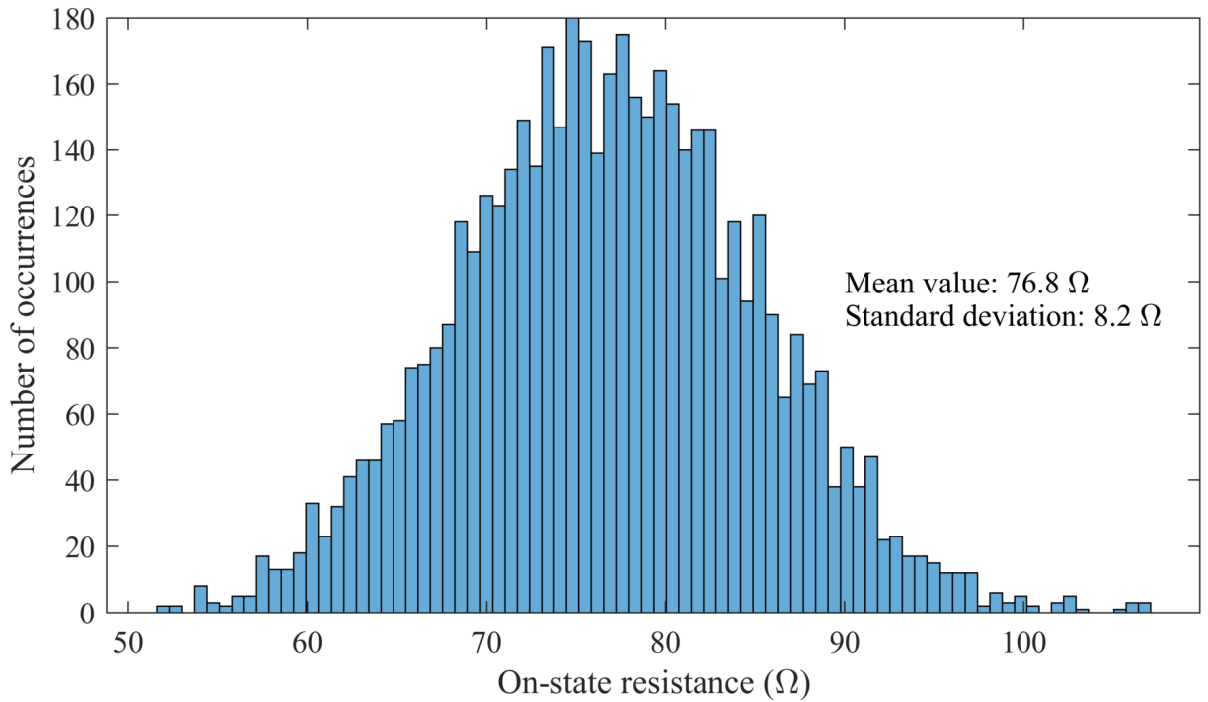
$$f_{optimal} = \frac{K}{R_{FSL} \cdot C_{fly}} \quad (4.21)$$

Figure 60 – On-state resistance of the CMOS switch for the SC Converter.



Source: Author.

Figure 61 – 5000-run Monte-Carlo analysis of the on-state resistance of the CMOS switch considering mismatch and process effects



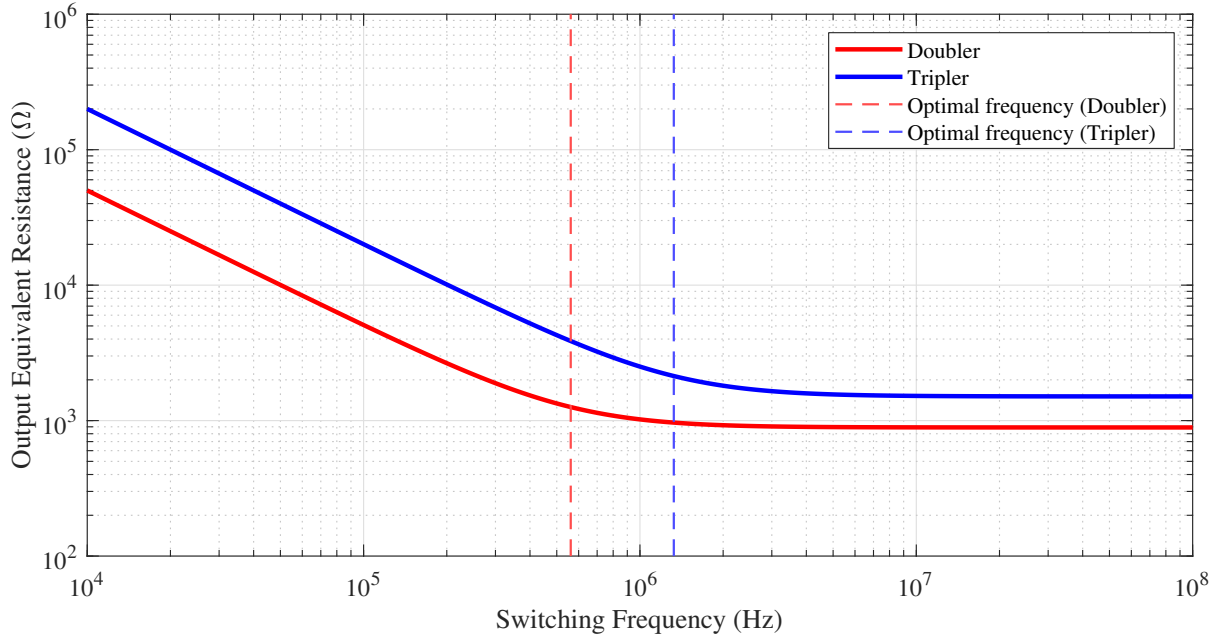
Source: Author.

Where K is a topological constant, R_{FSL} is the Fast Switching Limit resistance, and C_{fly} is the flying-capacitance.

Considering flying-capacitors of 1 nF and CMOS switches with an average resistance of 80 Ω and applying this value into Eq. 4.19 and Eq. 4.20, the optimal frequency can be calculated, and is 561 kHz and 1.3 MHz for the Doubler and Tripler topologies, respectively. The Output Equivalent Resistance in function of switching frequency for both modes of the converter is shown in Figure 62.

Due to the increase in the flying-capacitors, the optimal switching frequency

Figure 62 – Output Equivalent Resistance and optimal frequency for Doubler and Tripler modes.



Source: Author.

decreased. Thus, the DCO from Section 4.3.2 requires a calibration through the V_{CTRL} voltage. Thus, a resistive divider is used for around 15% of V_{DD} , that matches with a 1.3 MHz maximum switching frequency. The DCO is supplied with a V_{DD} of around 650 mV, and has a calibration voltage adjustment with 15% of V_{DD} to obtain a 1.3 MHz maximum frequency, as explained in the previous. The V_{CTRL} voltage ranges from 120 mV to 160 mV, thus, the DCO now has a power consumption under 2 μ W. Figure 63 shows the oscillation frequency and power consumption of the DCO in function of the calibration voltage V_{CTRL} .

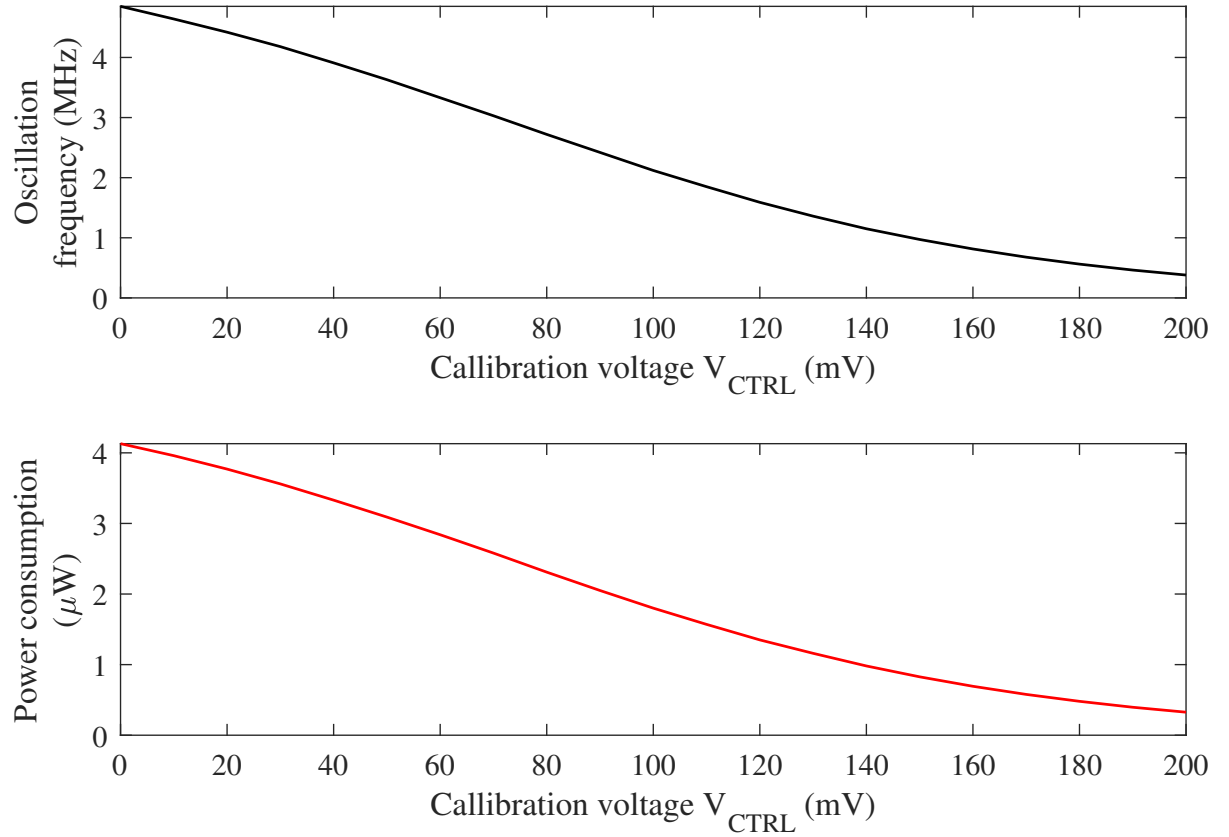
A current-based calibration would be a better option due to less complexity in current sources. In order to generate the V_{CTRL} voltage, a DAC (digital-to-analog converter) could be used.

4.3.2.2 MULTIPLEXERS

A total of three dual-input multiplexers (Mux) are implemented in order to select the mode on the dual-mode SC converter, as illustrated in Figure 64. A single-bit signal V_{MODE} is required for the selection, where a low logic-level represents the Doubler mode and a high logic-level represents the Tripler mode.

Table 9 shows the combinations of topological states used to select between the doubler and tripler topologies. The multiplexers are used to change the signal for switches S_2 , S_5 and S_7 in order to select either the Doubler or Tripler mode.

The sizing of the CMOS switches, multiplexers, flying-capacitor and buffer capac-

Figure 63 – Frequency and power consumption in function of V_{CTRL} .

Source: Author.

Table 9 – Combination of topological states for the SC Converter.

Switch	Doubler	Tripler
S_1	ϕ_1	ϕ_1
S_2	ON	ϕ_1
S_3	ϕ_2	ϕ_2
S_4	ϕ_2	ϕ_2
S_5	OFF	ϕ_2
S_6	ϕ_1	ϕ_1
S_7	ϕ_2	OFF
S_8	ϕ_1	ϕ_1

Source: Author.

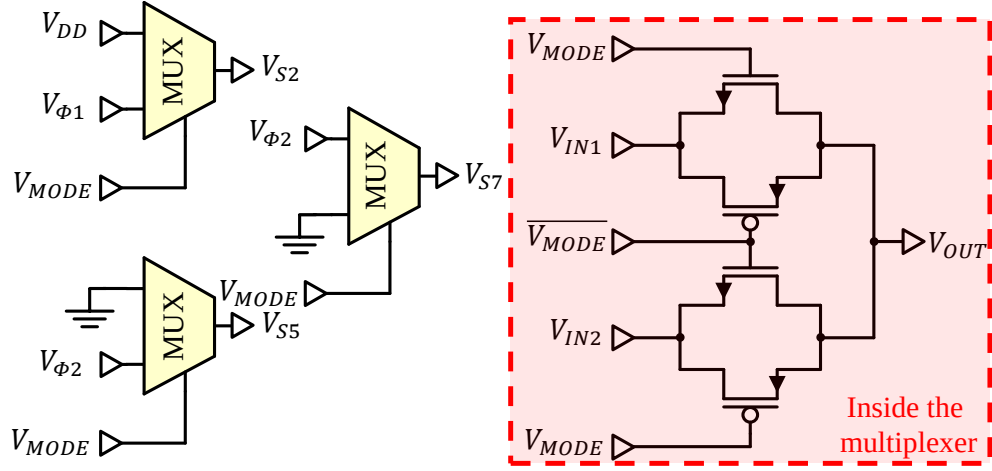
itor are shown in Table 10.

4.3.3 CONTROL

4.3.3.1 COMPARATORS

To maintain control of the output voltage of the SC Converter, two comparators are needed to check if the voltage level is between two defined thresholds (380mV and

Figure 64 – Doubler/Tripler mode selector with three 2-to-1 multiplexers.



Source: Author.

Table 10 – Sizing of components in the multi-topology SC Converter.

Specification	Sizing	Type	Fingers
S_1 to S_8 (W_N/L_N)	$5 \mu\text{m}/0.3 \mu\text{m}$	Medium-VT	10
S_1 to S_8 (W_P/L_P)	$17.5 \mu\text{m}/0.25 \mu\text{m}$	Medium-VT	10
Mux (W_N/L_N)	$1 \mu\text{m}/0.18 \mu\text{m}$	Nominal-VT	1
Mux (W_P/L_P)	$2 \mu\text{m}/0.18 \mu\text{m}$	Nominal-VT	1
C_{fly}	1 nF	External	-
C_{buffer}	50 nF	External	-

Source: Author.

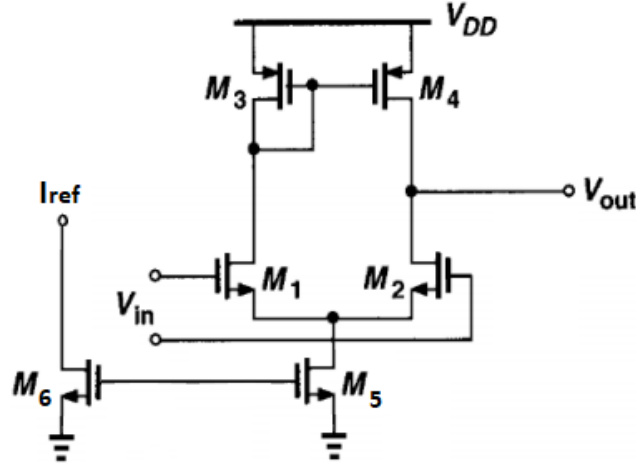
420mV), thus, two comparators are needed for this system. A comparator must output a high logic-level in signal UP when V_{OUT} is below 380mV. The other comparator must output a high logic-level in $DOWN$ when V_{OUT} is above 420mV.

Oliveira et al. (2017) presents a 180-nm CMOS voltage reference with a V_{REF} of 225.3 mV, with a power consumption of 57.8 pW, and can start from supply voltages of 450 mV. This voltage reference can be implemented for use in the voltage thresholds of 380 mV and 420 mV, although the output voltage V_{OUT} is required have a voltage divider due to the lower V_{REF} .

A low-power dynamic comparator, such as a StrongARM latch comparator (RAZAVI, 2015) or a Double-Tail comparator (BABAYAN-MASHHADI; LOTFI, 2014) could be used in this case, but for simplicity purposes, a single-ended differential amplifier (RAZAVI, 2016) is used as a comparator. This comparator is simple and has low power consumption, not significant enough to consider other topology. The topology is illustrated in Figure 65.

The I_{ref} reference current of 90 nA is generated externally. Although, for an internally-generated current reference, a topology of current-source could be implemented,

Figure 65 – Single-ended differential amplifier.



Source: Adapted from (RAZAVI, 2016).

for example, Osaki et al. (2010) designs a 93 nA current-reference with temperature compensation. The power consumption of such a circuit is 811 nW.

The differential amplifiers are sized by considering reference currents of 90 nA, and voltage levels of 380 mV and 420 mV. Table 11 shows the sizing of the transistors for the differential amplifier.

Table 11 – Sizing of transistors for the differential amplifier.

Transistor	Type	Length (μm)	Width (μm)	Multipliers
M1	NMOS	3	19.995	1
M2	NMOS	3	19.995	1
M3	PMOS	5	4.8	1
M4	PMOS	5	4.8	1
M5	NMOS	3	16.1	2
M6	NMOS	3	16.1	2

Source: Author.

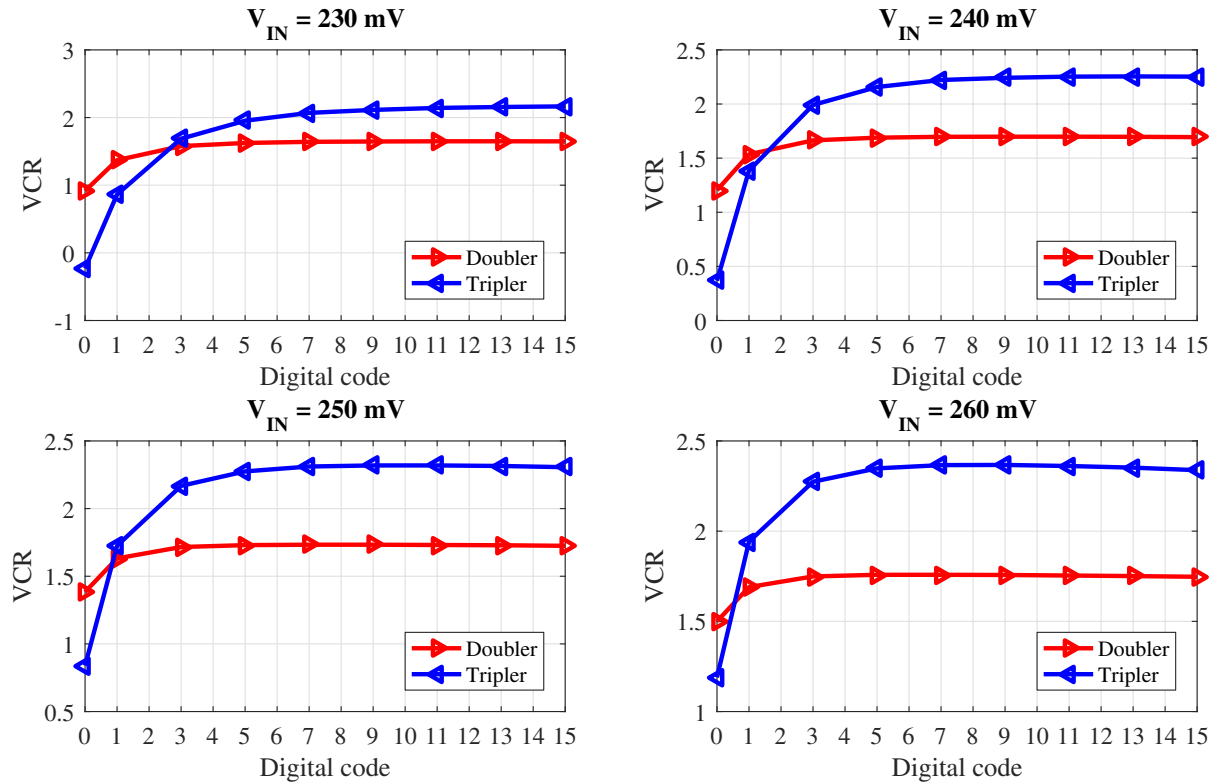
4.3.3.2 HYSTERETIC LOGIC SYSTEM AND BIDIRECTIONAL COUNTER

In Figure 56, in order to start operation faster on a high frequency, the V_{DOWN} signal is disabled through an AND logic gate (LG1), and is only enabled when a time represented by signal Sw_Load passes after the load is added to the output of the SC Converter. This time is sufficient for the load at the output to stabilize under a high frequency.

The Slow Switching Limit is dependant on flying-capacitance and switching frequency (Van Breussegeem; STEYAERT, 2013). This dependence can be effectively used to modify the VCR of the converter through switching frequency. The output of both

modes creates an hysteretic effect that can be used in a closed-loop system, thus, a digital counter could be implemented to either increase or decrease the digital codes in a DCO to obtain a certain output voltage. As illustrated in Figure 66, the VCR of the SC converter with input voltages of 230 mV to 260 mV is dependant on the switching frequency for the SSL region in both doubler and tripler topologies. After reaching the optimal frequency where SSL and FSL resistances are equal, the FSL region starts and the VCR does not increase regardless of frequency.

Figure 66 – Steady-state Voltage Conversion Ratio (VCR) in function of a digital code for DCO frequency.



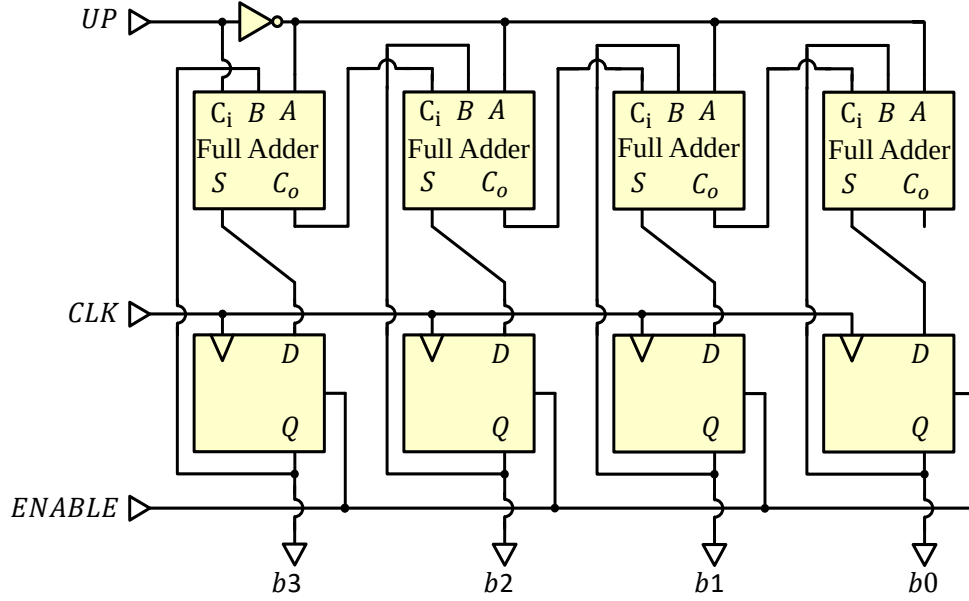
Source: Author.

The counter topology is a simple 4-bit synchronous up/down binary counter, as illustrated in Figure 67. It consists of four stages of a full-adder and an one-bit register (D-type Flop Flop). The carry-out of a stage is one of the inputs of the next carry out, thus, the counter is able to count up or down (WESTE; HARRIS, 2011).

The logic system that controls the the counter and SC converter modes is illustrated in Figure 68.

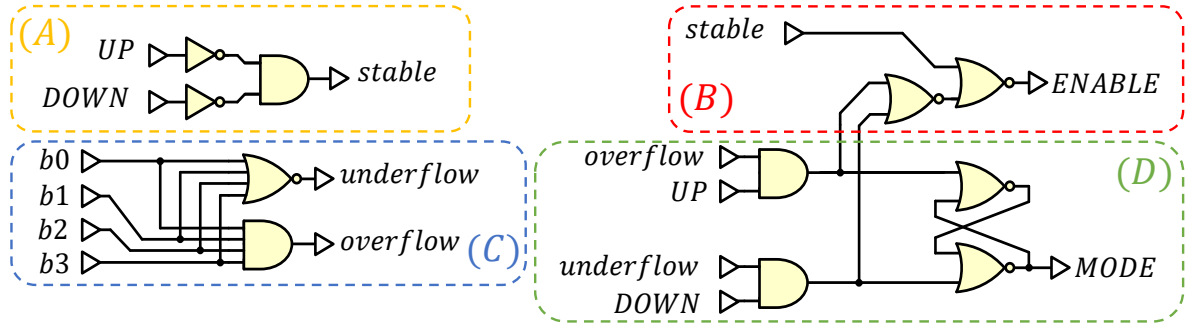
Due to the use of a synchronous counter, the counter increases or decreases in every clock signal rise. The counter should be disabled when the output voltage is stable between threshold voltages V_{LOW} and V_{HIGH} in order to reduce oscillations and ripple. The stability detection is illustrated in item (A) of Figure 68 and returns a high logic signal on node *stable* when both UP and DOWN signals have a low logic signal.

Figure 67 – Synchronous 5-bit up/down counter using full-adder and registers.



Source: Author.

Figure 68 – Logic system to enable registers, detection of stability and underflow/overflow, and mode selection.



Source: Author.

The underflow and overflow detection is made of a NOR and an AND logic gate, respectively, with the four outputs b_0 , b_1 , b_2 and b_3 of the counter, as shown in item (C) of Figure 68.

The selection of the SC Converter mode (doubler and tripler) is made through a detection of the overflow or underflow of the counter and a SR (set-reset) latch. If the counter is at the lowest digital code (0) and there the DOWN signal is a logic high, the output *MODE* should return a low logic-level for the doubler mode. If the counter is at the highest digital code (15) and the UP signal is logic high, the output *MODE* should return a high logic-level for the tripler mode. The mode selector is illustrated in item (D) of Figure 68.

The system that enables and disables the registers of the counter is illustrated in item (B) of Figure 68. If the *stable* signal is at high logic-level and an underflow or overflow

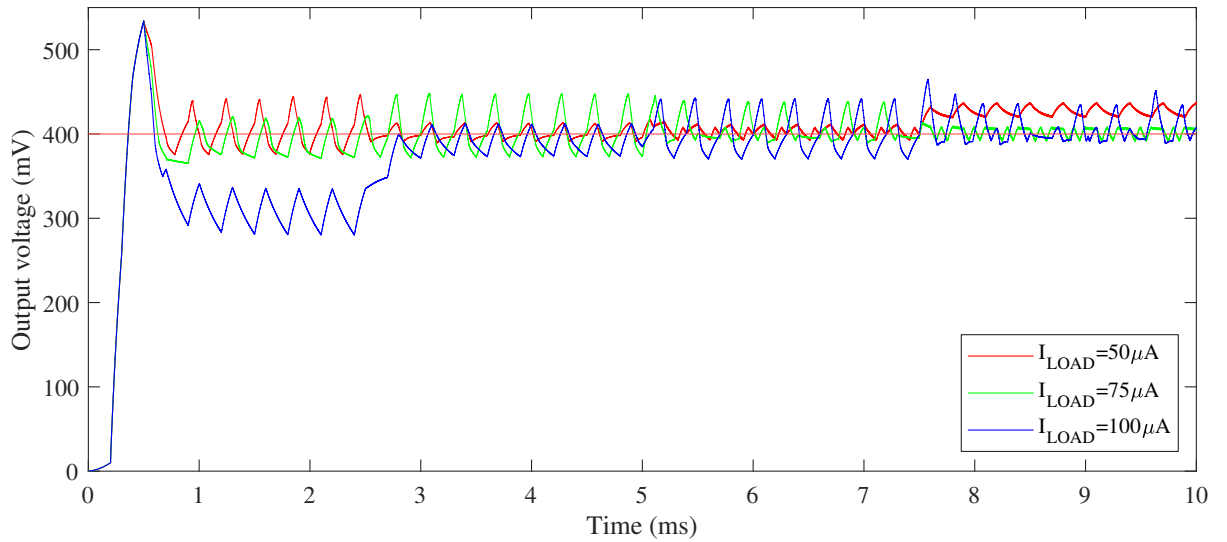
is detected, the *ENABLE* signal returns a low logic-level and disables the registers. This system is illustrated in item (B) of Figure 68.

4.4 RESULTS

This section presents and discusses the results obtained from simulations with the complete Energy Harvesting system illustrated in Figure 56.

Figure 69 shows a transient simulation of the output voltage of the proposed energy harvesting system for current loads of $50\ \mu\text{A}$, $75\ \mu\text{A}$, and $100\ \mu\text{A}$, to represent power outputs of $20\ \mu\text{W}$, $30\ \mu\text{W}$ and $40\ \mu\text{W}$, respectively.

Figure 69 – Output voltage of the converter for current loads of $50\ \mu\text{A}$, $75\ \mu\text{A}$, and $100\ \mu\text{A}$ with input voltages of 230 mV up to 260 mV.



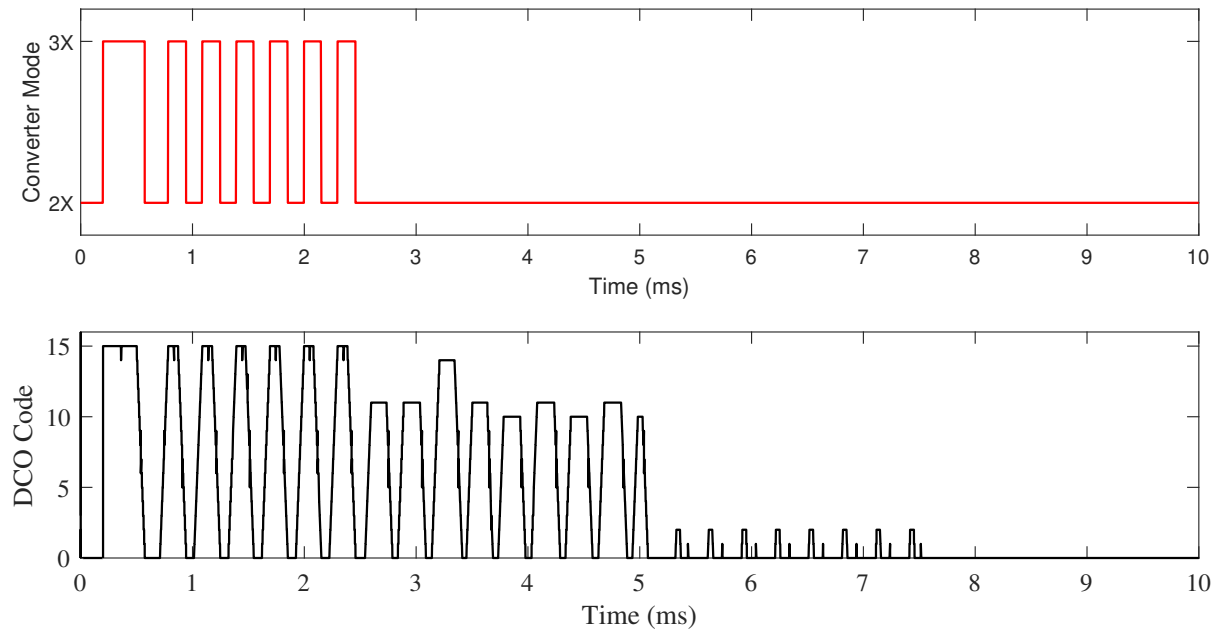
Source: Author.

From the start of the transient simulation up to a period of $500\ \mu\text{s}$, the system is ongoing the cold-start phase with an input voltage of 230 mV, where the supply voltage V_{DD} is generated for all subsystems, including the DCO. After this cold-start phase, the circuit starts the operation phase.

Figure 70 shows the transient simulation of the SC converter's mode and also shows the digital code of the DCO, considering a current load of $50\ \mu\text{A}$.

The analysis starts with an input voltage of 230 mV, and shows that after the start-up stage up to 2.5 ms, the converter is able to reach an output voltage of 400 mV with the $50\ \mu\text{A}$ load. The feedback control is able to maintain the output voltage within an upper and lower threshold, but, ripple is higher in this situation where the converter mode is changed continuously. In this case, the DCO code does a full sweep in the frequencies to maintain a constant output voltage. At 2.5 ms, the input voltage is increased to 240 mV, and as expected, it reaches a voltage of 400 mV with a small ripple. At 5 ms, the input

Figure 70 – Transient of converter mode and DCO digital code of the SC Converter for a $50\ \mu\text{A}$ current load.



Source: Author.

voltage is increased to 250 mV, and similarly, is able to maintain the desired output voltage. At 7.5 ms, the input voltage is increased to 260 mV, and is operating at the limit, where it is not able to decrease the DCO code and converter mode, depending only on the input voltage. Therefore, the output voltage is a bit higher than the desired output voltage of 400 mV.

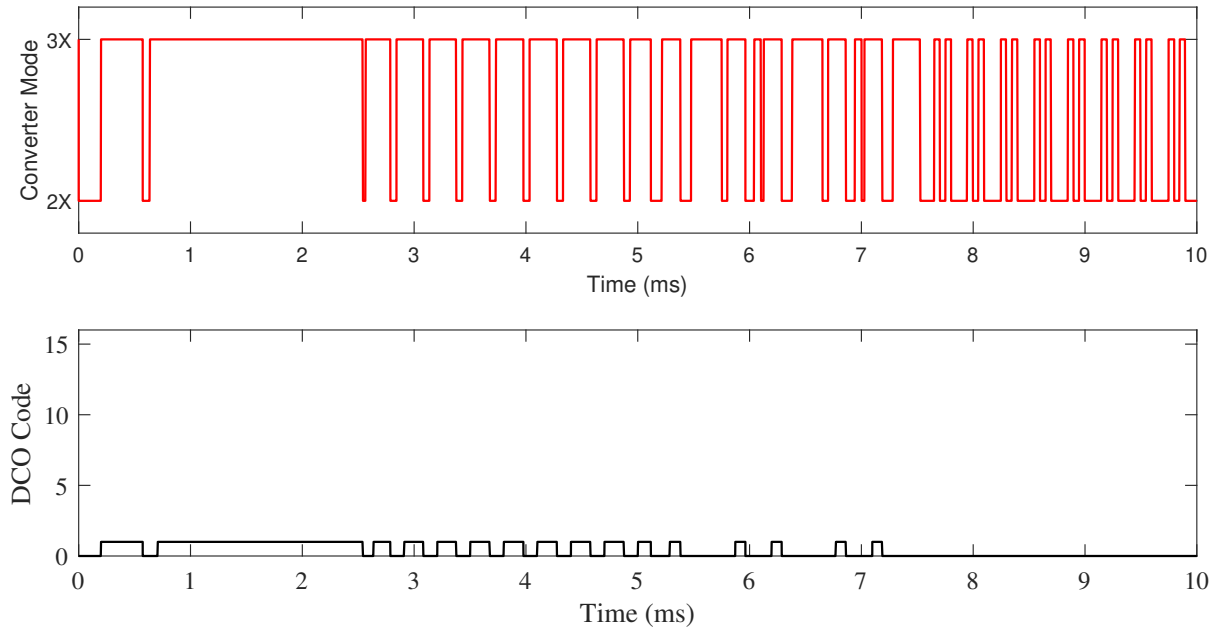
Figure 71 shows the transient simulation of the SC converter's mode and also shows the digital code of the DCO, considering a current load of $75\ \mu\text{A}$.

The analysis starts with an input voltage of 230 mV, and shows that after the start-up stage up to 2.5 ms, the converter is able to reach an output voltage of 400 mV with the $75\ \mu\text{A}$ load. In this case, the DCO code does a full sweep in the frequencies to maintain a constant output voltage. At 2.5 ms, the input voltage is increased to 240 mV and is able to reach the desired output voltage with a voltage ripple of $\pm 30\ \text{mV}$. A similar situation is encountered at 5 ms and 7.5 ms, when the input voltage is increased to 250 mV and 260 mV, respectively. It is also noticeable that the SC converter is operating in a region where the converter mode is constantly switching, thus, creating a higher voltage ripple.

Figure 72 shows the transient simulation of the SC converter's mode and also shows the digital code of the DCO, considering a current load of $100\ \mu\text{A}$.

The analysis starts with an input voltage of 230 mV, and shows that after the start-up stage up to 2.5 ms, the converter is not able to reach an output voltage of 400 mV, thus, requiring a higher input voltage to do so. At 2.5 ms, the input voltage is increased to

Figure 71 – Transient of converter mode and DCO digital code of the SC Converter for a $75\ \mu\text{A}$ current load.



Source: Author.

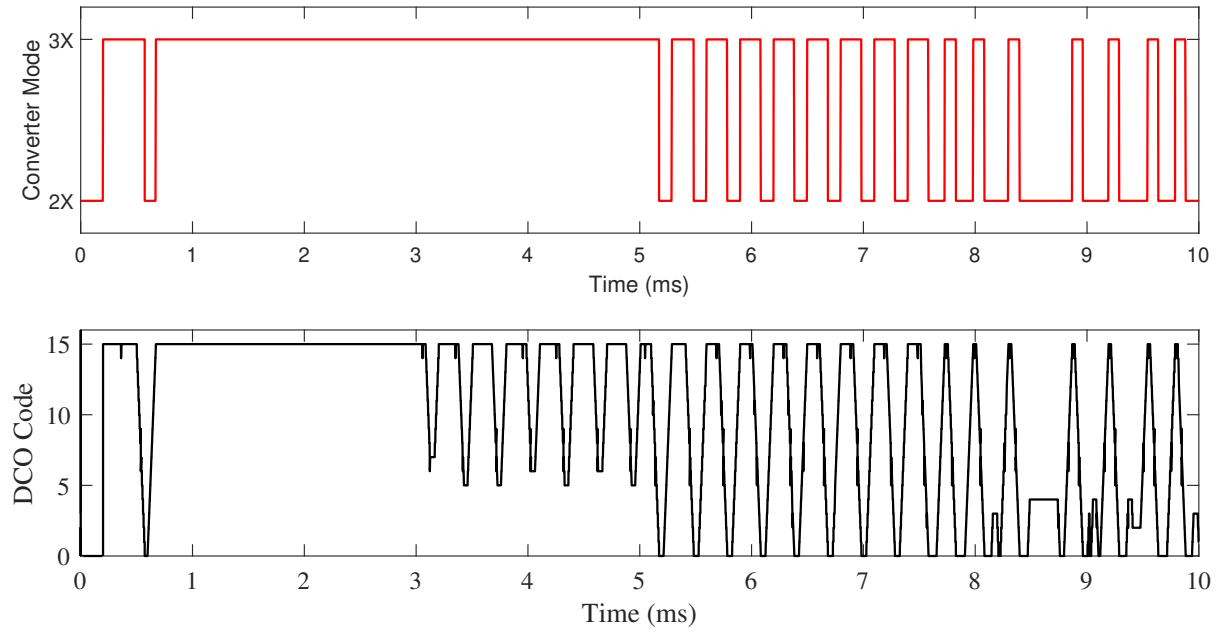
240 mV and is able to reach the desired output voltage with a voltage ripple of ± 20 mV, considering that the converter mode is constant. At 5 ms and 7.5 ms, for input voltages of 250 mV and 260 mV, respectively, full DCO digital code sweeps are done to maintain the 400 mV output voltage, thus, the converter mode is constantly changing between doubler and tripler mode, hence the higher voltage ripple.

The output voltage is highly dependant on input voltage as shown in the VCR analysis of Figure 66, as it starts under a voltage of 230 mV and reaches a voltage of 400 mV at the output, with the exception of the simulation for a $100\ \mu\text{A}$ current load that is not able to reach the required voltage.

The high voltage ripple in the output voltage V_{OUT} can affect circuits that require a stable supply voltage, such as ADCs and DACs. But, the converter can be used in cases where a very stable voltage is unneeded. The ripple can be reduced with the use of a large external buffer capacitor in the range of microfarads, although, it is not viable for simulation due to the simulation time, thus, tests are made with a 50 nF buffer capacitor.

When V_{OUT} reaches the upper threshold of the comparator, the next clock rise signal must be crossed in order to decrease the frequency of the DCO. A single decrease may not be enough, thus, the situation repeats until the voltage is at a stable level. The clock frequency of the logic system is around 200 kHz, but can be even lower when considering a larger buffer capacitor. Another situation that creates the voltage ripple is the transition between doubler and tripler modes (iVCR 2 and 3), due to the fast charge of the buffer capacitor it causes voltages peaks.

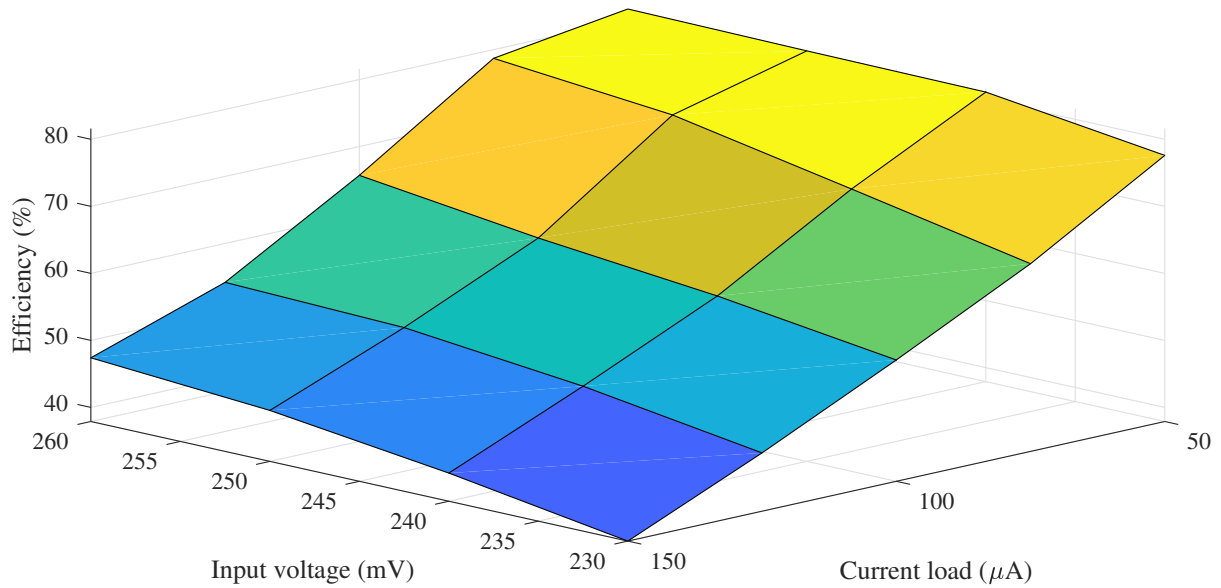
Figure 72 – Transient of converter mode and DCO digital code of the SC Converter for a $100\ \mu\text{A}$ current load.



Source: Author.

The average module of the instantaneous power at steady-state is used to measure the efficiency of the SC converter. Figure 73 shows a surface of steady-state efficiency of the SC converter in function of input voltage and current load.

Figure 73 – Efficiency of the complete energy harvesting system.

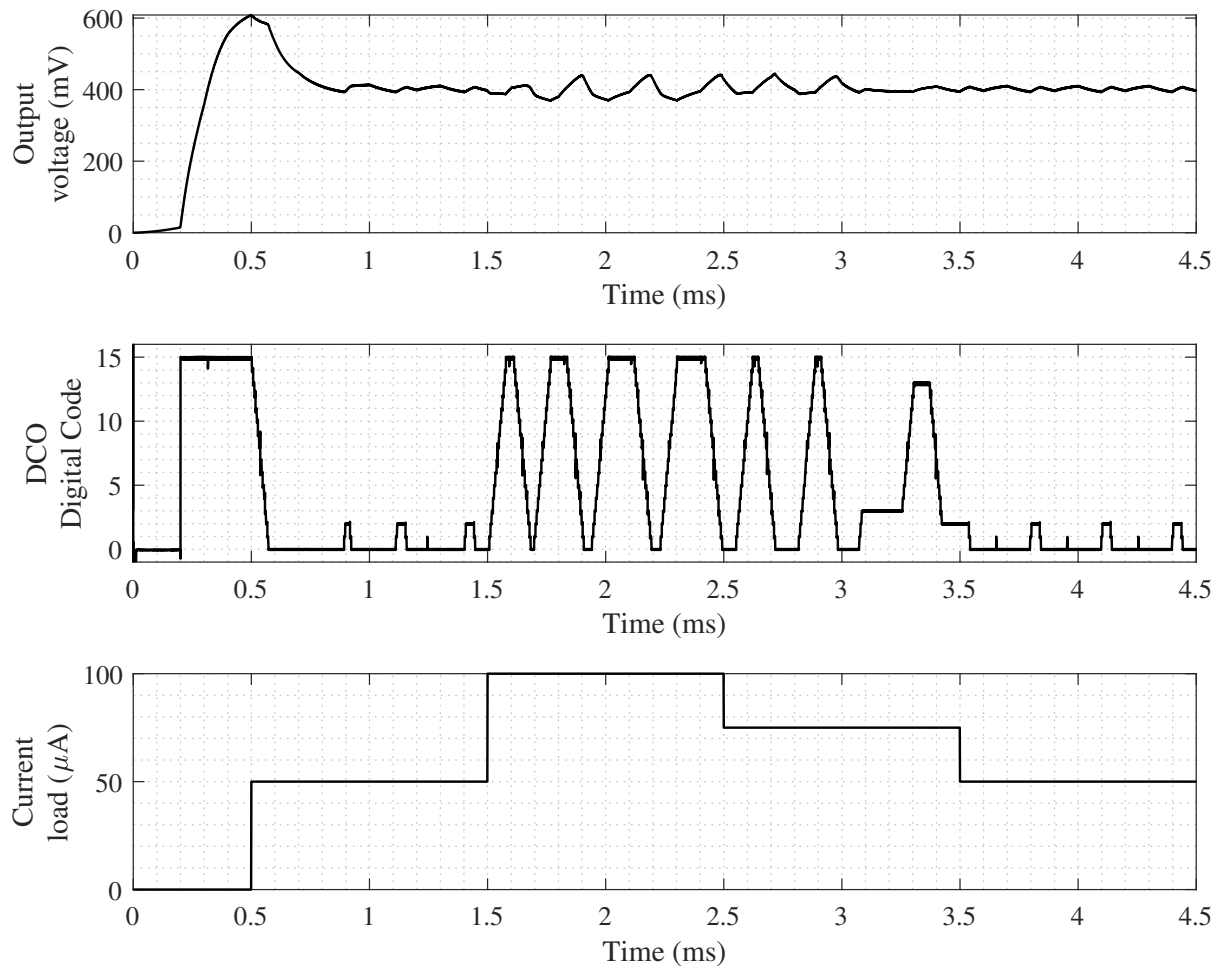


Source: Author.

The converter's peak efficiency of 81.6% is reached at an input voltage of 260 mV for a current load of $50\ \mu\text{A}$.

A transient simulation at schematic level of an abrupt variation in current load is illustrated in Figure 74. The output voltage manages to stay stable through the abrupt changes in load. Similar to the tests from above, the DCO digital code is on its inferior limit with a low load of $50\ \mu\text{A}$, and during high loads it starts to increase and decrease until stability is found.

Figure 74 – Transient simulation of an abrupt change in current load.



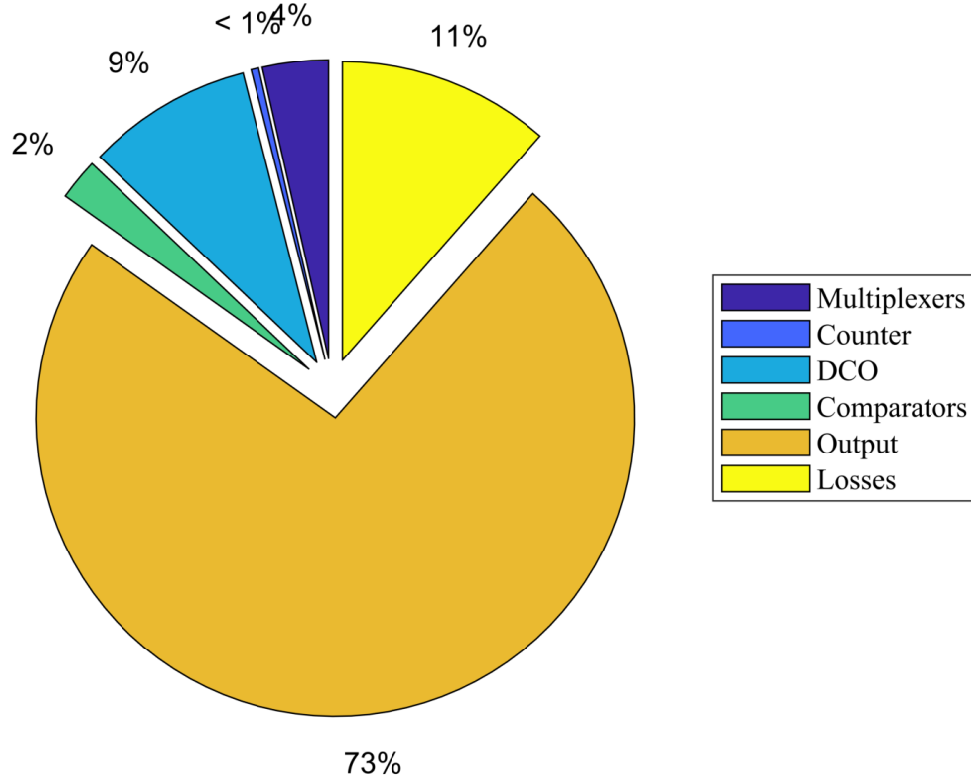
Source: Author.

Figure 75 shows the distribution of power consumption on the energy harvesting system considering an input voltage of 250 mV and a load of $30\ \mu\text{W}$. The counter accounts for less than one percent of the power consumption each (169 nW). The comparator accounts for less than one percent of the power consumption (122 nW), but, the 90 nA current-reference increases it to 3%, with a consumption of 933 nW. The multiplexers have a power consumption of $1.48\ \mu\text{W}$. The consumption in the DCO is $3.72\ \mu\text{W}$.

Table 12 shows a comparison of the proposed energy harvester with two state-of-the-art energy harvesters.

The proposed energy harvester presents a peak efficiency of 81.24% with an input voltage of 260 mV, which is comparable to other works in the state-of-the-art. Although,

Figure 75 – Pie-chart of power consumption considering a V_{IN} of 250 mV and a $30 \mu\text{W}$ load.



Source: Author.

for a lower input voltage, such as 230 mV, the efficiency is in the range of 40% to 50%, which is low in comparison to other works. Also, three external capacitors are required, two flying-capacitors and a buffer capacitor for the primary SC Converter. The secondary SC converter that generates the supply voltage for subsystems is fully-integrated with MIM capacitors.

It provides a voltage of 400 mV, and a minimum output power of $30 \mu\text{W}$ with an input voltage of 230 mV. The output power can be increased at the cost of a higher input voltage, for example it is able to drive a $50 \mu\text{W}$ load at 260 mV. Also, our work was able to operate in lower input voltage compared to (DEVARAJ et al., 2019). Still, it is much higher than inductor-based topologies such as (CAO et al., 2019), that operates with input voltages down to ± 25 mV, although, requires +129 mV/-140 mV to cold-start.

4.5 CONCLUSION

The proposed energy harvesting system is able to provide power to an ULP device between $30 \mu\text{W}$ and $40 \mu\text{W}$ for a minimum input voltage of 230 mV, supplying it with a voltage of 400 mV. The idea of the work is to use a control system with comparators and a digital counter to adjust the switching frequency and the output voltage of a

Table 12 – Comparison with state-of-the-art energy harvesters.

Specification	This work	(DEVARAJ et al., 2019)	(CAO et al., 2019)
Technology	180 nm	65 nm	180 nm
Topology	SC	SC	SI
Input voltage	230 mV	550 mV	± 25 mV
Output voltage	0.4 V	1.8–2.5 V	0.8 V
Output power	20–40 μ W	35–70 μ W	67.6 μ W
Conversion Efficiency	81.6% (20 μ A @ 260 mV)	74.6%	84%
Energy source	Indoor-Light	Piezo and Solar	Thermoelectric
Has cold-start?	Yes	No	Yes
External components	3 Capacitors	No	1 Transformer

Source: Author.

switched-capacitor converter that is provided power by indoor-light energy harvesting. This work was able to obtain a peak efficiency of 81.24% at 260 mV, although it requires three external capacitors.

5 CONCLUSION

Energy Harvesting is an emerging technology in the twenty-first century. In recent years, it has been used in batteryless applications to remove the need for batteries, as most batteries end up in landfills, endangering the environment with toxic substances. Many sources of energy are available, such as light, thermal, vibrations, and electromagnetic energies. Thermal and vibration energies are not reliable for indoor use, except for industrial applications. Although light energy is not always available outdoors, especially at nighttime, artificial lights such as fluorescent light bulbs can be used at indoor ambients to provide power to PV cells for long periods.

DC-DC converters can be used in numerous applications in ultra-low power systems, especially in applications related to the Internet of Things. Even though inductor-based converters are dominant in discrete implementation, capacitors are preferred in fully integrated implementations because capacitors are easier to manufacture with high quality. Many switched-capacitor DC-DC converters found in the literature are used for energy harvesting, and most of them use multi-topology converters to obtain a broader range of conversion ratios and higher efficiency.

Transducers are non-ideal devices and have finite series resistance, therefore, the analytical model of the output resistance of switched-capacitor converters should include the series resistance of the transducer. A few state-of-the-art methods to accurately model the equivalent output resistance are available, such as the Charge Flow Analysis. A new method to model the equivalent output resistance based on the Charge Flow analysis is proposed and includes the effects of the source resistance.

An Energy Harvesting system, consisting of a dual-mode switched-capacitor DC-DC converter is proposed to obtain an output voltage of 400 mV using photovoltaic cells with indoor-light levels of illuminance. The proposed system is able to provide power to an ultra-low power device between 20 μ W and 40 μ W for a minimum input voltage of 230 mV. The idea of the work is to use a hysteretic control system with comparators and a logic system to adjust the switching frequency and VCR of the converter. This work was able to obtain peak efficiency of 81.24% at 260 mV for a 20 μ W current load, although it requires three external capacitors.

5.1 FUTURE WORKS

As future works for this research theme, it is suggested to: implement an MPPT system for better power conversion efficiency; optimize the power consumption of the DCO by reducing the supply voltage to 0.4 V; optimize the cold-start system to work under lower input voltages; reduce the voltage ripple in higher loads by implementing a third iVCR in the multi-topology SC converter.

BIBLIOGRAPHY

- ABDELHADY, S.; ABD-ELHADY, M. S.; FOUAD, M. M. An Understanding of the Operation of Silicon Photovoltaic Panels. *Energy Procedia*, v. 113, p. 466–475, may 2017. ISSN 18766102. Available at <<https://linkinghub.elsevier.com/retrieve/pii/S1876610217321641>>. Cited on page 29.
- ALLEN, P. E.; HOLBERG, D. R. *CMOS Analog Circuit Design*. [S.l.]: Oxford University Press, 2002. 797 p. Cited 2 times on pages 48 and 49.
- BABAYAN-MASHHADI, S.; LOTFI, R. Analysis and design of a low-voltage low-power double-tail comparator. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, v. 22, n. 2, p. 343–352, 2014. Cited on page 81.
- BALLO, A.; GRASSO, A. D.; PALUMBO, G. A subthreshold cross-coupled hybrid charge pump for 50-mV cold-start. *IEEE Access*, v. 8, p. 188959–188969, 2020. ISSN 21693536. Cited on page 39.
- BOSE, S.; ANAND, T.; JOHNSTON, M. L. Fully-integrated 57 mv cold start of a thermoelectric energy harvester using a cross-coupled complementary charge pump. In: *IEEE Custom Integrated Circuits Conference*. [S.l.: s.n.], 2018. p. 1–4. Cited 2 times on pages 67 and 69.
- BRADSHAW, A. M.; REUTER, B.; HAMACHER, T. The Potential Scarcity of Rare Elements for the Energiewende. *Green*, v. 3, n. 2, p. 93–111, jan 2013. ISSN 1869-8778. Available at <<https://www.degruyter.com/document/doi/10.1515/green-2013-0014/html>>. Cited 2 times on pages 30 and 31.
- CAO, P. et al. A Bipolar-Input Thermoelectric Energy-Harvesting Interface With Boost/Flyback Hybrid Converter and On-Chip Cold Starter. *IEEE Journal of Solid-State Circuits*, v. 54, n. 12, p. 3362–3374, 2019. Cited 3 times on pages 67, 90, and 91.
- CARVALHO, C. M. F.; PAULINO, N. F. S. V. *CMOS Indoor Light Energy Harvesting System for Wireless Sensing Applications*. Cham: Springer International Publishing, 2016. ISBN 978-3-319-21616-4. Available at <<http://link.springer.com/10.1007/978-3-319-21617-1>>. Cited 4 times on pages 20, 21, 22, and 29.
- CHEN, Z. Effective regeneration of LiCoO₂ from spent lithium-ion batteries: a direct approach towards high-performance active particles. Royal Society of Chemistry, 2018. ISSN 1463-9262. Cited on page 17.
- CHENG, H. C. et al. A Redistributable Capacitive Power Converter for Indoor Light-Powered Batteryless IoT Devices. *IEEE Solid-State Circuits Letters*, v. 3, p. 350–353, 2020. ISSN 25739603. Cited 3 times on pages 20, 43, and 44.
- CHOUHAN, S. S.; HALONEN, K. The design and implementation of DTMOS biased all PMOS rectifier for RF energy harvesting. *2014 IEEE 12th International New Circuits and Systems Conference, NEWCAS 2014*, p. 444–447, 2014. Cited on page 39.
- CHURCHILL, K. K. P. et al. Low-voltage capacitive-based Step-Up DC-DC converters for RF energy harvesting system: A review. *IEEE Access*, v. 8, p. 186393–186407, 2020. ISSN 21693536. Cited 5 times on pages 17, 18, 24, 25, and 26.

COMPASSI-SEVERO, L.; Van Noije, W. A 0.4-V 10.9- μ W/Pole Third-Order Complex BPF for Low Energy RF Receivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, v. 66, n. 6, p. 2017–2026, 2019. ISSN 15580806. Cited on page 20.

CORRADINI, L. et al. *Energy Harvesting - Power Electronics Group*. 2014. Available at <<http://pelgroup.dei.unipd.it/energyharvesting>>. Cited on page 17.

DABAS, S.; KUMAR, M. A new design of digitally controlled oscillator for low power applications. In: *2016 2nd International Conference on Contemporary Computing and Informatics (IC3I)*. IEEE, 2016. p. 671–675. ISBN 978-1-5090-5256-1. Available at <<http://ieeexplore.ieee.org/document/7918047/>>. Cited on page 65.

DAS, S. Development of a Low-cost, Portable, and Programmable Solar Module to Facilitate Hands-on Experiments and Improve Student Learning. In: *2016 ASEE Annual Conference Exposition Proceedings*. ASEE Conferences, 2016. Available at <<http://peer.asee.org/26800>>. Cited on page 32.

DEVARAJ, A. et al. A Switched Capacitor Multiple Input Single Output Energy Harvester (Solar + Piezo) Achieving 74.6% Efficiency with Simultaneous MPPT. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 66, n. 12, p. 4876–4887, 2019. ISSN 15580806. Cited 8 times on pages 19, 28, 33, 41, 42, 43, 90, and 91.

DEZYANI, M. et al. A 60 mV Input Voltage, Process Tolerant Start-Up System for Thermoelectric Energy Harvesting. *IEEE Transactions on Circuits and Systems I: Regular Papers*, IEEE, v. 65, n. 10, p. 3568–3577, 2018. ISSN 15498328. Cited on page 27.

DIAS, T. (Ed.). *Electronic Textiles: Smart Fabrics and Wearable Technology*. 1. ed. Woodhead Publishing, 2015. ISBN 9780081002018. Available at <<https://linkinghub.elsevier.com/retrieve/pii/C20140030201>>. Cited 2 times on pages 27 and 28.

DIGIKEY.COM. *DFR0379*. 2021. Available at <<https://www.digikey.com/en/products/detail/dfrobot/DFR0379/7087190>>. Cited on page 19.

DIGIKEY.COM. *Mide Technology Corporation PPA-1014*. 2021. Available at <<https://www.digikey.com/en/products/detail/mide-technology-corporation/PPA-1014/6190298>>. Cited on page 28.

DUTRA, L. F. M.; GIRARDI, A.; COMPASSI-SEVERO, L. Modelling the Equivalent Output Resistance of Integrated SC DC-DC Converters Including Source Resistance Effects. In: *36th South Symposium on Microelectronics*. [S.l.: s.n.], 2021. p. 55–58. Cited 2 times on pages 22 and 55.

DUTRA, L. F. M.; GIRARDI, A.; COMPASSI-SEVERO, L. Analytical Model for Output Resistance of SC Converters including Source Resistance Effects. In: *37th South Symposium on Microelectronics*. [S.l.: s.n.], 2022. Cited on page 22.

DUTRA, L. F. M.; GIRARDI, A. G.; COMPASSI-SEVERO, L. A 0.3 to 5-MHz Low-Voltage Digitally-Controlled Oscillator for Energy Harvesting Applications. In: *35th Symp. on Integr. Circ. and Systems Design*. [S.l.: s.n.], 2022. ISBN 9781665481281. Cited 2 times on pages 22 and 68.

GAIKWAD, K.; LOKHANDE, S. Novel maximum power point tracking (MPPT) algorithm for solar tree application. In: *2015 International Conference on Energy Systems and Applications*. IEEE, 2015. p. 189–193. ISBN 978-1-4673-6817-9. Available at <<http://ieeexplore.ieee.org/document/7503337/>>. Cited on page 20.

GEISZ, J. F. et al. Six-junction III–V solar cells with 47.1% conversion efficiency under 143 Suns concentration. *Nature Energy*, Springer US, v. 5, n. 4, p. 326–335, 2020. ISSN 2058-7546. Available at <<http://dx.doi.org/10.1038/s41560-020-0598-5>>. Cited on page 29.

GUTIERREZ, F. Fully-Integrated Converter for Low-Cost and Low-Size Power Supply in Internet-of-Things Applications. *Electronics*, v. 6, n. 2, p. 38, 2017. ISSN 2079-9292. Cited 2 times on pages 45 and 46.

HU, X. et al. Battery Lifetime Prognostics. *Joule*, v. 4, n. 2, p. 310–346, 2020. ISSN 25424351. Available at <<http://dx.doi.org/10.1016/j.rser.2015.11.010>>. Cited on page 17.

JEON, B.-g.; MOON, Y.; AHN, T.-w. A study on 11 MHz x007E; 1537 MHz DCO using tri-state inverter for DAB application. In: *TENCON 2009 - 2009 IEEE Region 10 Conference*. IEEE, 2009. p. 1–5. ISBN 978-1-4244-4546-2. Available at <<http://ieeexplore.ieee.org/document/5395955/>>. Cited on page 65.

KANG, D. H. P.; CHEN, M.; OGUNSEITAN, O. A. Potential Environmental and Human Health Impacts of Rechargeable Lithium Batteries in Electronic Waste. *Environmental Science Technology*, v. 47, n. 10, p. 5495–5503, may 2013. ISSN 0013-936X. Available at <<http://dx.doi.org/10.1021/es400614y>>. Cited on page 17.

KESARWANI, K.; SANGWAN, R.; STAUTH, J. T. Resonant-switched capacitor converters for chip-scale power delivery: Design and implementation. *IEEE Transactions on Power Electronics*, v. 30, n. 12, p. 6966–6977, 2015. Cited on page 74.

KIZIROGLOU, M.; YEATMAN, E. Materials and techniques for energy harvesting. In: *Functional Materials for Sustainable Energy Applications*. Elsevier, 2012. p. 541–572. ISBN 9780857090591. Available at <<http://dx.doi.org/10.1016/9780857096371.4.539>>. Cited 6 times on pages 17, 24, 26, 27, 28, and 67.

KOO, J. et al. A quadrature rc oscillator with noise reduction by voltage swing control. *IEEE Transactions on Circuits and Systems I: Regular Papers*, v. 66, n. 8, p. 3077–3088, 2019. Cited 2 times on pages 65 and 66.

KRAMP, T.; KRANENBURG, R. van; LANGE, S. Introduction to the Internet of Things. In: *Enabling Things to Talk*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2013. p. 1–10. ISBN 9783642404030. Available at <http://link.springer.com/10.1007/978-3-642-40403-0_1>. Cited on page 17.

LU, S.-Y.; LIAO, Y.-T. A low-power, differential relaxation oscillator with the self-threshold-tracking and swing-boosting techniques in 0.18- μ m cmos. *IEEE Journal of Solid-State Circuits*, v. 54, n. 2, p. 392–402, 2019. Cited 2 times on pages 65 and 66.

MACHADO, M. B. et al. Fully-integrated 86 mV–1V step-up converter for energy harvesting applications. In: *2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)*. [S.l.: s.n.], 2014. p. 452–455. Cited on page 73.

- MAKSIMOVIC, D.; DHAR, S. Switched-capacitor DC-DC converters for low-power on-chip applications. In: *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*. [S.l.]: IEEE, 1999. v. 1, p. 54–59. ISBN 0-7803-5421-4. Cited 2 times on pages 37 and 47.
- MIDE Engineering Solutions. *Piezo Product: PPA-1014*. 2021. Available at <<https://www.mide.com/products/piezo-product-ppa-1014>>. Cited on page 28.
- MILLER, C. A.; PETERS, I. M.; SHIVAM, Z. *Thin Film CdTe Photovoltaics and the U.S. Energy Transition in 2020*. [S.l.], 2020. Available at <<https://www.firstsolar.com/-/media/First-Solar/Sustainability-Documents/Sustainability-Peer-Reviews/QESST-Thin-Film-PV-Report-2020.ashx>>. Cited on page 30.
- MONTEIRO, V. et al. Parameter Extraction Methodology of 1D2R PV Cell Electrical Model for Indoor Applications. In: *36th Symposium on Microelectronics Technology (SBMICRO)*. [S.l.: s.n.], 2022. Cited 4 times on pages 22, 32, 45, and 72.
- MONTEIRO, V. A. et al. PV Cell Electrical Model Parameter Extraction Methodology for Low Illuminance Scenarios. In: *37th South Symposium on Microelectronics*. [S.l.: s.n.], 2022. Cited on page 22.
- OLIVEIRA, A. C. de et al. Picowatt, 0.45–0.6 V Self-Biased Subthreshold CMOS Voltage Reference. *IEEE Transactions on Circuits and Systems I: Regular Papers*, v. 64, n. 12, p. 3036–3046, 2017. Cited on page 81.
- OSAKI, Y. et al. Nano-ampere cmos current reference with little temperature dependence using small offset voltage. In: *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*. [S.l.: s.n.], 2010. p. 668–671. Cited on page 82.
- RABAEY, J. M.; CHANDRAKASAN, A. P.; NIKOLIC, B. *Digital Integrated Circuits: A Design Perspective*. 2. ed. [S.l.]: Prentice Hall, 2003. 761 p. ISBN 9780130909961. Cited 2 times on pages 56 and 57.
- RAGHUNATHAN, V.; CHOU, P. H. Design and power management of energy harvesting embedded systems. In: *Proceedings of the 2006 international symposium on Low power electronics and design - ISLPED '06*. New York, New York, USA: ACM Press, 2006. p. 369. ISBN 1595934626. Available at <<http://portal.acm.org/citation.cfm?doid=1165573.1165663>>. Cited on page 20.
- RASHEED, M.; SHIHAB, S. Parameters Estimation for Mathematical Model of Solar Cell. *Electronics Science Technology and Application*, p. 20–28, 2019. Cited on page 32.
- RAZAVI, B. The strongarm latch [a circuit for all seasons]. *IEEE Solid-State Circuits Magazine*, v. 7, n. 2, p. 12–17, 2015. Cited on page 81.
- RAZAVI, B. *Design of Analog CMOS Integrated Circuits*. 2th. ed. New York: McGraw-Hill Education, 2016. 801 p. ISBN 9780072524932. Cited 2 times on pages 81 and 82.
- SEEMAN, M.; SANDERS, S. Analysis and Optimization of Switched-Capacitor DC-DC Converters. In: *2006 IEEE Workshops on Computers in Power Electronics*. [S.l.]: IEEE, 2006. p. 216–224. Cited on page 37.

SEEMAN, M. D. *Analytical and practical analysis of switched-capacitor DC-DC converters*. 66 p. Thesis (Masters) — University of California, Berkeley, 2006. Available at <<http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-111.html>>. Cited 5 times on pages 35, 36, 37, 45, and 46.

SEEMAN, M. D. *A Design Methodology for Switched-Capacitor DC-DC Converters*. 249 p. Dissertation (Ph.D. dissertation) — University of California, Berkeley, 2009. Available at <<http://www.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html>>. Cited on page 46.

SEEMAN, M. D. et al. A comparative analysis of Switched-Capacitor and inductor-based DC-DC conversion technologies. In: *2010 IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2010. p. 1–7. ISBN 978-1-4244-7462-2. Available at <<http://ieeexplore.ieee.org/document/5562407/>>. Cited on page 19.

SHAH, A. V. et al. Thin-film silicon solar cell technology. *Progress in Photovoltaics: Research and Applications*, v. 12, n. 23, p. 113–142, mar 2004. ISSN 1062-7995. Available at <<https://onlinelibrary.wiley.com/doi/10.1002/pip.533>>. Cited on page 29.

SHAIKH, F. K.; ZEADALLY, S. Energy harvesting in wireless sensor networks: A comprehensive review. *Renewable and Sustainable Energy Reviews*, Elsevier, v. 55, p. 1041–1054, mar 2016. ISSN 13640321. Available at <<http://dx.doi.org/10.1016/j.rser.2015.11.010>>. Cited on page 17.

SILVA, L. A. *Integrated DC-DC Converter for Photovoltaic Energy Harvesting Targeted to Indoor Applications*. 104 p. Thesis (Masters) — Federal University of Pampa, Alegrete, Brazil, 2020. Cited 11 times on pages 32, 33, 37, 39, 42, 43, 45, 50, 55, 67, and 77.

SILVA, L. A.; COMPASSI-SEVERO, L.; GIRARDI, A. A Practical Method for the Electrical Characterization of Low Energy - Indoor Photovoltaic Cells. In: *2019 South Symposium on Microelectronics (SIM)*. [S.l.: s.n.], 2019. Cited on page 18.

SILVA, L. A.; SEVERO, L. C.; GIRARDI, A. A Novel Fully Integrated ULV SC DC-DC Converter for Indoor Light Energy Harvesting. In: *2020 33rd Symposium on Integrated Circuits and Systems Design (SBCCI)*. IEEE, 2020. p. 1–6. ISBN 978-1-7281-9625-1. Available at <<https://ieeexplore.ieee.org/document/9189894/>>. Cited 3 times on pages 19, 40, and 75.

SOUSA, L. F. V. A. N. de. *Charge Pump for Solar Cell*. 108 p. Thesis (Masters) — Instituto Superior Técnico, 2017. Available at <<https://fenix.tecnico.ulisboa.pt/cursos/meec/dissertacao/565303595501517>>. Cited 2 times on pages 20 and 29.

SOYATA, T.; COPELAND, L.; HEINZELMAN, W. RF Energy Harvesting for Embedded Systems: A Survey of Tradeoffs and Methodology. *IEEE Circuits and Systems Magazine*, IEEE, v. 16, n. 1, p. 22–57, 2016. ISSN 1531636X. Cited 3 times on pages 17, 24, and 26.

STARZYK, J. A.; JAN, Y. W.; QIU, F. A DC-DC charge pump design based on voltage doublers. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, v. 48, n. 3, p. 350–359, 2001. ISSN 10577122. Cited on page 39.

SUNAR, B.; MARTIN, W.; STINSON, D. A Provably Secure True Random Number Generator with Built-In Tolerance to Active Attacks. *IEEE Transactions on Computers*, v. 56, p. 109–119, 1 2007. ISSN 0018-9340. Cited on page 56.

SVARC, J. *Clean Energy Reviews: Solar PV Cell Construction*. 2021. Available at <<https://www.cleanenergyreviews.info/blog/solar-pv-cell-construction>>. Cited on page 29.

TRAN, L.-G.; CHA, H.-K.; PARK, W.-T. RF power harvesting: a review on designing methodologies and applications. *Micro and Nano Systems Letters*, Springer Berlin Heidelberg, v. 5, n. 1, p. 14, dec 2017. ISSN 2213-9621. Available at <<http://mns-l-journal.springeropen.com/articles/10.1186/s40486-017-0051-0>>. Cited on page 18.

Van Breussegem, T.; STEYAERT, M. *CMOS Integrated Capacitive DC–DC Converters*. [S.l.]: Springer-Verlag New York, 2013. 218 p. ISBN 9781461442790. Cited 20 times on pages 19, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 45, 46, 50, 51, 67, 69, 74, 75, and 82.

WANG, W. et al. Thermoelectric Energy Harvesting for Building Energy Management Wireless Sensor Networks. *International Journal of Distributed Sensor Networks*, v. 9, n. 6, p. 232438, jun 2013. ISSN 1550-1477. Available at <<http://journals.sagepub.com/doi/10.1155/2013/232438>>. Cited 2 times on pages 26 and 27.

WANG, Y.-R.; YU, Z.-G. A high-efficiency cross-coupled charge pump for flash memories. In: *2010 2nd International Conference on Advanced Computer Control*. [S.l.]: IEEE, 2010. v. 3, p. 130–133. ISBN 978-1-4244-5845-5. Cited on page 47.

WESTE, N. H. E.; HARRIS, D. M. *CMOS VLSI design: a circuits and systems perspective*. 4th ed. ed. Boston: Addison Wesley, 2011. ISBN 978-0-321-54774-3. Cited on page 83.

YI, H. et al. A 0.032-mm² 0.15-V Three-Stage Charge-Pump Scheme Using a Differential Bootstrapped Ring-VCO for Energy-Harvesting Applications. *IEEE Trans. on Circuits and Systems II: Express Briefs*, v. 65, n. 2, p. 146–150, 2018. Cited 4 times on pages 43, 44, 70, and 71.

YIN, J. et al. A 0.2v energy-harvesting ble transmitter with a micropower manager achieving 25in 28nm cmos. In: *IEEE Int. Solid-State Circuits Conference*. [S.l.: s.n.], 2018. p. 450–452. Cited on page 73.

YING, T.; KI, W.-H.; CHAN, M. Area-efficient CMOS charge pumps for LCD drivers. *IEEE Journal of Solid-State Circuits*, v. 38, n. 10, p. 1721–1725, oct 2003. ISSN 0018-9200. Cited on page 47.

YOON, E. J.; PARK, J. T.; YU, C. G. Thermal energy harvesting circuit with maximum power point tracking control for self-powered sensor node applications. *Frontiers of Information Technology and Electronic Engineering*, v. 19, n. 2, p. 285–296, 2018. ISSN 20959230. Cited on page 19.

ZAMPARETTE, R. L. B. *High Efficiency MPPT Switched Capacitor DC-DC Converter for Photovoltaic Energy Harvesting Aiming for IoT Applications*. Thesis (Masters) — Federal University of Rio Grande do Sul, 2017. Available at <<https://lume.ufrgs.br/handle/10183/173738>>. Cited 2 times on pages 32 and 33.

ZENDEHDEL, M.; Yaghoobi Nia, N.; YAGHOUBINIA, M. Emerging Thin Film Solar Panels. In: *Reliability and Ecological Aspects of Photovoltaic Modules*. IntechOpen, 2020. Available at <<https://www.intechopen>>.

com/books/reliability-and-ecological-aspects-of-photovoltaic-modules/emerging-thin-film-solar-panels>. Cited 3 times on pages 29, 30, and 31.

ZHAO, J.; Yong-bin Kim. A 12-bit digitally controlled oscillator with low power consumption. In: *2008 51st Midwest Symposium on Circuits and Systems*. IEEE, 2008. p. 370–373. ISBN 978-1-4244-2166-4. ISSN 15483746. Available at <<http://ieeexplore.ieee.org/document/4616813/>>. Cited on page 57.

ZHOU, W.; GOH, W. L.; GAO, Y. A 3-mhz 17.3- μ w 0.015% period jitter relaxation oscillator with energy efficient swing boosting. *IEEE Transactions on Circuits and Systems II: Express Briefs*, v. 67, n. 10, p. 1745–1749, 2020. Cited 2 times on pages 65 and 66.

APPENDIX A – CHIP TEST BENCH

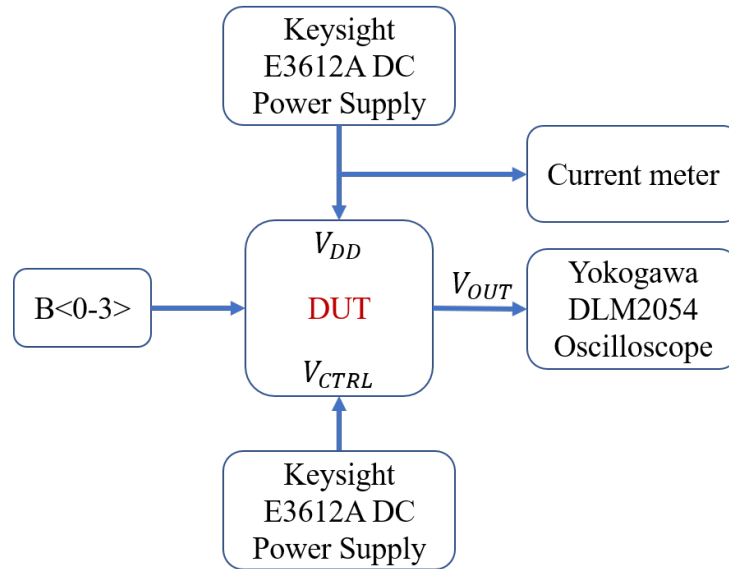
The test benches for devices on the chip are required to be tested with the following equipment: semiconductor probes, power supplies, oscilloscopes, and current-meters.

The chip is divided in a complete system, an individual DCO, and an individual DC-DC converter.

A.1 DCO INDIVIDUAL TEST BENCH

Figure 76 illustrates the individual test bench for the DCO as device on test (DUT), and it excludes all other subsystems, such as the DC-DC converter and the cold-start system.

Figure 76 – DCO Individual Test Bench.



Source: Author.

The supply voltage V_{DD} of 650 mV is obtained using a DC Power Supply from Keysight E3612A. The power supply output is connected to a current meter connected to measure the RMS current of the DUT in steady-state operation. The power consumption is measured using the V_{DD} voltage and measured RMS current.

The DCO has a four control signals to select the digital code, they are selectable using the B<0-3> device, which is a pull-down circuit for each bit. It uses the same voltage level of V_{DD} .

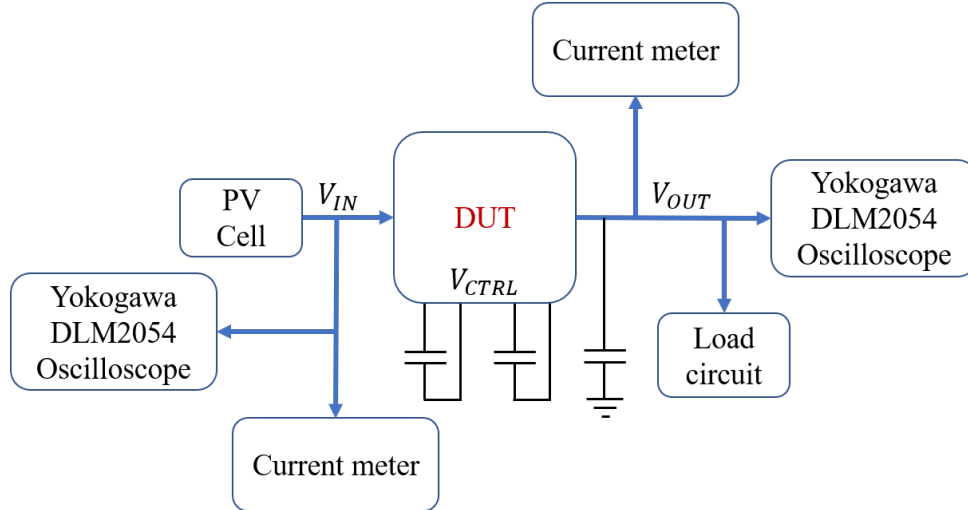
The V_{CTRL} voltage is also obtained using the Keysight E3612A, the range should be from 0 mV to 300 mV.

The frequency and amplitude of the output signal V_{OUT} are measured using a Yokogawa DML2054 oscilloscope.

A.3 COMPLETE ENERGY HARVESTING SYSTEM TEST BENCH

Figure 78 illustrates the complete energy harvesting system as device on test (DUT), and includes all subsystems, such as DCO and cold-start systems.

Figure 78 – Complete Energy Harvesting System Test Bench.



Source: Author.

The input of the energy harvesting system is a small 20 mm x 40 mm photovoltaic cell operating under different illuminance levels, and its voltage and current are measured using a Yokogawa DML2054 oscilloscope and a current meter, respectively.

The output of the energy harvesting system is connected to a load circuit of 20 μW to 40 μW , and the voltage is measured using a Yokogawa DML2054 oscilloscope. The current is obtained using a current meter to measure the current in steady-state operation.